

Features

- High speed
 - 15 ns
- Fast t_{DOE}
- CMOS for optimum speed/power
- Low active power
 - 550 mW (max, 15 ns “L” version)
- Low standby power
 - 0.275 mW (max, “L” version)
- 2 V data retention (“L” version only)
- Easy memory expansion with $\overline{CE}$ and $\overline{OE}$ features
- TTL-compatible inputs and outputs
- Automatic power-down when deselected

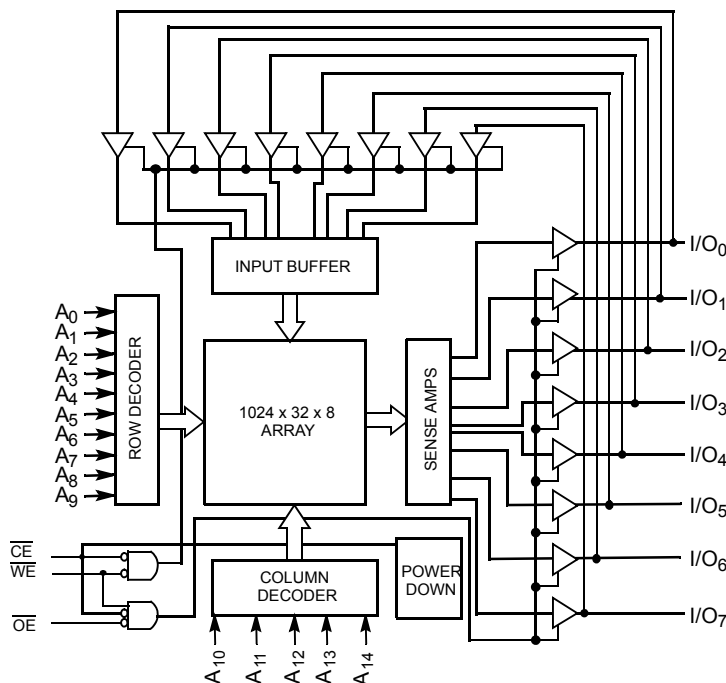
Functional Description

The CY7C199N is a high-performance CMOS static RAM organized as 32,768 words by 8 bits. Easy memory expansion is provided by an active LOW Chip Enable ($\overline{CE}$) and active LOW Output Enable ($\overline{OE}$) and three-state drivers. This device has an automatic power-down feature, reducing the power consumption by 81% when deselected. The CY7C199NN is in the standard 300-mil-wide DIP, SOJ, and LCC packages.

An active LOW Write Enable signal ($\overline{WE}$) controls the writing/reading operation of the memory. When $\overline{CE}$ and $\overline{WE}$ inputs are both LOW, data on the eight data input/output pins (I/O_0 through I/O_7) is written into the memory location addressed by the address present on the address pins (A_0 through A_{14}). Reading the device is accomplished by selecting the device and enabling the outputs, $\overline{CE}$ and $\overline{OE}$ active LOW, while $\overline{WE}$ remains inactive or HIGH. Under these conditions, the contents of the location addressed by the information on address pins are present on the eight data input/output pins.

The input/output pins remain in a high-impedance state unless the chip is selected, outputs are enabled, and Write Enable ($\overline{WE}$) is HIGH. A die coat is used to improve alpha immunity.

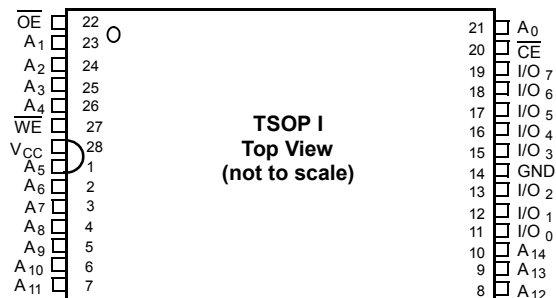
Logic Block Diagram



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Pin Configuration



Selection Guide

Description		-15	Unit
Maximum Access Time		15	ns
Maximum Operating Current	L	100	mA
Maximum CMOS Standby Current	L	0.05	mA

Maximum Ratings

Exceeding the maximum ratings may impair the useful life of the device. These user guidelines are not tested.

Storage Temperature -65 °C to +150 °C

Ambient Temperature with
Power Applied -55 °C to +125 °C

Supply Voltage to Ground Potential
(Pin 28 to Pin 14) -0.5 V to +7.0 V

DC Voltage Applied to Outputs
in High Z State^[1] -0.5 V to $V_{CC} + 0.5$ V

DC Input Voltage^[1] -0.5 V to $V_{CC} + 0.5$ V

Output Current into Outputs (LOW) 20 mA

Static Discharge Voltage > 2001 V
(per MIL-STD-883, Method 3015)

Latch-up Current > 200 mA

Operating Range

Range	Ambient Temperature ^[2]	V_{CC}
Commercial	0 °C to +70 °C	5 V $\pm$ 10%

Electrical Characteristics

Over the Operating Range

Parameter	Description	Test Conditions		-15		Unit
				Min	Max	
V _{OH}	Output HIGH Voltage	V _{CC} = Min, I _{OH} = −4.0 mA		2.4	–	V
V _{OL}	Output LOW Voltage	V _{CC} = Min, I _{OL} = 8.0 mA		–	0.4	V
V _{IH}	Input HIGH Voltage			2.2	V _{CC} + 0.3 V	V
V _{IL}	Input LOW Voltage			−0.5	0.8	V
I _{IX}	Input Load Current	GND ≤ V _I ≤ V _{CC}		−5	+5	μA
I _{OZ}	Output Leakage Current	GND ≤ V _O ≤ V _{CC} , Output Disabled		−5	+5	μA
I _{CC}	V _{CC} Operating Supply Current	V _{CC} = Max, I _{OUT} = 0 mA, f = f _{MAX} = 1/t _{RC}	L	–	100	mA
I _{SB1}	Automatic CE Power-down Current— TTL Inputs	Max V _{CC} , $\overline{CE} \geq V_{IH}$, V _{IN} ≥ V _{IH} or V _{IN} ≤ V _{IL} , f = f _{MAX}	L	–	5	mA
I _{SB2}	Automatic CE Power-down Current— CMOS Inputs	Max V _{CC} , CE ≥ V _{CC} − 0.3 V, V _{IN} ≥ V _{CC} − 0.3 V, or V _{IN} ≤ 0.3 V, f = 0	L	–	0.05	mA

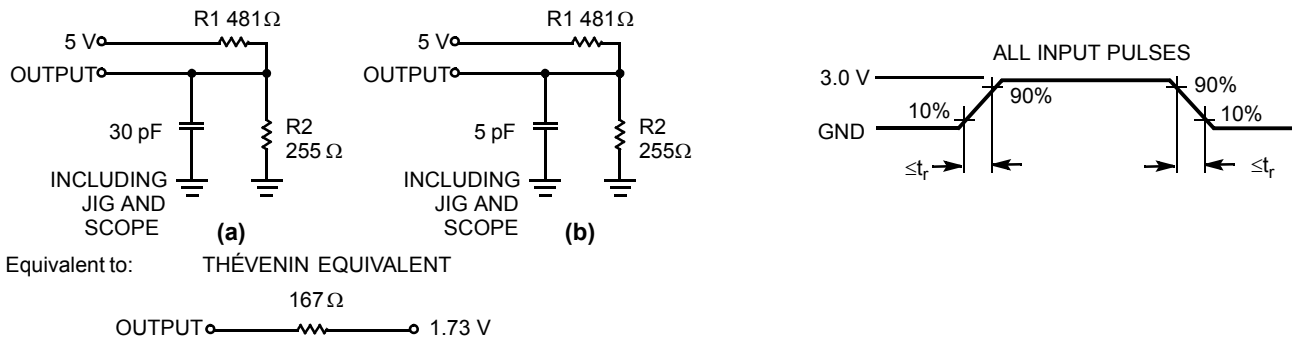
Notes

- $V_{IL}(\text{min}) = -2.0$ V for pulse durations of less than 20 ns.
- T_A is the "instant on" case temperature.

Capacitance^[3]

Parameter	Description	Test Conditions	Max	Unit
C _{IN}	Input Capacitance	T _A = 25 °C, f = 1 MHz, V _{CC} = 5.0 V	8	pF
C _{OUT}	Output Capacitance		8	pF

AC Test Loads and Waveforms^[4]

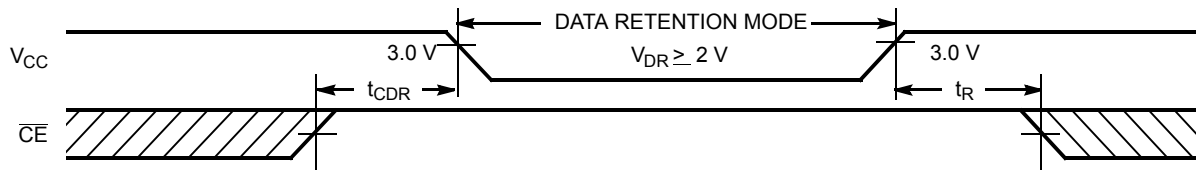


Data Retention Characteristics

Over the Operating Range (L-version only)

Parameter	Description	Conditions ^[5]	Min	Max	Unit
V _{DR}	V _{CC} for Data Retention	V _{CC} = V _{DR} = 2.0 V, CE ≥ V _{CC} - 0.3 V, V _{IN} ≥ V _{CC} - 0.3 V or V _{IN} ≤ 0.3 V	2.0	—	V
I _{CCDR}	Data Retention Current L		—	10	μA
t _{CDR} ^[3]	Chip Deselect to Data Retention Time		0	—	ns
t _R ^[4]	Operation Recovery Time		200	—	μs

Data Retention Waveform



Notes

- Tested initially and after any design or process changes that may affect these parameters.
- t_R ≤ 3 ns for -15 speed.
- No input may exceed V_{CC} + 0.5 V.

Switching Characteristics

Over the Operating Range^[6]

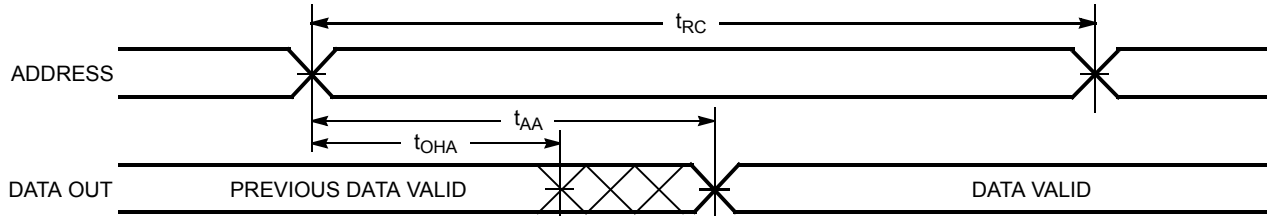
Parameter	Description	7C199-15		Unit
		Min	Max	
Read Cycle				
t _{RC}	Read Cycle Time	15	–	ns
t _{AA}	Address to Data Valid	–	15	ns
t _{OHA}	Data Hold from Address Change	3	–	ns
t _{ACE}	CE LOW to Data Valid	–	15	ns
t _{DOE}	OE LOW to Data Valid	–	7	ns
t _{LZOE}	OE LOW to Low Z ^[7]	0	–	ns
t _{HZOE}	OE HIGH to High Z ^[7, 8]	–	7	ns
t _{LZCE}	CE LOW to Low Z ^[7]	3	–	ns
t _{HZCE}	CE HIGH to High Z ^[7, 8]	–	7	ns
t _{PU}	CE LOW to Power-up	0	–	ns
t _{PD}	CE HIGH to Power-down	–	15	ns
Write Cycle ^[9, 10]				
t _{WC}	Write Cycle Time	15	–	ns
t _{SCE}	CE LOW to Write End	10	–	ns
t _{AW}	Address Set-up to Write End	10	–	ns
t _{HA}	Address Hold from Write End	0	–	ns
t _{SA}	Address Set-up to Write Start	0	–	ns
t _{PWE}	WE Pulse Width	9	–	ns
t _{SD}	Data Set-up to Write End	9	–	ns
t _{HD}	Data Hold from Write End	0	–	ns
t _{HZWE}	WE LOW to High Z ^[8]	–	7	ns
t _{LZWE}	WE HIGH to Low Z ^[7]	3	–	ns

Notes

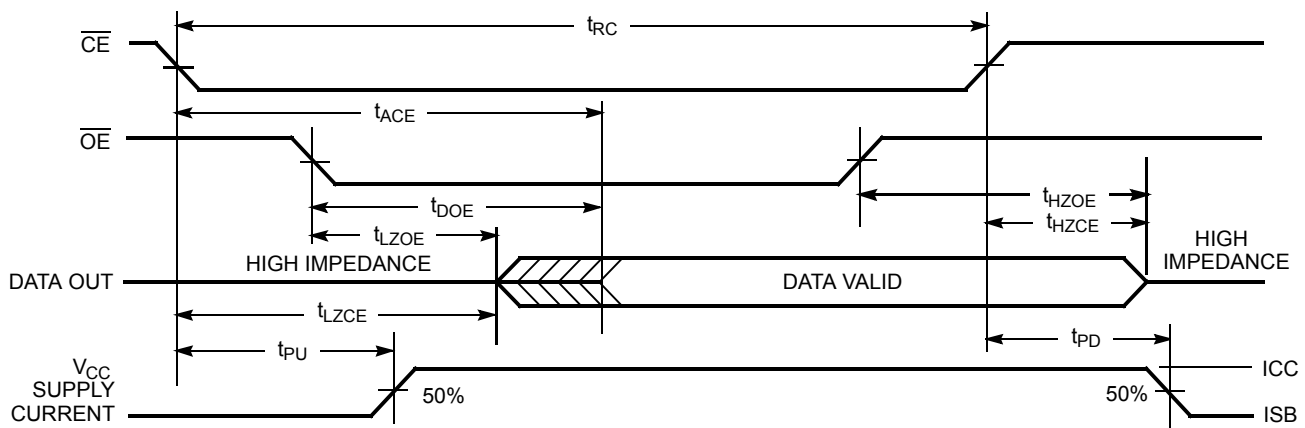
- Test conditions assume signal transition time of 3 ns or less for -15 speed, timing reference levels of 1.5 V, input pulse levels of 0 to 3.0 V, and output loading of the specified I_{OL}/I_{OH} and 30-pF load capacitance.
- At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE} , t_{HZOE} is less than t_{LZOE} , and t_{HZWE} is less than t_{LZWE} for any given device.
- t_{HZOE} , t_{HZCE} , and t_{HZWE} are specified with $C_L = 5$ pF as in part (b) of [AC Test Loads and Waveforms\[4\]](#) on page 5. Transition is measured ± 500 mV from steady-state voltage.
- The internal write time of the memory is defined by the overlap of $\overline{CE}$ LOW and $\overline{WE}$ LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.
- The minimum write cycle time for write cycle #3 ($\overline{WE}$ controlled, $\overline{OE}$ LOW) is the sum of t_{HZWE} and t_{SD} .

Switching Waveforms

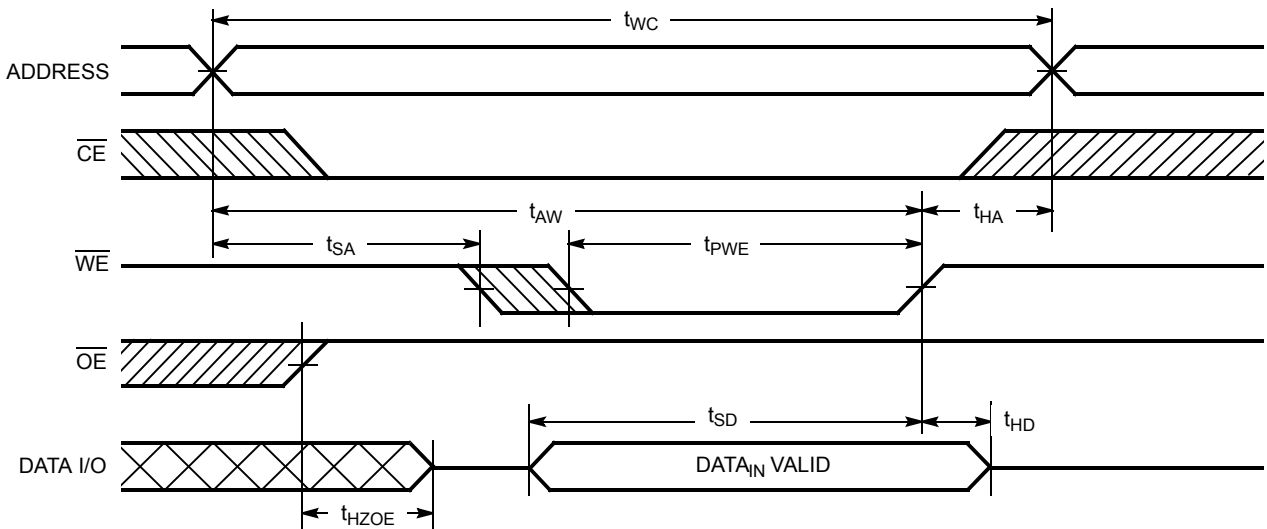
Read Cycle No. 1^[11, 12]



Read Cycle No. 2^[12, 13]



Write Cycle No. 1 ($\overline{WE}$ Controlled)^[14, 15, 16]

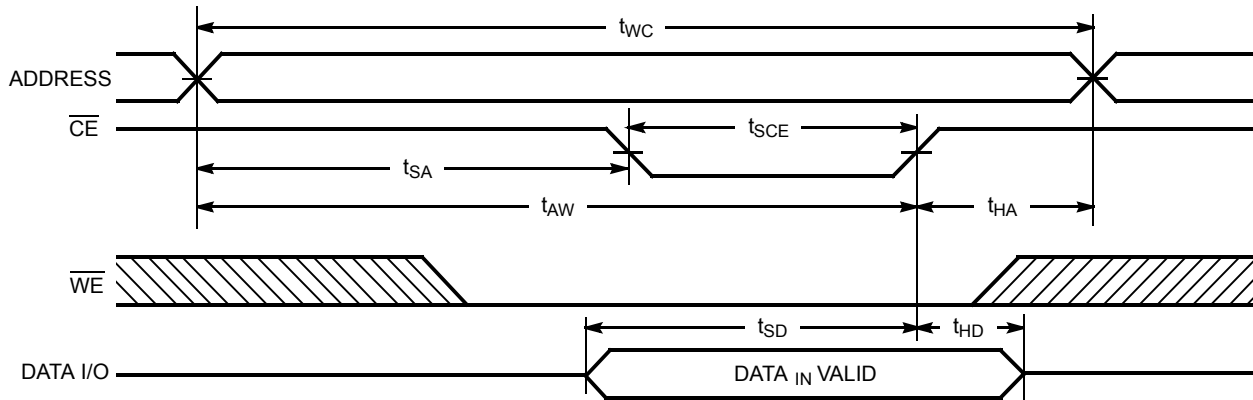


Notes

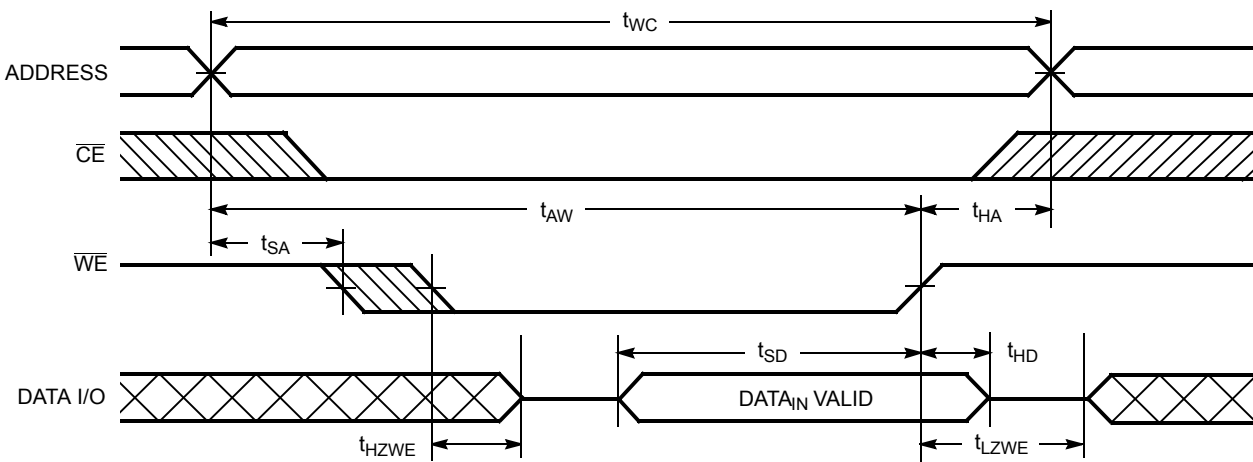
11. Device is continuously selected. $\overline{OE}$, $\overline{CE} = V_{IL}$.
12. $\overline{WE}$ is HIGH for read cycle.
13. Address valid prior to or coincident with $\overline{CE}$ transition LOW.
14. The internal write time of the memory is defined by the overlap of $\overline{CE}$ LOW and $\overline{WE}$ LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.
15. Data I/O is high impedance if $\overline{OE} = V_{IL}$.
16. If $\overline{CE}$ goes HIGH simultaneously with $\overline{WE}$ HIGH, the output remains in a high-impedance state.

Switching Waveforms (continued)

Write Cycle No. 2 ($\overline{\text{CE}}$ Controlled)^[17, 18, 19]



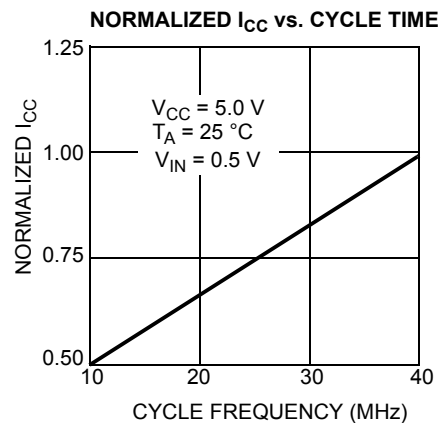
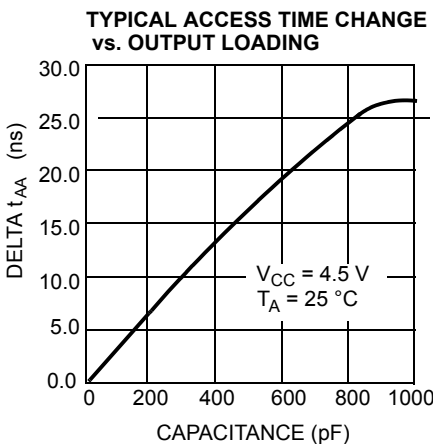
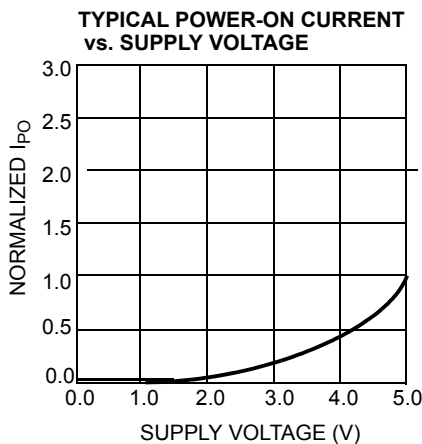
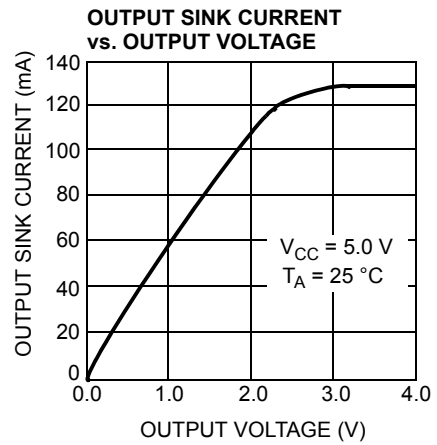
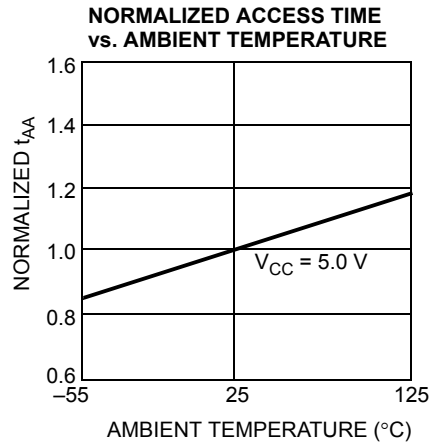
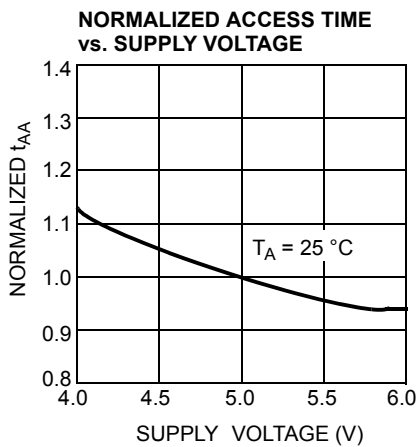
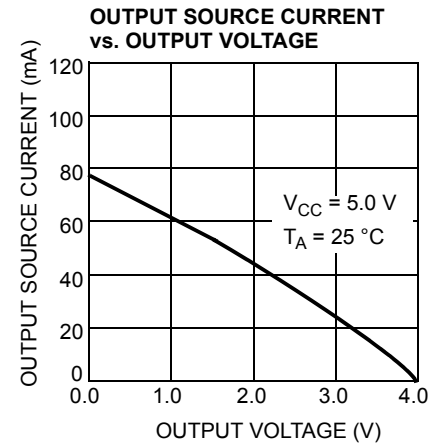
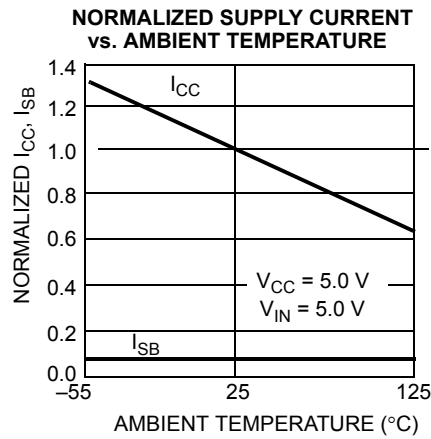
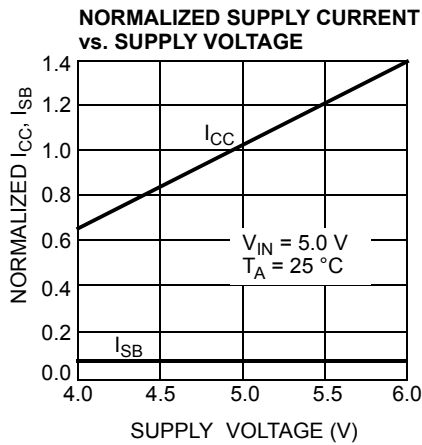
Write Cycle No. 3 ($\overline{\text{WE}}$ Controlled $\overline{\text{OE}}$ LOW)^[19, 20]



Notes

17. t_{HZOE} , t_{HZCE} , and t_{HZWE} are specified with $C_L = 5 \text{ pF}$ as in part (b) of [AC Test Loads and Waveforms\[4\]](#) on page 5. Transition is measured $\pm 500 \text{ mV}$ from steady-state voltage.
18. Data I/O is high impedance if $\overline{\text{OE}} = V_{IH}$.
19. If $\overline{\text{CE}}$ goes HIGH simultaneously with $\overline{\text{WE}}$ HIGH, the output remains in a high-impedance state.
20. The minimum write cycle time for write cycle #3 ($\overline{\text{WE}}$ controlled, $\overline{\text{OE}}$ LOW) is the sum of t_{HZWE} and t_{SD} .

Typical DC and AC Characteristics



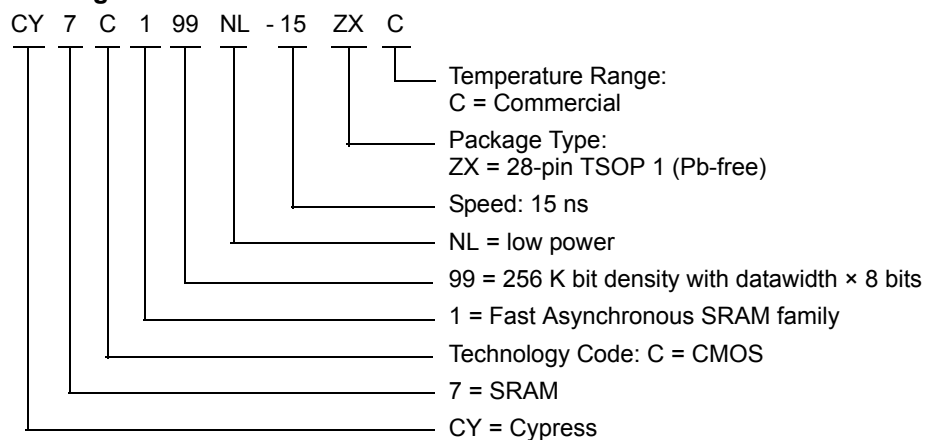
Truth Table

$\overline{CE}$	$\overline{WE}$	$\overline{OE}$	Inputs/Outputs	Mode	Power
H	X	X	High Z	Deselect/Power-down	Standby (I_{SB})
L	H	L	Data Out	Read	Active (I_{CC})
L	L	X	Data In	Write	Active (I_{CC})
L	H	H	High Z	Selected, Output disabled	Active (I_{CC})

Ordering Information

Speed (ns)	Ordering Code	Package Diagram	Package Type	Operating Range
15	CY7C199NL-15ZXC	51-85071	28-pin TSOP 1 (Pb-free)	Commercial

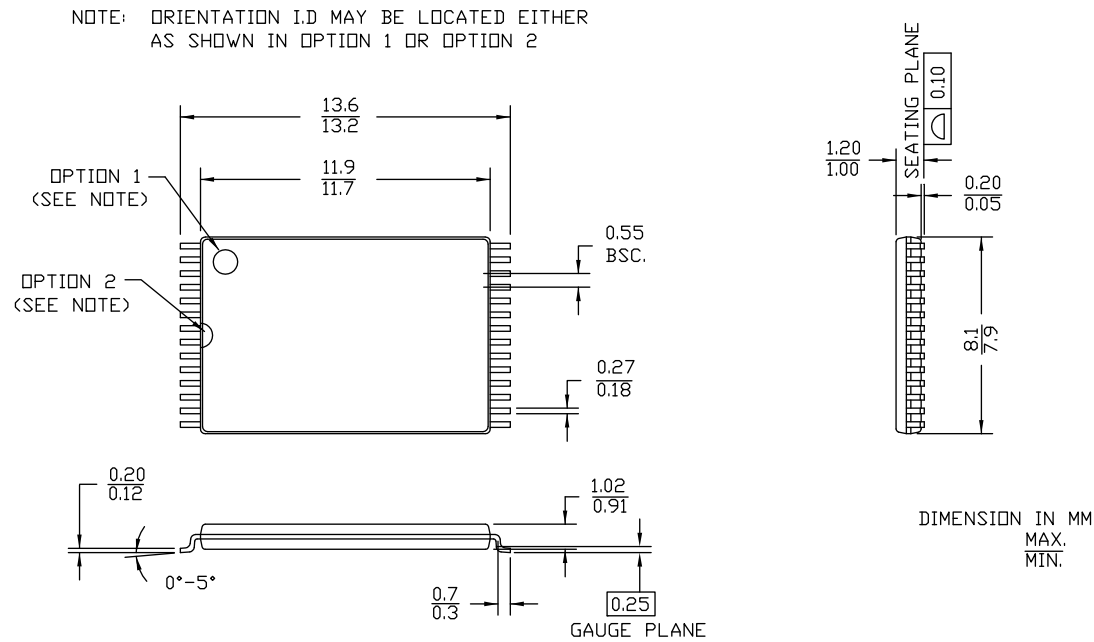
Ordering Code Definitions



Contact your Local Cypress sales representative for availability of these parts

Package Diagrams

Figure 1. 28-pin TSOP 1 (8 × 13.4 × 1.2 mm), 51-85071



51-85071 *I

Acronyms

Acronym	Description
CE	Chip Enable
CMOS	complementary metal-oxide semiconductor
I/O	input/output
OE	Output Enable
SOJ	small outline J-lead
SRAM	static random access memory
TTL	transistor-transistor logic
TSOP	thin small outline package
WE	Write Enable

Document Conventions

Units of Measure

Symbol	Unit of Measure
°C	degree Celsius
μA	micro Amperes
μs	micro seconds
MHz	Mega Hertz
mA	milli Amperes
ns	nano seconds
Ω	ohms
pF	pico Farad
V	Volts
mW	milli Watts
W	Watts
%	percent

Document History Page

Document Title: CY7C199N 32 K × 8 Static RAM Document Number: 001-06493				
REV.	ECN NO.	Issue Date	Orig. of Change	Description of Change
**	423877	See ECN	NXR	New Data Sheet
*A	2892510	03/18/2010	VKN	Removed speed bins from the data sheet: 12ns, 20ns, 25ns, 35ns, and 55ns. Removed Industrial and Military product information Removed 28-pin (300-Mil) PDIP package Updated Ordering Information table Updated Package Diagram
*B	3109199	12/13/2010	AJU	Added Ordering Code Definitions .
*C	3244591	04/29/2011	PRAS	Updated Package Diagrams . Added Acronyms and Units of Measure . Updated in new template.

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