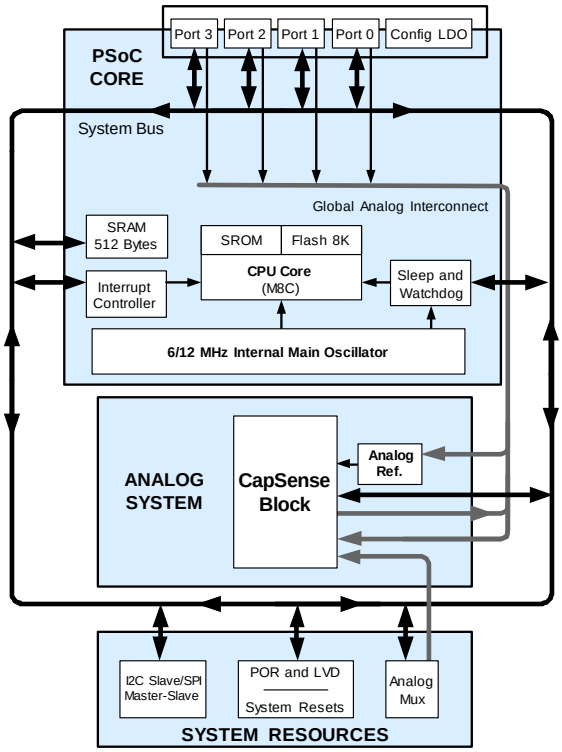
CY8C20134, CY8C20234, CY8C20334
CY8C20434, CY8C20534, CY8C20634

PSoC® Programmable System-on-Chip™

Features

- Low power CapSense® block
  - Configurable capacitive sensing elements
  - Supports combination of CapSense buttons, sliders, touchpads, and proximity sensors
- Powerful Harvard-architecture processor
  - M8C processor speeds running up to 12 MHz
  - Low power at high speed
  - Operating voltage: 2.4 V to 5.25 V
  - Industrial temperature range: –40 °C to +85 °C
- Flexible on-chip memory
  - 8 KB flash program storage 50,000 erase/write cycles
  - 512-Bytes SRAM data storage
  - Partial flash updates
  - Flexible protection modes
  - Interrupt controller
  - In-system serial programming (ISSP)
- Complete development tools
  - Free development tool (PSoC Designer™)
  - Full-featured, in-circuit emulator, and programmer
  - Full-speed emulation
  - Complex breakpoint structure
  - 128 KB trace memory
- Precision, programmable clocking
  - Internal ±5.0% 6- / 12-MHz main oscillator
  - Internal low speed oscillator at 32 kHz for watchdog and sleep
- Programmable pin configurations
  - Pull-up, high Z, open-drain, and CMOS drive modes on all GPIOs
  - Up to 28 analog inputs on all GPIOs
  - Configurable inputs on all GPIOs
  - 20-mA sink current on all GPIOs
  - Selectable, regulated digital I/O on port 1
    - 3.0 V, 20 mA total port 1 source current
    - 5 mA strong drive mode on port 1 versatile analog mux
  - Common internal analog bus
  - Simultaneous connection of I/O combinations
  - Comparator noise immunity
  - Low-dropout voltage regulator for the analog array
- Additional system resources
  - Configurable communication speeds
    - I^2C: selectable to 50 kHz, 100 kHz, or 400 kHz
    - SPI: configurable between 46.9 kHz and 3 MHz
  - I^2C slave
  - SPI master and SPI slave
  - Watchdog and sleep timers
  - Internal voltage reference
  - Integrated supervisory circuit

Logic Block Diagram



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PSoC Functional Overview

The PSoC family consists of many *Programmable System-on-Chips with On-Chip Controller* devices. These devices are designed to replace multiple traditional MCU based system components with one low cost single chip programmable component. A PSoC device includes configurable analog and digital blocks and programmable interconnect. This architecture enables the user to create customized peripheral configurations to match the requirements of each individual application. Additionally, a fast CPU, flash program memory, SRAM data memory, and configurable I/O are included in a range of convenient pinouts.

The PSoC architecture for this device family, as shown in Figure 1, consists of three main areas: the Core, the System Resources, and the CapSense Analog System. A common versatile bus enables connection between I/O and the analog system. Each CY8C20x34 PSoC device includes a dedicated CapSense block that provides sensing and scanning control circuitry for capacitive sensing applications. Depending on the PSoC package, up to 28 general purpose I/O (GPIO) are also included. The GPIO provide access to the MCU and analog mux.

PSoC Core

The PSoC Core is a powerful engine that supports a rich instruction set. It encompasses SRAM for data storage, an interrupt controller, sleep and watchdog timers, IMO , and ILO. The CPU core, called the M8C, is a powerful processor with speeds up to 12 MHz. The M8C is a two MIPS, 8-bit Harvard-architecture microprocessor.

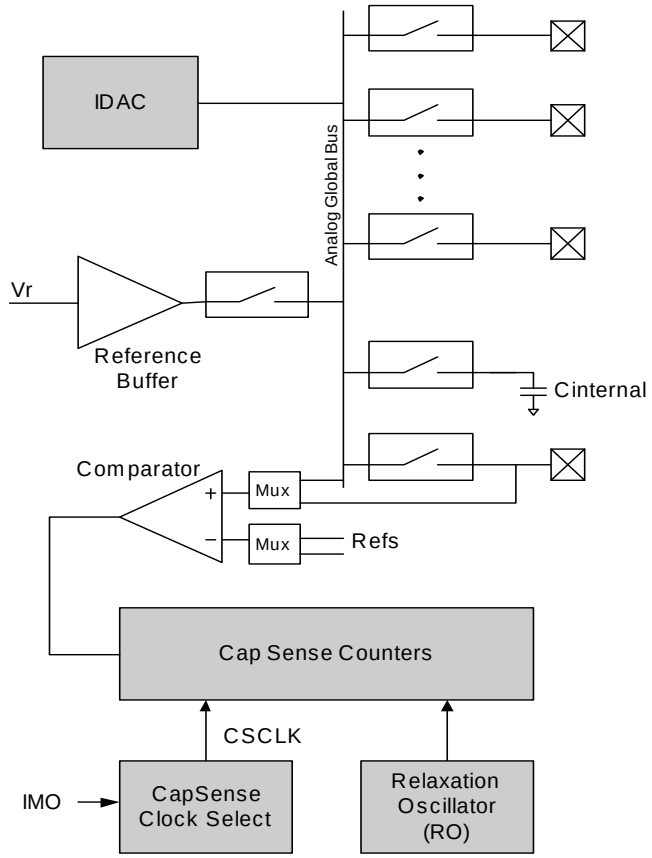
System Resources provide additional capability such as a configurable I^2C slave or SPI master-slave communication interface and various system resets supported by the M8C.

The Analog System consists of the CapSense PSoC block and an internal 1.8 V analog reference. Together they support capacitive sensing of up to 28 inputs.

CapSense Analog System

The Analog System contains the capacitive sensing hardware. Several hardware algorithms are supported. This hardware performs capacitive sensing and scanning without requiring external components. Capacitive sensing is configurable on each GPIO pin. Scanning of enabled CapSense pins is completed quickly and easily across multiple ports.

Figure 1. Analog System Block Diagram



Analog Multiplexer System

The Analog Mux Bus connects to every GPIO pin. Pins are connected to the bus individually or in any combination. The bus also connects to the analog system for analysis with the CapSense block comparator.

Switch control logic enables selected pins to precharge continuously under hardware control. This enables capacitive measurement for applications such as touch sensing. Other multiplexer applications include:

- Complex capacitive sensing interfaces such as sliders and touch pads
- Chip-wide mux that enables analog input from any I/O pin
- Crosspoint connection between any I/O pin combinations

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Additional System Resources

System Resources provide additional capability useful to complete systems. Additional resources include low voltage detection and power on reset. Brief statements describing the merits of each system resource follow:

- The I^2C slave or SPI master-slave module provides 50/100/400 kHz communication over two wires. SPI communication over three or four wires run at speeds of 46.9 kHz to 3 MHz (lower for a slower system clock).
- Low voltage detection (LVD) interrupts signal the application of falling voltage levels, while the advanced POR (Power On Reset) circuit eliminates the need for a system supervisor.
- An internal 1.8 V reference provides an absolute reference for capacitive sensing.
- The 5 V maximum input, 3 V fixed output, low dropout regulator (LDO) provides regulation for I/Os. A register controlled bypass mode enables the user to disable the LDO.

PSoC Device Characteristics

Depending on your PSoC device characteristics, the digital and analog systems can have 16, 8, or 4 digital blocks, and 12, 6, or 4 analog blocks. Table 1 lists the resources available for specific PSoC device groups. The PSoC device covered by this datasheet is highlighted.

Table 1. PSoC Device Characteristics

PSoC Part Number	Digital I/O	Digital Rows	Digital Blocks	Analog Inputs	Analog Outputs	Analog Columns	Analog Blocks	SRAM Size	Flash Size
CY8C29x66	up to 64	4	16	up to 12	4	4	12	2 K	32 K
CY8C28xxx	up to 44	up to 3	up to 12	up to 44	up to 4	up to 6	up to 12 + 4[1]	1 K	16 K
CY8C27x43	up to 44	2	8	up to 12	4	4	12	256	16 K
CY8C24x94	up to 56	1	4	up to 48	2	2	6	1 K	16 K
CY8C24x23A	up to 24	1	4	up to 12	2	2	6	256	4 K
CY8C23x33	up to 26	1	4	up to 12	2	2	4	256	8 K
CY8C22x45	up to 38	2	8	up to 38	0	4	6[1]	1 K	16 K
CY8C21x45	up to 24	1	4	up to 24	0	4	6[1]	512	8 K
CY8C21x34	up to 28	1	4	up to 28	0	2	4[1]	512	8 K
CY8C21x23	up to 16	1	4	up to 8	0	2	4[1]	256	4 K
CY8C20x34	up to 28	0	0	up to 28	0	0	3[1,2]	512	8 K
CY8C20xx6	up to 36	0	0	up to 36	0	0	3[1,2]	up to 2 K	up to 32 K

Notes
1. Limited analog functionality
2. Two analog blocks and one CapSense®.

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Getting Started

For in-depth information, along with detailed programming details, see the *PSoC® Technical Reference Manual*.

For up-to-date ordering, packaging, and electrical specification information, see the latest PSoC device datasheets on the web.

Application Notes

Cypress application notes are an excellent introduction to the wide variety of possible PSoC designs.

Development Kits

PSoC Development Kits are available online from and through a growing number of regional and global distributors, which include Arrow, Avnet, Digi-Key, Farnell, Future Electronics, and Newark.

Training

Free PSoC technical training (on demand, webinars, and workshops), which is available online via www.cypress.com, covers a wide variety of topics and skill levels to assist you in your designs.

CYPros Consultants

Certified PSoC consultants offer everything from technical assistance to completed PSoC designs. To contact or become a PSoC consultant go to the CYPros Consultants web site.

Solutions Library

Visit our growing library of solution focused designs. Here you can find various application designs that include firmware and hardware design files that enable you to complete your designs quickly.

Technical Support

Technical support – including a searchable Knowledge Base articles and technical forums – is also available online. If you cannot find an answer to your question, call our Technical Support hotline at 1-800-541-4736.

Development Tools

PSoC Designer™ is the revolutionary integrated design environment (IDE) that you can use to customize PSoC to meet your specific application requirements. PSoC Designer software accelerates system design and time to market. Develop your applications using a library of precharacterized analog and digital peripherals (called user modules) in a drag-and-drop design environment. Then, customize your design by leveraging the dynamically generated application programming interface (API) libraries of code. Finally, debug and test your designs with the integrated debug environment, including in-circuit emulation and standard software debug features. PSoC Designer includes:

- Application editor graphical user interface (GUI) for device and user module configuration and dynamic reconfiguration
- Extensive user module catalog
- Integrated source-code editor (C and assembly)
- Free C compiler with no size restrictions or time limits
- Built-in debugger
- In-circuit emulation
- Built-in support for communication interfaces:
  - Hardware and software I^2C slaves and masters
  - Full-speed USB 2.0
  - Up to four full-duplex universal asynchronous receiver/transmitters (UARTs), SPI master and slave, and wireless

PSoC Designer supports the entire library of PSoC 1 devices and runs on Windows XP, Windows Vista, and Windows 7.

PSoC Designer Software Subsystems

Design Entry

In the chip-level view, choose a base device to work with. Then select different onboard analog and digital components that use the PSoC blocks, which are called user modules. Examples of user modules are ADCs, DACs, amplifiers, and filters. Configure the user modules for your chosen application and connect them to each other and to the proper pins. Then generate your project. This prepopulates your project with APIs and libraries that you can use to program your application.

The tool also supports easy development of multiple configurations and dynamic reconfiguration. Dynamic reconfiguration makes it possible to change configurations at run time. In essence, this allows you to use more than 100 percent of PSoC's resources for an application.

Code Generation Tools

The code generation tools work seamlessly within the PSoC Designer interface and have been tested with a full range of debugging tools. You can develop your design in C, assembly, or a combination of the two.

Assemblers. The assemblers allow you to merge assembly code seamlessly with C code. Link libraries automatically use absolute addressing or are compiled in relative mode, and are linked with other software modules to get absolute addressing.

C Language Compilers. C language compilers are available that support the PSoC family of devices. The products allow you to create complete C programs for the PSoC family devices. The optimizing C compilers provide all of the features of C, tailored to the PSoC architecture. They come complete with embedded libraries providing port and bus operations, standard keypad and display support, and extended math functionality.

Debugger

PSoC Designer has a debug environment that provides hardware in-circuit emulation, allowing you to test the program in a physical system while providing an internal view of the PSoC device. Debugger commands allow you to read and program and read and write data memory, and read and write I/O registers. You can read and write CPU registers, set and clear breakpoints, and provide program run, halt, and step control. The debugger

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also allows you to create a trace buffer of registers and memory locations of interest.

Online Help System

The online help system displays online, context-sensitive help. Designed for procedural and quick reference, each functional subsystem has its own context-sensitive help. This system also provides tutorials and links to FAQs and an online support Forum to aid the designer.

In-Circuit Emulator

A low-cost, high-functionality in-circuit emulator (ICE) is available for development support. This hardware can program single devices.

The emulator consists of a base unit that connects to the PC using a USB port. The base unit is universal and operates with all PSoC devices. Emulation pods for each device family are available separately. The emulation pod takes the place of the PSoC device in the target board and performs full-speed (24 MHz) operation.

Designing with PSoC Designer

The development process for the PSoC device differs from that of a traditional fixed function microprocessor. The configurable analog and digital hardware blocks give the PSoC architecture a unique flexibility that pays dividends in managing specification change during development and by lowering inventory costs. These configurable resources, called PSoC Blocks, have the ability to implement a wide variety of user-selectable functions. The PSoC development process is summarized in four steps:

1. Select User Modules.
2. Configure User Modules.
3. Organize and Connect.
4. Generate, Verify, and Debug.

Select User Modules

PSoC Designer provides a library of prebuilt, pretested hardware peripheral components called “user modules.” User modules make selecting and implementing peripheral devices, both analog and digital, simple.

Configure User Modules

Each user module that you select establishes the basic register settings that implement the selected function. They also provide parameters and properties that allow you to tailor their precise configuration to your particular application. For example, a PWM User Module configures one or more digital PSoC blocks, one for each 8 bits of resolution. The user module parameters permit you to establish the pulse width and duty cycle. Configure the parameters and properties to correspond to your chosen application. Enter values directly or by selecting values from drop-down menus. All the user modules are documented in datasheets that may be viewed directly in PSoC Designer or on the Cypress website. These user module datasheets explain the internal operation of the user module and provide performance specifications. Each datasheet describes the use of each user module parameter, and other information you may need to successfully implement your design.

Organize and Connect

You build signal chains at the chip level by interconnecting user modules to each other and the I/O pins. You perform the selection, configuration, and routing so that you have complete control over all on-chip resources.

Generate, Verify, and Debug

When you are ready to test the hardware configuration or move on to developing code for the project, you perform the “Generate Configuration Files” step. This causes PSoC Designer to generate source code that automatically configures the device to your specification and provides the software for the system. The generated code provides application programming interfaces (APIs) with high-level functions to control and respond to hardware events at run-time and interrupt service routines that you can adapt as needed.

A complete code development environment allows you to develop and customize your applications in either C, assembly language, or both.

The last step in the development process takes place inside PSoC Designer’s debugger (access by clicking the Connect icon). PSoC Designer downloads the HEX image to the ICE where it runs at full speed. PSoC Designer debugging capabilities rival those of systems costing many times more. In addition to traditional single-step, run-to-breakpoint, and watch-variable features, the debug interface provides a large trace buffer and allows you to define complex breakpoint events. These include monitoring address and data bus values, memory locations, and external signals.

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Pin Information

This section describes, lists, and illustrates the CY8C20234, CY8C20334, CY8C20434, CY8C20534, and CY8C20634 PSoC device pins and pinout configurations.

The CY8C20x34 PSoC device is available in a variety of packages that are listed and shown in the following tables. Every port pin (labeled with a “P”) is capable of Digital I/O and connection to the common analog bus. However, V_{SS}, V_{DD}, and XRES are not capable of Digital I/O.

8-Pin SOIC Pinout

Figure 2. CY8C20134-12SXI 8-Pin SOIC Pinout

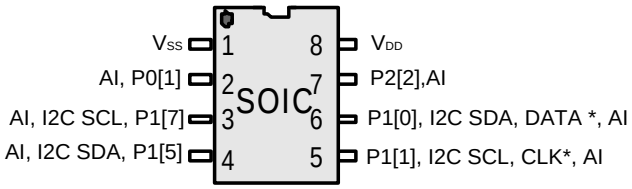

Table 2. Pin Definitions – CY8C20134 8-Pin (SOIC)

Pin No.	Digital	Analog	Name	Description
1	Power		V_{SS}	Ground connection
2	I/O	I	P0[1]	Analog column mux input, integrating input
3	I/O	I	P1[7]	I2C serial clock (SCL)
4	I/O	I	P1[5]	I2C serial data (SDA)
5	I/O	I	P1[1]	I2C serial clock (SCL), ISSP-SCLK
6	I/O	I	P1[0]	I2C serial data (SDA), ISSP-SDATA
7	I/O	I	P2[2]	Analog column mux input
8	Power		V_{DD}	Supply voltage

A = Analog, I = Input, O = Output, OH = 5 mA High Output Drive.

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16-Pin SOIC Pinout

Figure 3. CY8C20234-12SXI 16-Pin SOIC Pinout

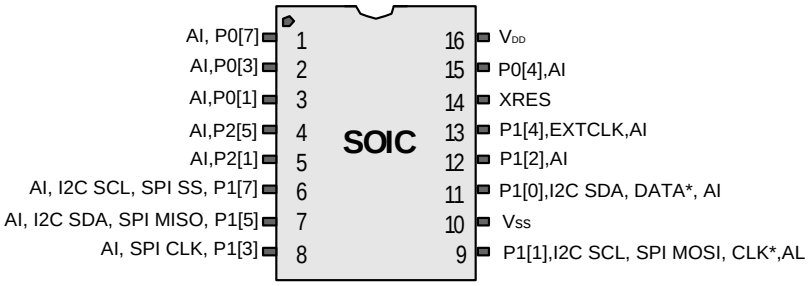

Table 3. Pin Definitions – CY8C20234 16-Pin (SOIC)

Pin No.	Digital	Analog	Name	Description
1	I/O	I	P0[7]	Analog column mux input
2	I/O	I	P0[3]	Analog column mux input and column input, integrating input
3	I/O	I	P0[1]	Analog column mux input, integrating input
4	I/O	I	P2[5]	Analog column mux input
5	I/O	I	P2[1]	Analog column mux input
6	I/O	I	P1[7]	I2C serial clock (SCL), SPI SS
7	I/O	I	P1[5]	I2C serial data (SDA),SPI MISO
8	I/O	I	P1[3]	Analog column mux input, SPI CLK
9	I/O	I	P1[1]	I2C serial clock (SCL), ISSP-SCLK,SPI MOSI
10	Power		V_{SS}	Ground connection
11	I/O	I	P1[0]	I2C serial data (SDA), ISSP-SDATA
12	I/O	I	P1[2]	Analog column mux input
13	I/O	I	P1[4]	Analog column mux input, optional external clock input (EXTCLK)
14	I/O	I	XRES	XRES
15	I/O	I	P0[4]	Analog column mux input
16	Power		V_{DD}	Supply voltage

A = Analog, I = Input, O = Output, OH = 5 mA High Output Drive.

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48-Pin OCD Part Pinout

The 48-Pin QFN part table and pin diagram is for the CY8C20000 On-Chip Debug (OCD) PSoC device. This part is only used for in-circuit debugging. It is NOT available for production.

Figure 4. CY8C20000 48-Pin OCD PSoC Device

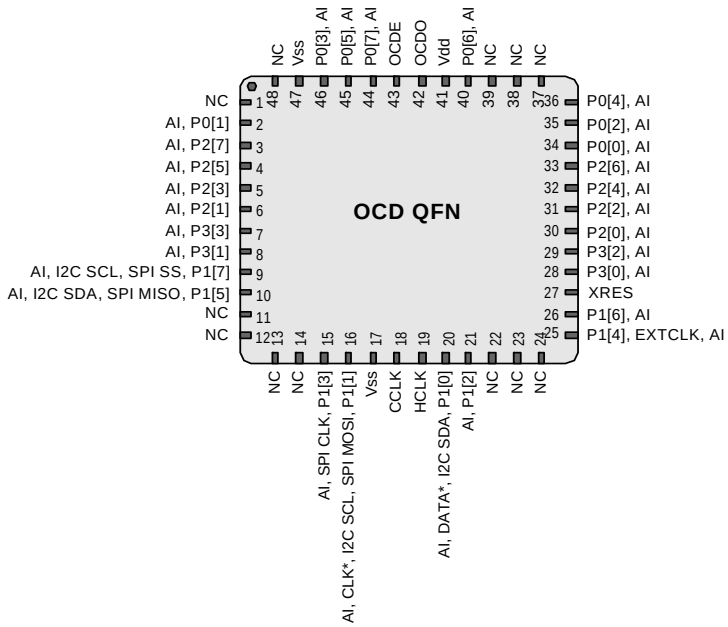

Table 4. Pin Definitions – CY8C20000 48-Pin OCD (QFN) [3]

Pin No.	Digital	Analog	Name	Description
1			NC	No connection
2	I/O	I	P0[1]	
3	I/O	I	P2[7]	
4	I/O	I	P2[5]	
5	I/O	I	P2[3]	
6	I/O	I	P2[1]	
7	I/O	I	P3[3]	
8	I/O	I	P3[1]	
9	I_{OH}	I	P1[7]	I^2C SCL, SPI SS
10	I_{OH}	I	P1[5]	I^2C SDA, SPI MISO
11	I/O	I	P0[1]	
12			NC	No connection
13			NC	No Connection
14			NC	No Connection
15			NC	SPI CLK
16	I_{OH}	I	P1[3]	CLK[4], I^2C SCL, SPI MOSI
17	I_{OH}	I	P1[1]	Ground connection
18	Power		V_{SS}	OCD CPU clock output

Notes
3. The center pad on the QFN package is connected to ground (V_{SS}) for best mechanical, thermal, and electrical performance. If not connected to ground, it is electrically floated and not connected to any other signal.
4. These are the ISSP pins, that are not High Z at POR (Power-on-Reset). See the *PSoC Technical Reference Manual* for details.

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Table 4. Pin Definitions – CY8C20000 48-Pin OCD (QFN) [3]

Pin No.	Digital	Analog	Name	Description
19			CCLK	OCD high speed clock output
20			HCLK	DATA[5], I^2C SDA
21	I_{OH}	I	P1[0]	
22	I_{OH}	I	P1[2]	No connection
23			NC	No connection
24			NC	No connection
25			NC	Optional external clock input (EXTCLK)
26	I_{OH}	I	P1[4]	
27	I_{OH}	I	P1[6]	Active high external reset with internal pull-down
28	Input		XRES	
29	I/O	I	P3[0]	
30	I/O	I	P3[2]	
31	I/O	I	P2[0]	
32	I/O	I	P2[2]	
33	I/O	I	P2[4]	
34	I/O	I	P2[6]	
35	I/O	I	P0[0]	
36	I/O	I	P0[2]	
37			NC	No connection
38			NC	No connection
39			NC	No connection
40	I/O	I	P0[6]	Analog bypass
41	Power		V_{DD}	Supply voltage
42			OCDO	OCD odd data output
43			OCDE	OCD even data I/O
44	I/O	I	P0[7]	
45	I/O	I	P0[5]	
46	I/O	I	P0[3]	Integrating Input
47	Power		V_{SS}	Ground connection
48			NC	No connection
CP	Power		V_{SS}	Center pad is connected to ground

A = Analog, I = Input, O = Output, NC = No Connection H = 5 mA High Output Drive.

Note

5. These are the ISSP pins, that are not High Z at POR (Power-on-Reset). See the *PSoC Technical Reference Manual* for details.

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16-Pin Part Pinout

Figure 5. CY8C20234 16-Pin PSoC Device

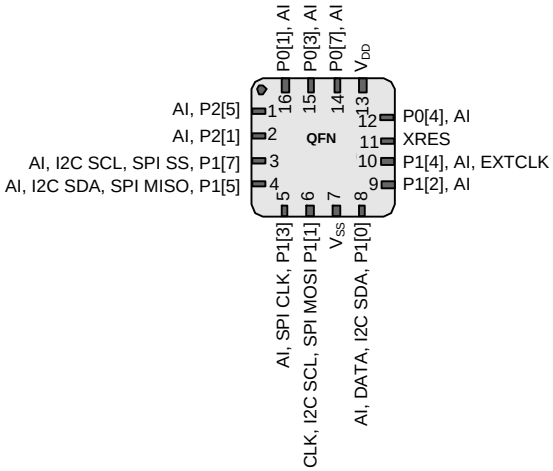

Table 5. Pin Definitions – CY8C20234 16-Pin (QFN no e-pad)

Pin No.	Type		Name	Description
	Digital	Analog		
1	I/O	I	P2[5]	
2	I/O	I	P2[1]	
3	I_{OH}	I	P1[7]	I^2C SCL, SPI SS
4	I_{OH}	I	P1[5]	I^2C SDA, SPI MISO
5	I_{OH}	I	P1[3]	SPI CLK
6	I_{OH}	I	P1[1]	CLK[6], I^2C SCL, SPI MOSI
7	Power		V_{SS}	Ground connection
8	I_{OH}	I	P1[0]	DATA[6], I^2C SDA
9	I_{OH}	I	P1[2]	
10	I_{OH}	I	P1[4]	Optional external clock input (EXTCLK)
11	Input		XRES	Active high external reset with internal pull-down
12	I/O	I	P0[4]	
13	Power		V_{DD}	Supply voltage
14	I/O	I	P0[7]	
15	I/O	I	P0[3]	Integrating Input
16	I/O	I	P0[1]	

A = Analog, I = Input, O = Output, OH = 5 mA High Output Drive

Note
6. These are the ISSP pins, that are not High Z at POR (Power-on-Reset). See the *PSoC Technical Reference Manual* for details.

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24-Pin Part Pinout

Figure 6. CY8C20334 24-Pin PSoC Device

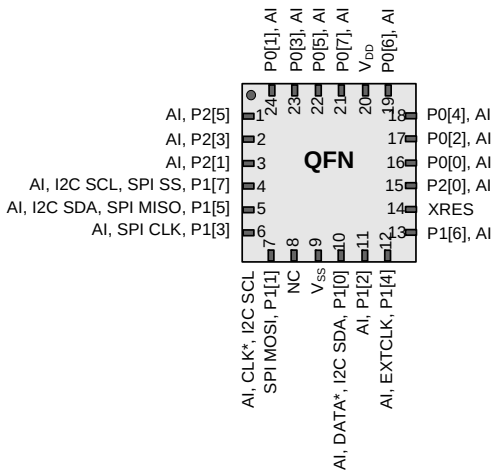


Table 6. Pin Definitions – CY8C20334 24-Pin (QFN) [7]

Pin No.	Type		Name	Description
	Digital	Analog		
1	I/O	I	P2[5]	
2	I/O	I	P2[3]	
3	I/O	I	P2[1]	
4	I_{OH}	I	P1[7]	I^2C SCL, SPI SS
5	I_{OH}	I	P1[5]	I^2C SDA, SPI MISO
6	I_{OH}	I	P1[3]	SPI CLK
7	I_{OH}	I	P1[1]	CLK[8], I^2C SCL, SPI MOSI
8			NC	No Connection
9	Power		V_{SS}	Ground Connection
10	I_{OH}	I	P1[0]	DATA[8], I^2C SDA
11	I_{OH}	I	P1[2]	
12	I_{OH}	I	P1[4]	Optional external clock input (EXTCLK)
13	I_{OH}	I	P1[6]	
14	Input		XRES	Active high external reset with internal pull-down
15	I/O	I	P2[0]	
16	I/O	I	P0[0]	
17	I/O	I	P0[2]	
18	I/O	I	P0[4]	
19	I/O	I	P0[6]	Analog bypass
20	Power		V_{DD}	Supply voltage
21	I/O	I	P0[7]	
22	I/O	I	P0[5]	
23	I/O	I	P0[3]	Integrating input
24	I/O	I	P0[1]	
CP	Power		V_{SS}	Center pad is connected to ground

A = Analog, I = Input, O = Output, OH = 5 mA High Output Drive

Notes

7. The center pad on the QFN package is connected to ground (V_{SS}) for best mechanical, thermal, and electrical performance. If not connected to ground, it is electrically floated and not connected to any other signal.
8. These are the ISSP pins, that are not High Z at POR (Power-on-Reset). See the *PSoC Technical Reference Manual* for details.

[+] Feedback

32-Pin Part Pinout

Figure 7. CY8C20434 32-Pin PSoC Device

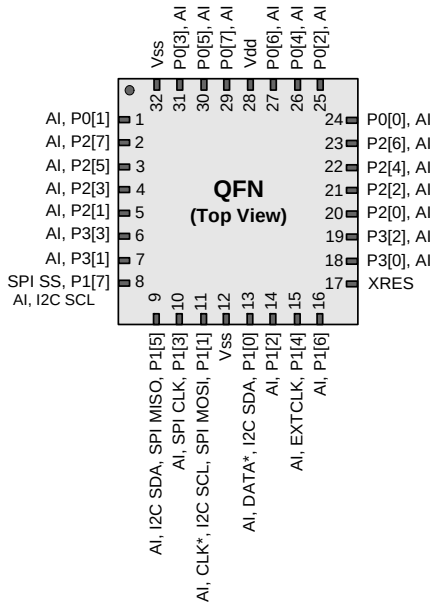


Table 7. Pin Definitions – CY8C20434 32-Pin (QFN) [9]

Pin No.	Type		Name	Description
	Digital	Analog		
1	I/O	I	P0[1]	
2	I/O	I	P2[7]	
3	I/O	I	P2[5]	
4	I/O	I	P2[3]	
5	I/O	I	P2[1]	
6	I/O	I	P3[3]	
7	I/O	I	P3[1]	
8	I_{OH}	I	P1[7]	I^2C SCL, SPI SS
9	I_{OH}	I	P1[5]	I^2C SDA, SPI MISO
10	I_{OH}	I	P1[3]	SPI CLK
11	I_{OH}	I	P1[1]	CLK[10], I^2C SCL, SPI MOSI
12	Power		V_{SS}	Ground Connection
13	I_{OH}	I	P1[0]	DATA[10], I^2C SDA
14	I_{OH}	I	P1[2]	
15	I_{OH}	I	P1[4]	Optional external clock input (EXTCLK)
16	I_{OH}	I	P1[6]	
17	Input		XRES	Active high external reset with internal pull-down
18	I/O	I	P3[0]	
19	I/O	I	P3[2]	

Notes

9. The center pad on the QFN package is connected to ground (V_{SS}) for best mechanical, thermal, and electrical performance. If not connected to ground, it is electrically floated and not connected to any other signal.
10. These are the ISSP pins, that are not High Z at POR (Power-on-Reset). See the *PSoC Technical Reference Manual* for details.

[+] Feedback

Table 7. Pin Definitions – CY8C20434 32-Pin (QFN) [9]

Pin No.	Type		Name	Description
	Digital	Analog		
20	I/O	I	P2[0]	
21	I/O	I	P2[2]	
22	I/O	I	P2[4]	
23	I/O	I	P2[6]	
24	I/O	I	P0[0]	
25	I/O	I	P0[2]	
26	I/O	I	P0[4]	
27	I/O	I	P0[6]	Analog bypass
28	Power		V_{DD}	Supply voltage
29	I/O	I	P0[7]	
30	I/O	I	P0[5]	
31	I/O	I	P0[3]	Integrating input
32	Power		V_{SS}	Ground connection
CP	Power		V_{SS}	Center pad is connected to ground

A = Analog, I = Input, O = Output, OH = 5 mA high output drive.

[+] Feedback

28-Pin Part Pinout

Figure 8. CY8C20534 28-Pin PSoC Device

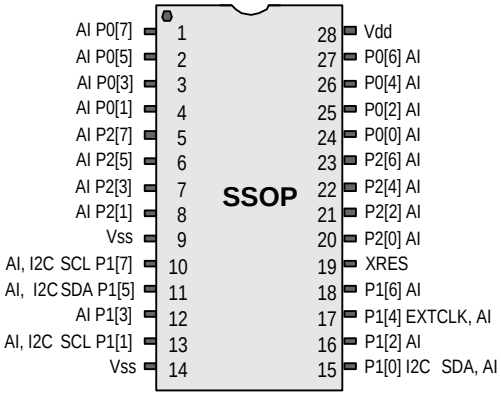


Table 8. Pin Definitions – CY8C20534 28-Pin (SSOP)

Pin No.	Type		Name	Description
	Digital	Analog		
1	I/O	I	P0[7]	Analog column mux input
2	I/O	I	P0[5]	Analog column mux input and column output
3	I/O	I	P0[3]	Analog column mux input and column output, integrating input
4	I/O	I	P0[1]	Analog column mux input, integrating input
5	I/O	I	P2[7]	
6	I/O	I	P2[5]	
7	I/O	I	P2[3]	Direct switched capacitor block input
8	I/O	I	P2[1]	Direct switched capacitor block input
9	Power		V_{SS}	Ground connection
10	I/O	I	P1[7]	I2C serial clock (SCL)
11	I/O	I	P1[5]	I2C serial data (SDA)
12	I/O	I	P1[3]	
13	I/O	I	P1[1]	I2C serial clock (SCL), ISSP-SCLK[11]
14	Power		V_{SS}	Ground connection
15	I/O	I	P1[0]	I2C serial data (SDA), ISSP-SDATA[11]
16	I/O	I	P1[2]	
17	I/O	I	P1[4]	Optional external clock input (EXTCLK)
18	I/O	I	P1[6]	
19	Input		XRES	Active high external reset with internal pull-down
20	I/O	I	P2[0]	Direct switched capacitor block input
21	I/O	I	P2[2]	Direct switched capacitor block input
22	I/O	I	P2[4]	
23	I/O	I	P2[6]	
24	I/O	I	P0[0]	Analog column mux input
25	I/O	I	P0[2]	Analog column mux input
26	I/O	I	P0[4]	Analog column mux input
27	I/O	I	P0[6]	Analog column mux input
28	Power		V_{DD}	Supply voltage

A = Analog, I = Input, O = Output, OH = 5 mA High Output Drive.

Note

11. These are the ISSP pins, that are not High Z at POR (Power-on-Reset). See the *PSoC Technical Reference Manual* for details.

[+] Feedback

30-Ball Part Pinout

Figure 9. CY8C20634 30-Ball PSoC Device

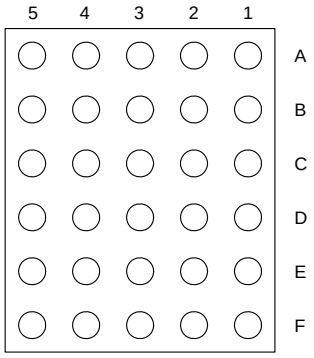


Table 9. 30-Ball Part Pinout (WLCSP)

Pin No.	Type		Name	Description
	Digital	Analog		
A1	Power		V_{DD}	Supply voltage
A2	I/O	I	P0[6]	Analog bypass
A3	I/O	I	P0[4]	
A4	I/O	I	P0[3]	Integrating input
A5	I/O	I	P2[7]	
B1	I/O	I	P0[2]	
B2	I/O	I	P0[0]	
B3	I/O	I	P2[6]	
B4	I/O	I	P0[5]	
B5	I/O	I	P0[1]	
C1	I/O	I	P2[4]	
C2	I/O	I	P2[2]	
C3	I/O	I	P3[1]	
C4	I/O	I	P0[7]	
C5	I/O	I	P2[1]	
D1	I/O	I	P2[0]	
D2	I/O	I	P3[0]	
D3	I/O	I	P3[2]	
D4	I_{OH}	I	P1[1]	CLK[12], I^2C SCL, SPI MOSI
D5	I/O	I	P2[3]	
E1	Input		XRES	Active high external reset with internal pull-down
E2	I_{OH}	I	P1[6]	
E3	I_{OH}	I	P1[4]	Optional external clock input (EXTCLK)
E4	I_{OH}	I	P1[5]	I^2C SDA, SPI MISO
E5	I/O	I	P2[5]	
F1	Power		V_{SS}	Ground connection
F2	I_{OH}	I	P1[2]	
F3	I_{OH}	I	P1[0]	DATA[12], I^2C SDA
F4	I_{OH}	I	P1[3]	SPI CLK
F5	I_{OH}	I	P1[7]	I^2C SCL, SPI SS

A = Analog, I = Input, O = Output, OH = 5 mA High Output Drive.

Note
12. These are the ISSP pins, that are not High Z at POR (Power-on-Reset). See the *PSoC Technical Reference Manual* for details.

[+] Feedback

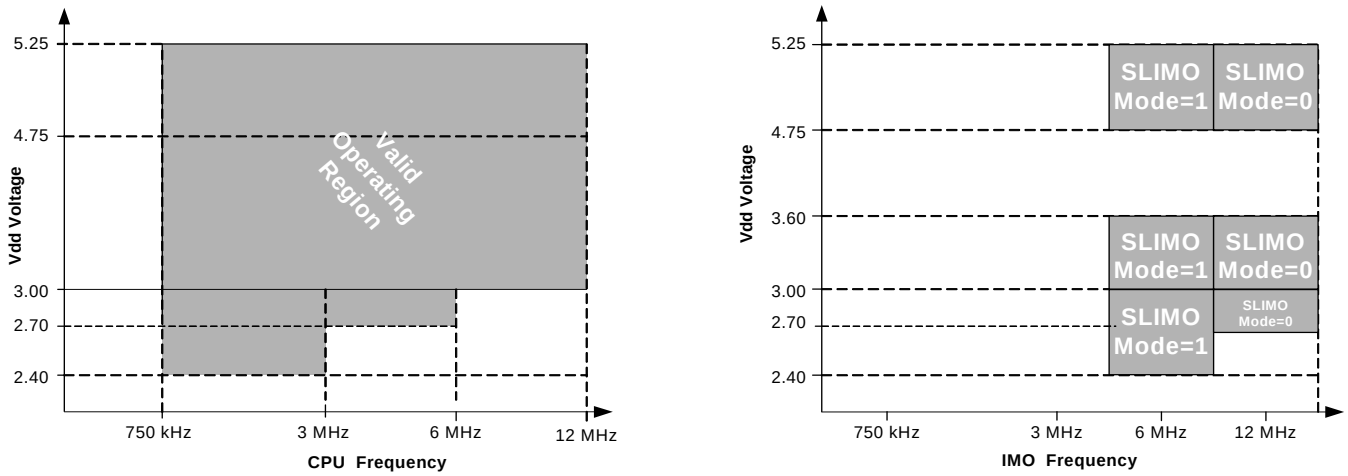
Electrical Specifications

This section presents the DC and AC electrical specifications of the CY8C20234, CY8C20334, CY8C20434, CY8C20534, and CY8C20634 PSoC devices. For the latest electrical specifications, check the most recent datasheet by visiting the web at http://www.cypress.com.

Specifications are valid for –40 °C ≤ T_A ≤ 85 °C and T_J ≤ 100 °C as specified, except where mentioned.

Refer to Table 19 on page 23 for the electrical specifications on the internal main oscillator (IMO) using SLIMO mode.

Figure 10. Voltage versus CPU Frequency and IMO Frequency Trim Options



Absolute Maximum Ratings

Table 10. Absolute Maximum Ratings

Symbol	Description	Min	Typ	Max	Units	Notes
T_{STG}	Storage Temperature	–55	25	+100	°C	Higher storage temperatures reduces data retention time. Recommended storage temperature is +25 °C ± 25 °C. Extended duration storage temperatures above 65 °C degrades reliability.
$T_{BAKETEMP}$	Bake temperature	–	125	See package label	°C	
$t_{BAKETIME}$	Bake time	See package label	–	72	Hours	
T_A	Ambient temperature with power applied	–40	–	+85	°C	
V_{DD}	Supply voltage on V_{DD} relative to V_{SS}	–0.5	–	+6.0	V	
V_{IO}	DC input voltage	V_{SS} – 0.5	–	V_{DD} + 0.5	V	
V_{IOZ}	DC voltage applied to tri-state	V_{SS} – 0.5	–	V_{DD} + 0.5	V	
I_{MIO}	Maximum current into any port pin	–25	–	+50	mA	
ESD	Electro static discharge voltage	2000	–	–	V	Human body model ESD.
LU	Latch-up current	–	–	200	mA	

[+] Feedback

Operating Temperature

Table 11. Operating Temperature

Symbol	Description	Min	Typ	Max	Units	Notes
T_A	Ambient temperature	–40	–	+85	°C	
T_J	Junction temperature	–40	–	+100	°C	The temperature rise from ambient to junction is package specific. See Table 16 on page 21. The user must limit the power consumption to comply with this requirement.

DC Electrical Characteristics

DC Chip Level Specifications

Table 12 lists the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C, 3.0V to 3.6V and –40 °C ≤ T_A ≤ 85 °C, or 2.4 V to 3.0 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters apply to 5 V, 3.3 V, or 2.7 V at 25 °C. These are for design guidance only.

Table 12. DC Chip Level Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
V_{DD}	Supply voltage	2.40	–	5.25	V	See Table 16 on page 21.
I_{DD12}	Supply current, IMO = 12 MHz	–	1.5	2.5	mA	Conditions are V_{DD} = 3.0 V, T_A = 25 °C, CPU = 12 MHz.
I_{DD6}	Supply current, IMO = 6 MHz	–	1	1.5	mA	Conditions are V_{DD} = 3.0 V, T_A = 25 °C, CPU = 6 MHz
I_{SB27}	Sleep (mode) current with POR, LVD, Sleep timer, WDT, and internal slow oscillator active. Mid temperature range.	–	2.6	4	µA	V_{DD} = 2.55 V, 0 °C ≤ T_A ≤ 40 °C
I_{SB}	Sleep (mode) current with POR, LVD, Sleep timer, WDT, and internal slow oscillator active.	–	2.8	5	µA	V_{DD} = 3.3 V, –40 °C ≤ T_A ≤ 85 °C

DC GPIO Specifications

Unless otherwise noted, Table 13 lists the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C, 3.0 V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C, or Table 14 for 2.4 V to 3.0 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters apply to 5 V, 3.3 V, and 2.7 V at 25 °C. These are for design guidance only.

Table 13. 5-V and 3.3-V DC GPIO Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
R_{PU}	Pull-up resistor	4	5.6	8	kΩ	
V_{OH1}	High output voltage Port 0, 2, or 3 pins	V_{DD} – 0.2	–	–	V	I_{OH} ≤ 10 µA, V_{DD} ≥ 3.0 V, maximum of 20 mA source current in all I/Os.
V_{OH2}	High output voltage Port 0, 2, or 3 pins	V_{DD} – 0.9	–	–	V	I_{OH} = 1 mA, V_{DD} ≥ 3.0 V, maximum of 20 mA source current in all I/Os.
V_{OH3}	High output voltage Port 1 pins with LDO regulator disabled	V_{DD} – 0.2	–	–	V	I_{OH} < 10 µA, V_{DD} ≥ 3.0 V, maximum of 10 mA source current in all I/Os.
V_{OH4}	High output voltage Port 1 pins with LDO regulator disabled	V_{DD} – 0.9	–	–	V	I_{OH} = 5 mA, V_{DD} ≥ 3.0 V, maximum of 20 mA source current in all I/Os.
V_{OH5}	High output voltage Port 1 pins with 3.0 V LDO regulator enabled	2.7	3.0	3.3	V	I_{OH} < 10 µA, V_{DD} ≥ 3.1 V, maximum of 4 I/Os all sourcing 5 mA.
V_{OH6}	High output voltage Port 1 pins with 3.0 V LDO regulator enabled	2.2	–	–	V	I_{OH} = 5 mA, V_{DD} ≥ 3.1 V, maximum of 20 mA source current in all I/Os.

[+] Feedback

Table 13. 5-V and 3.3-V DC GPIO Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
V_{OH7}	High output voltage Port 1 pins with 2.4 V LDO regulator enabled	2.1	2.4	2.7	V	I_{OH} < 10 µA, $V_{DD} \geq 3.0$ V , maximum of 20 mA source current in all I/Os.
V_{OH8}	High output voltage Port 1 pins with 2.4 V LDO regulator enabled	2.0	–	–	V	I_{OH} < 200 µA, $V_{DD} \geq 3.0$ V, maximum of 20 mA source current in all I/Os.
V_{OH9}	High output voltage Port 1 pins with 1.8 V LDO regulator enabled	1.6	1.8	2.0	V	I_{OH} < 10 µA $3.0V \leq V_{DD} \leq 3.6$ V $0\ °C \leq T_A \leq 85\ °C$ Maximum of 20 mA source current in all I/Os.
V_{OH10}	High output voltage Port 1 pins with 1.8 V LDO regulator enabled	1.5	–	–	V	I_{OH} < 100 µA. $3.0V \leq V_{DD} \leq 3.6$ V. $0\ °C \leq T_A \leq 85\ °C$. Maximum of 20 mA source current in all I/Os.
V_{OL}	Low output voltage	–	–	0.75	V	I_{OL} = 20 mA, V_{DD} > 3.0 V, maximum of 60 mA sink current on even port pins (for example, P0[2] and P1[4]) and 60 mA sink current on odd port pins (for example, P0[3] and P1[5]).
I_{OH}	High level source current	–	–	20	mA	$V_{OH} = V_{DD} – 0.9$. See the limitations of the total current in the Notes for V_{OH}.
I_{OH2}	High level source current port 0, 2, or 3 pins	1	–	–	mA	$V_{OH} = V_{DD} – 0.9$, for the limitations of the total current and I_{OH} at other V_{OH} levels, see the Notes for V_{OH}.
I_{OH4}	High level source current port 1 Pins with LDO regulator disabled	5	–	–	mA	$V_{OH} = V_{DD} – 0.9$, for the limitations of the total current and I_{OH} at other V_{OH} levels, see the Notes for V_{OH}.
I_{OL}	Low level sink current	20	–	–	mA	V_{OL} = 0.75 V, see the limitations of the total current in the Notes for V_{OL}
V_{IL}	Input low voltage	–	–	0.8	V	$3.6\ V \leq V_{DD} \leq 5.25$ V
V_{IH}	Input high voltage	2.0	–	–	V	$3.6\ V \leq V_{DD} \leq 5.25$ V
V_H	Input hysteresis voltage	–	140	–	mV	
I_{IL}	Input leakage (absolute value)	–	1	–	nA	Gross tested to 1 µA
C_{IN}	Capacitive load on pins as input	0.5	1.7	5	pF	Package and pin dependent Temperature = 25 °C
C_{OUT}	Capacitive load on pins as output	0.5	1.7	5	pF	Package and pin dependent Temperature = 25 °C

[+] Feedback

Table 14. 2.7-V DC GPIO Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
R_{PU}	Pull-up resistor	4	5.6	8	kΩ	
V_{OH1}	High output voltage Port 1 pins with LDO regulator disabled	V_{DD} – 0.2	–	–	V	I_{OH} < 10 µA, maximum of 10 mA source current in all I/Os.
V_{OH2}	High output voltage Port 1 pins with LDO regulator disabled	V_{DD} – 0.5	–	–	V	I_{OH} = 2 mA, maximum of 10 mA source current in all I/Os.
V_{OL}	Low output voltage	–	–	0.75	V	I_{OL} = 10 mA, maximum of 30 mA sink current on even port pins (for example, P0[2] and P1[4]) and 30 mA sink current on odd port pins (for example, P0[3] and P1[5]).
I_{OH2}	High level source current port 1 Pins with LDO regulator disabled	2	–	–	mA	V_{OH} = V_{DD} – 0.5, for the limitations of the total current and I_{OH} at other V_{OH} levels see the notes for V_{OH}.
I_{OL}	Low level sink current	10	–	–	mA	V_{OH} = .75 V, see the limitations of the total current in the note for V_{OL}
V_{OLP1}	Low output voltage port 1 pins	–	–	0.4	V	I_{OL} = 5 mA Maximum of 50 mA sink current on even port pins (for example, P0[2] and P3[4]) and 50 mA sink current on odd port pins (for example, P0[3] and P2[5]). 2.4 V ≤ V_{DD} < 3.6 V
V_{IL}	Input low voltage	–	–	0.75	V	2.4 V ≤ V_{DD} < 3.6 V
V_{IH1}	Input high voltage	1.4	–	–	V	2.4 V ≤ V_{DD} < 2.7 V
V_{IH2}	Input high voltage	1.6	–	–	V	2.7 V ≤ V_{DD} < 3.6 V
V_H	Input hysteresis voltage	–	60	–	mV	
I_{IL}	Input leakage (absolute value)	–	1	–	nA	Gross tested to 1 µA
C_{IN}	Capacitive load on pins as input	0.5	1.7	5	pF	Package and pin dependent Temperature = 25 °C
C_{OUT}	Capacitive load on pins as output	0.5	1.7	5	pF	Package and pin dependent Temperature = 25 °C

DC Analog Mux Bus Specifications

Table 15 lists the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C, 3.0 V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C, or 2.4 V to 3.0 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters apply to 5 V, 3.3 V, or 2.7 V at 25 °C. These are for design guidance only.

Table 15. DC Analog Mux Bus Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
R_{SW}	Switch resistance to common analog bus	–	–	400 800	Ω Ω	V_{DD} ≥ 2.7 V 2.4 V ≤ V_{DD} ≤ 2.7 V

[+] Feedback

DC POR and LVD Specifications

Table 16 lists the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C, 3.0 V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C, or 2.4 V to 3.0 V and –40 °C ≤ T_A ≤ 85 °C, respectively.

Typical parameters apply to 5 V, 3.3 V, or 2.7 V at 25 °C. These are for design guidance only.

Table 16. DC POR and LVD Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
	V_{DD} value for PPOR trip					V_{DD} is greater than or equal to 2.5 V during startup, reset from the XRES pin, or reset from watchdog.
V_{PPOR0}	PORLEV[1:0] = 00b	–	2.36	2.40	V	
V_{PPOR1}	PORLEV[1:0] = 01b	–	2.60	2.65	V	
V_{PPOR2}	PORLEV[1:0] = 10b	–	2.82	2.95	V	
	V_{DD} value for LVD trip					
V_{LVD0}	VM[2:0] = 000b	2.39	2.45	2.51[13]	V	
V_{LVD1}	VM[2:0] = 001b	2.54	2.71	2.78[14]	V	
V_{LVD2}	VM[2:0] = 010b	2.75	2.92	2.99[15]	V	
V_{LVD3}	VM[2:0] = 011b	2.85	3.02	3.09	V	
V_{LVD4}	VM[2:0] = 100b	2.96	3.13	3.20	V	
V_{LVD5}	VM[2:0] = 101b	–	–	–	V	
V_{LVD6}	VM[2:0] = 110b	–	–	–	V	
V_{LVD7}	VM[2:0] = 111b	4.52	4.73	4.83	V	

Notes
13. Always greater than 50 mV above V_{PPOR} (PORLEV = 00) for falling supply.
14. Always greater than 50 mV above V_{PPOR} (PORLEV = 01) for falling supply.
15. Always greater than 50 mV above V_{PPOR} (PORLEV = 10) for falling supply.

[+] Feedback

DC Programming Specifications

Table 17 lists the guaranteed minimum and maximum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C, 3.0 V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C, or 2.4 V to 3.0 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters apply to 5 V, 3.3 V, or 2.7 V at 25 °C. These are for design guidance only. Flash endurance and retention specifications with the use of the EEPROM User Module are valid only within the range: 25 °C +/–20C during the Flash Write operation. Reference the EEPROM User Module datasheet instructions for EEPROM flash write requirements outside of the 25 °C +/–20 °C temperature window.

Table 17. DC Programming Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
V_{DDP}	V_{DD} for programming and erase	4.5	5	5.5	V	This specification applies to the functional requirements of external programmer tools
V_{DDLV}	Low V_{DD} for verify	2.4	2.5	2.6	V	This specification applies to the functional requirements of external programmer tools
V_{DDHV}	High V_{DD} for verify	5.1	5.2	5.3	V	This specification applies to the functional requirements of external programmer tools
$V_{DDIWRITE}$	Supply voltage for flash write operation	2.7	–	5.25	V	This specification applies to this device when it is executing internal flash writes
I_{DDP}	Supply current during programming or verify	–	5	25	mA	
V_{ILP}	Input low voltage during programming or verify	–	–	0.8	V	
V_{IHP}	Input high voltage during programming or verify	2.2	–	–	V	
I_{ILP}	Input current when applying V_{ILP} to P1[0] or P1[1] during programming or verify	–	–	0.2	mA	Driving internal pull-down resistor.
I_{IHP}	Input current when applying V_{IHP} to P1[0] or P1[1] during programming or verify	–	–	1.5	mA	Driving internal pull-down resistor.
V_{OLV}	Output low voltage during programming or verify	–	–	V_{SS} + 0.75	V	
V_{OHV}	Output high voltage during programming or verify	V_{DD} – 1.0	–	V_{DD}	V	
$Flash_{ENPB}$	Flash endurance (per block)	50,000[17]	–	–	–	Erase/write cycles per block.
$Flash_{ENT}$	Flash endurance (total)[16]	1,800,000	–	–	–	Erase/write cycles.
$Flash_{DR}$	Flash data retention	10	–	–	Years	

Notes

16. A maximum of 36 × 50,000 block endurance cycles is allowed. This is balanced between operations on 36 × 1 blocks of 50,000 maximum cycles each, 36 × 2 blocks of 25,000 maximum cycles each, or 36 × 4 blocks of 12,500 maximum cycles each (to limit the total number of cycles to 36 × 50,000 and that no single block ever sees more than 50,000 cycles).
17. The 50,000 cycle flash endurance per block is only guaranteed if the flash is operating within one voltage range. Voltage ranges are 2.4 V to 3.0 V, 3.0 V to 3.6 V and 4.75 V to 5.25 V.

[+] Feedback

DC I²C Specifications

Table 18 lists the guaranteed minimum and maximum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C, 3.0V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C, or 2.4 V to 3.0 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters apply to 5 V, 3.3 V, or 2.7 V at 25 °C. These are for design guidance only. Flash endurance and retention specifications with the use of the EEPROM user module are valid only within the range: 25 °C +/–20C during the Flash Write operation. Reference the EEPROM User Module datasheet instructions for EEPROM flash Write requirements outside of the 25 °C +/–20 °C temperature window.

Table 18. DC I²C Specifications[18]

Symbol	Description	Min	Typ	Max	Units	Notes
V_{ILI2C}	Input low level	–	–	0.3 × V_{DD}	V	2.4 V ≤ V_{DD} ≤ 3.6 V
		–	–	0.25 × V_{DD}	V	4.75 V ≤ V_{DD} ≤ 5.25 V
V_{IHI2C}	Input high level	0.7 × V_{DD}	–	–	V	2.4 V ≤ V_{DD} ≤ 5.25 V

AC Electrical Characteristics

AC Chip Level Specifications

Table 19, Table 20, and Table 21 list the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C, 3.0 V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C, or 2.4 V to 3.0 V and –40 °C ≤ T_A ≤ 85 °C respectively. Typical parameters apply to 5 V, 3.3 V, or 2.7 V at 25 °C. These are for design guidance only.

Table 19. 5-V and 3.3-V AC Chip-Level Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
F_{CPU1}	CPU frequency (3.3 V nominal)	0.75	–	12.6	MHz	12 MHz only for SLIMO Mode = 0.
F_{32K1}	Internal low speed oscillator frequency	15	32	64	kHz	
F_{32K_U}	Internal low speed oscillator (ILO) untrimmed frequency	5	–	100	kHz	After a reset and before the M8C starts to run, the ILO is not trimmed. See the System Resets section of the PSoC Technical Reference Manual for details on this timing.
F_{IMO12}	Internal main oscillator stability for 12 MHz (commercial temperature)[19]	11.4	12	12.6	MHz	Trimmed for 3.3 V operation using factory trim values. See Figure 10 on page 17, SLIMO mode = 0.
F_{IMO6}	Internal main oscillator stability for 6 MHz (commercial temperature)	5.5	6.0	6.5	MHz	Trimmed for 3.3 V operation using factory trim values. See Figure 10 on page 17, SLIMO mode = 1.
DC_{IMO}	Duty cycle of IMO	40	50	60	%	
DC_{ILO}	Internal low speed oscillator duty cycle	20	50	80	%	
t_{XRST}	External reset pulse width	10	–	–	µs	
$t_{POWERUP}$	Time from end of POR to CPU executing code	–	16	100	ms	Power-up from 0 V. See the System Resets section of the PSoC Technical Reference Manual.
SR_{POWER_UP}	Power supply slew rate	–	–	250	V/ms	
t_{jit_IMO} [20]	12 MHz IMO cycle-to-cycle jitter (RMS)	–	200	1600	ps	
	12 MHz IMO long term N cycle-to-cycle jitter (RMS)	–	600	1400	ps	N = 32
	12 MHz IMO period jitter (RMS)	–	100	900	ps	

Notes
18. All GPIO meet the DC GPIO V_{IL} and V_{IH} specifications found in the DC GPIO Specifications sections. The I²C GPIO pins also meet the above specs.
19. 0 to 70 °C ambient, V_{DD} = 3.3 V.
20. Refer to Cypress Jitter Specifications Application Note – AN5054 at http://www.cypress.com for more information.

[+] Feedback

Table 20. 2.7-V AC Chip Level Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
F_{CPU1}	CPU Frequency (2.7 V nominal)	0.75	–	3.25	MHz	SLIMO mode = 0
F_{32K1}	Internal low speed oscillator frequency	8	32	96	kHz	
F_{32K_U}	Internal low speed oscillator (ILO) untrimmed frequency	5	–	100	kHz	After a reset and before the M8C starts to run, the ILO is not trimmed. See the System Resets section of the PSoC Technical Reference Manual for details on this timing.
F_{IMO12}	IMO stability for 12 MHz (commercial temperature)[21]	11.0	12	12.9	MHz	Trimmed for 2.7 V operation using factory trim values. See Figure 10 on page 17, SLIMO mode = 0.
F_{IMO6}	IMO stability for 6 MHz (commercial temperature)	5.5	6.0	6.5	MHz	Trimmed for 2.7 V operation using factory trim values. See Figure 10 on page 17, SLIMO mode = 1.
DC_{IMO}	Duty cycle of IMO	40	50	60	%	
DC_{ILO}	Internal low speed oscillator duty cycle	20	50	80	%	
t_{XRST}	External reset pulse width	10	–	–	µs	
$t_{POWERUP}$	Time from end of POR to CPU executing code	–	16	100	ms	Power-up from 0 V. See the System Resets section of the PSoC Technical Reference Manual
SR_{POWER_UP}	Power supply slew rate	–	–	250	V/ms	
t_{JIT_IMO} [22]	12 MHz IMO cycle-to-cycle jitter (RMS)	–	500	900	ps	
	12 MHz IMO long term N cycle-to-cycle jitter (RMS)	–	800	1400	ps	N = 32
	12 MHz IMO period jitter (RMS)	–	300	500	ps	

Notes
21. 0 °C to 70 °C ambient, V_{DD} = 3.3 V.
22. Refer to Cypress Jitter Specifications Application Note – AN5054 at http://www.cypress.com for more information.

[+] Feedback

AC GPIO Specifications

Table 21 and Table 22 list the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C, 3.0 V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C, or 2.4 V to 3.0 V and –40 °C ≤ T_A ≤ 85 °C respectively. Typical parameters apply to 5 V, 3.3 V, or 2.7 V at 25 °C. These are for design guidance only.

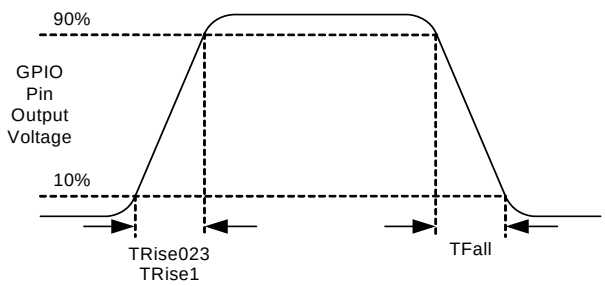
Table 21. 5-V and 3.3-V AC GPIO Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
F_{GPIO}	GPIO operating frequency	0	–	6	MHz	Normal strong mode, port 1.
$t_{RISE023}$	Rise time, strong mode, Cload = 50 pF ports 0, 2, 3	15	–	80	ns	V_{DD} = 3.0 to 3.6 V and 4.75 V to 5.25 V, 10% to 90%
t_{RISE1}	Rise time, strong mode, Cload = 50 pF port 1	10	–	50	ns	V_{DD} = 3.0 V to 3.6 V, 10% to 90%
t_{FALL}	Fall time, strong mode, Cload = 50 pF all ports	10	–	50	ns	V_{DD} = 3.0 V to 3.6 V and 4.75 V to 5.25 V, 10% to 90%

Table 22. 2.7-V AC GPIO Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
F_{GPIO}	GPIO operating frequency	0	–	1.5	MHz	Normal strong mode, port 1.
$t_{RISE023}$	Rise time, strong mode, Cload = 50 pF ports 0, 2, 3	15	–	100	ns	V_{DD} = 2.4 V to 3.0 V, 10% to 90%
t_{RISE1}	Rise time, strong mode, Cload = 50 pF port 1	10	–	70	ns	V_{DD} = 2.4 V to 3.0 V, 10% to 90%
t_{FALL}	Fall time, strong mode, Cload = 50 pF all Ports	10	–	70	ns	V_{DD} = 2.4 V to 3.0 V, 10% to 90%

Figure 11. GPIO Timing Diagram



AC Comparator Specifications

Table 23 lists the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C, 3.0 V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C, or 2.4 V to 3.0 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters apply to 5 V, 3.3 V, or 2.7 V at 25 °C. These are for design guidance only.

Table 23. AC Comparator Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
t_{COMP}	Comparator response time, 50 mV overdrive	–	–	100 200	ns ns	V_{DD} ≥ 3.0 V. 2.4 V < V_{CC} < 3.0 V.

[+] Feedback

AC External Clock Specifications

Table 24, Table 25, Table 26, and Table 27 list the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C, 3.0 V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C, or 2.4 V to 3.0 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters apply to 5 V, 3.3 V, or 2.7 V at 25 °C. These are for design guidance only.

Table 24. 5-V AC External Clock Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
F_{OSCEXT}	Frequency	0.750	–	12.6	MHz	
–	High period	38	–	5300	ns	
–	Low period	38	–	–	ns	
–	Power-up IMO to switch	150	–	–	µs	

Table 25. 3.3-V AC External Clock Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
F_{OSCEXT}	Frequency with CPU clock divide by 1	0.750	–	12.6	MHz	Maximum CPU frequency is 12 MHz at 3.3 V. With the CPU clock divider set to 1, the external clock must adhere to the maximum frequency and duty cycle requirements.
–	High period with CPU clock divide by 1	41.7	–	5300	ns	
–	Low period with CPU clock divide by 1	41.7	–	–	ns	
–	Power-up IMO to switch	150	–	–	µs	

Table 26. 2.7-V (Nominal) AC External Clock Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
F_{OSCEXT}	Frequency with CPU clock divide by 1	0.750	–	3.08	MHz	Maximum CPU frequency is 3 MHz at 2.7 V. With the CPU clock divider set to 1, the external clock must adhere to the maximum frequency and duty cycle requirements.
F_{OSCEXT}	Frequency with CPU clock divide by 2 or greater	0.15	–	6.35	MHz	If the frequency of the external clock is greater than 3 MHz, the CPU clock divider is set to 2 or greater. In this case, the CPU clock divider ensures that the fifty percent duty cycle requirement is met.
–	High period with CPU clock divide by 1	160	–	5300	ns	
–	Low period with CPU clock divide by 1	160	–	–	ns	
–	Power-up IMO to switch	150	–	–	µs	

Table 27. 2.7-V (Minimum) AC External Clock Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
F_{OSCEXT}	Frequency with CPU clock divide by 1	0.750	–	6.3	MHz	Maximum CPU frequency is 6 MHz at 2.7 V. With the CPU clock divider set to 1, the external clock must adhere to the maximum frequency and duty cycle requirements.
F_{OSCEXT}	Frequency with CPU clock divide by 2 or greater	0.15	–	12.6	MHz	If the frequency of the external clock is greater than 6 MHz, the CPU clock divider is set to 2 or greater. In this case, the CPU clock divider ensures that the fifty percent duty cycle requirement is met.
–	High period with CPU clock divide by 1	160	–	5300	ns	
–	Low period with CPU clock divide by 1	160	–	–	ns	
–	Power-up IMO to switch	150	–	–	µs	

[+] Feedback

AC Programming Specifications

Table 28 lists the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C, 3.0 V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C, or 2.4 V to 3.0 V and –40 °C ≤ T_A ≤ 85 °C respectively. Typical parameters apply to 5 V, 3.3 V, or 2.7 V at 25 °C. These are for design guidance only.

Table 28. AC Programming Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
t_{RSCLK}	Rise time of SCLK	1	–	20	ns	
t_{FSCLK}	Fall time of SCLK	1	–	20	ns	
t_{SSCLK}	Data setup time to falling edge of SCLK	40	–	–	ns	
t_{HSCLK}	Data hold time from falling edge of SCLK	40	–	–	ns	
F_{SCLK}	Frequency of SCLK	0	–	8	MHz	
t_{ERASEB}	Flash erase time (Block)	–	10	–	ms	
t_{WRITE}	Flash block write time	–	40	–	ms	
t_{DSCLK}	Data out delay from falling edge of SCLK	–	–	45	ns	3.6 < V_{DD}
t_{DSCLK3}	Data out delay from falling edge of SCLK	–	–	50	ns	3.0 ≤ V_{DD} ≤ 3.6
t_{DSCLK2}	Data out delay from falling edge of SCLK	–	–	70	ns	2.4 ≤ V_{DD} ≤ 3.0
$t_{ERASEALL}$	Flash erase time (Bulk)	–	20	–	ms	Erase all blocks and protection fields at once
$t_{PROGRAM_HOT}$	Flash block erase + flash block write time	–	–	100	ms	0 °C ≤ T_j ≤ 100 °C
$t_{PROGRAM_COLD}$	Flash block erase + flash block write time	–	–	200	ms	–40 °C ≤ T_j ≤ 0 °C

AC I^2C Specifications

Table 29 and Table 30 list the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C, 3.0 V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C, or 2.4 V to 3.0 V and –40 °C ≤ T_A ≤ 85 °C respectively. Typical parameters apply to 5 V, 3.3 V, or 2.7 V at 25 °C. These are for design guidance only.

Table 29. AC Characteristics of the I^2C SDA and SCL Pins for V_{DD} ≥ 3.0 V

Symbol	Description	Standard Mode		Fast Mode		Units
		Min	Max	Min	Max	
F_{SCLI2C}	SCL clock frequency	0	100	0	400	kHz
$t_{HDSTAI2C}$	Hold time (repeated) START condition. After this period, the first clock pulse is generated	4.0	–	0.6	–	µs
t_{LOWI2C}	LOW period of the SCL clock	4.7	–	1.3	–	µs
$t_{HIGHI2C}$	HIGH period of the SCL clock	4.0	–	0.6	–	µs
$t_{SUSTAI2C}$	Setup time for a repeated START condition	4.7	–	0.6	–	µs
$t_{HDDATI2C}$	Data hold time	0	–	0	–	µs
$t_{SUDATI2C}$	Data setup time	250	–	100[23]	–	ns
$t_{SUSTOI2C}$	Setup time for STOP condition	4.0	–	0.6	–	µs
t_{BUFI2C}	Bus free time between a STOP and START condition	4.7	–	1.3	–	µs
t_{SPI2C}	Pulse width of spikes are suppressed by the input filter	–	–	0	50	ns

Note

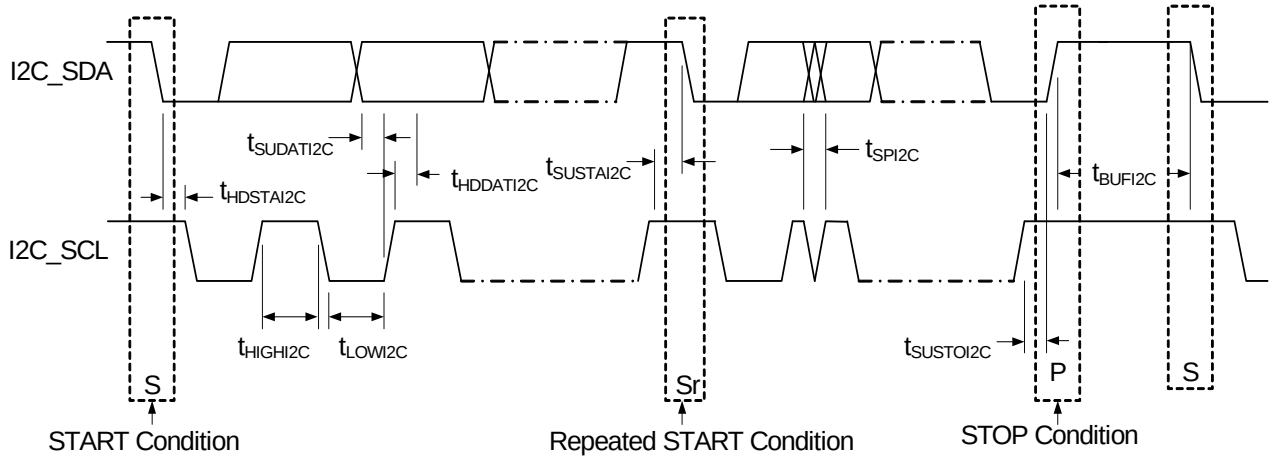
23. A Fast Mode I^2C bus device is used in a Standard Mode I^2C bus system but the requirement tSU; DAT ≥ 250 ns is met. This automatically is the case if the device does not stretch the LOW period of the SCL signal. If such device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line trmax + tSU; DAT = 1000 + 250 = 1250 ns (according to the Standard Mode I^2C bus specification) before the SCL line is released.

[+] Feedback

Table 30. 2.7-V AC Characteristics of the I²C SDA and SCL Pins (Fast Mode not Supported)

Symbol	Description	Standard Mode		Fast Mode		Units
		Min	Max	Min	Max	
F_{SCLI2C}	SCL clock frequency	0	100	–	–	kHz
$t_{HDSTAI2C}$	Hold time (repeated) START condition. After this period, the first clock pulse is generated	4.0	–	–	–	µs
t_{LOWI2C}	LOW period of the SCL clock	4.7	–	–	–	µs
$t_{HIGHI2C}$	HIGH period of the SCL clock	4.0	–	–	–	µs
$t_{SUSTAI2C}$	Setup time for a repeated start condition	4.7	–	–	–	µs
$t_{HDDATI2C}$	Data hold time	0	–	–	–	µs
$t_{SUDATI2C}$	Data setup time	250	–	–	–	ns
$t_{SUSTOI2C}$	Setup time for STOP condition	4.0	–	–	–	µs
t_{BUFI2C}	Bus free time between a STOP and START condition	4.7	–	–	–	µs
t_{SPI2C}	Pulse width of spikes are suppressed by the input filter	–	–	–	–	ns

Figure 12. Definition for Timing for Fast/Standard Mode on the I²C Bus



[+] Feedback

AC SPI Specifications

Table 31 and Table 32 list the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C, 3.0 V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C, or 2.4 V to 3.0 V and –40 °C ≤ T_A ≤ 85 °C respectively. Typical parameters apply to 5 V, 3.3 V, or 2.7 V at 25 °C. These are for design guidance only.

Table 31. SPI Master AC Specifications

Symbol	Parameter	Conditions	Min	Typ	Max	Units
F_{SCLK}	SCLK clock frequency	–	–	–	12	MHz
DC_{SCLK}	SCLK duty cycle	–	–	50	–	%
t_{SETUP}	MISO to SCLK setup time	–	40	–	–	ns
t_{HOLD}	SCLK to MISO hold time	–	40	–	–	ns
t_{OUT_VAL}	SCLK to MOSI valid time	–	–	–	40	ns
t_{OUT_HIGH}	MOSI high time	–	40	–	–	ns

Table 32. SPI Slave AC Specifications

Symbol	Parameter	Conditions	Min	Typ	Max	Units
F_{SCLK}	SCLK clock frequency	–	–	–	12	MHz
t_{LOW}	SCLK low time	–	41.67	–	–	ns
t_{HIGH}	SCLK high time	–	41.67	–	–	ns
t_{SETUP}	MOSI to SCLK setup time	–	30	–	–	ns
t_{HOLD}	SCLK to MOSI hold time	–	50	–	–	ns
t_{SS_MISO}	SS low to MISO valid	–	–	–	153	ns
t_{SCLK_MISO}	SCLK to MISO valid	–	–	–	125	ns
t_{SS_HIGH}	SS high time	–	50	–	–	ns
t_{SS_SCLK}	Time from SS low to first SCLK	–	$2/F_{SCLK}$	–	–	ns
t_{SCLK_SS}	Time from last SCLK to SS high	–	$2/F_{SCLK}$	–	–	ns

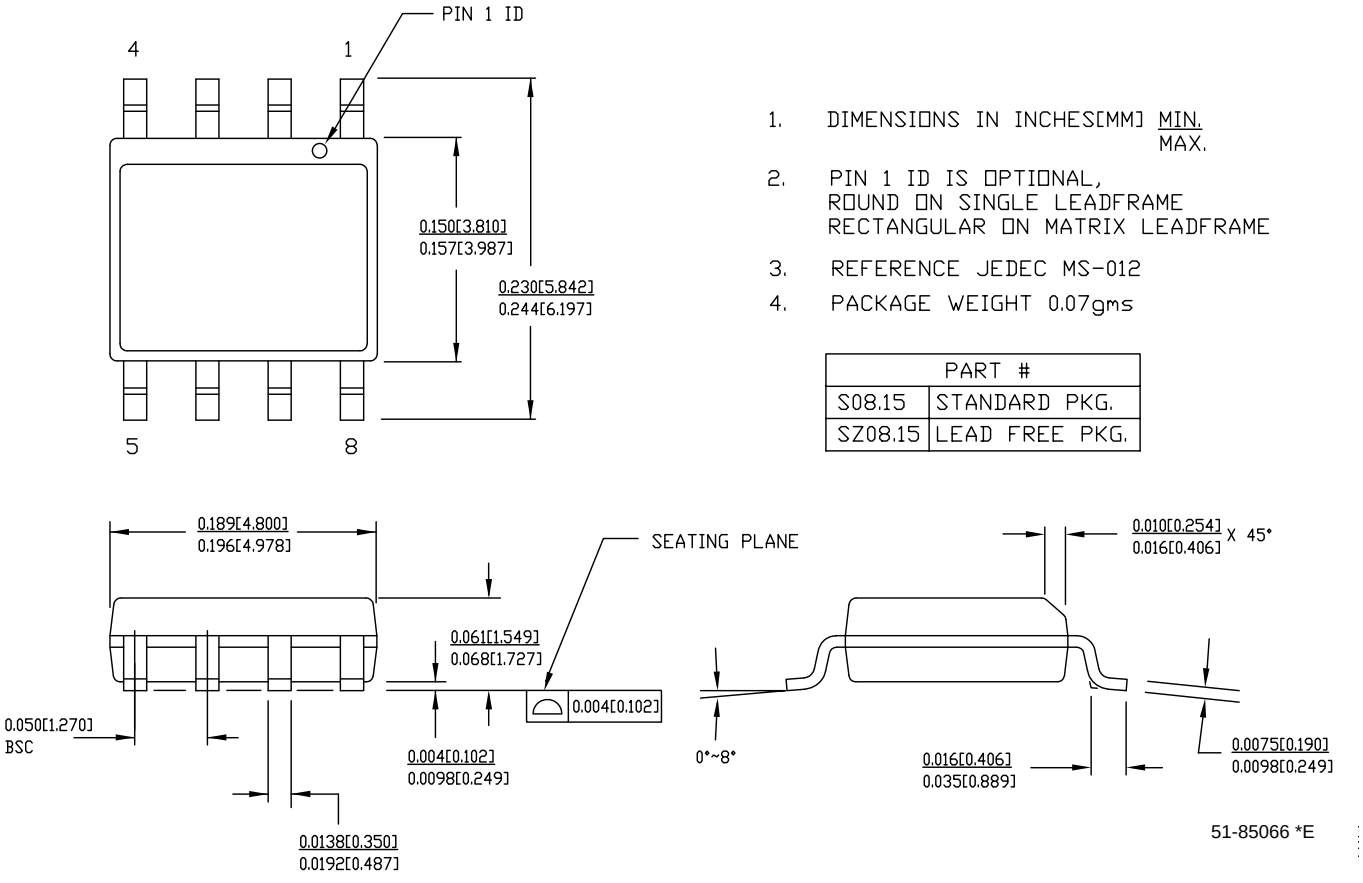
[+] Feedback

Packaging Dimensions

This section illustrates the packaging specifications for the CY8C20234, CY8C20334, CY8C20434, CY8C20534, and CY8C20634 PSoC devices along with the thermal impedances for each package.

Important Note Emulation tools may require a larger area on the target PCB than the chip's footprint. For a detailed description of the emulation tools' dimensions, refer to the emulator pod drawings at http://www.cypress.com.

Figure 13. 8-Pin (150-Mil) SOIC



[+] Feedback

Figure 14. 16-Pin (150-Mil) SOIC

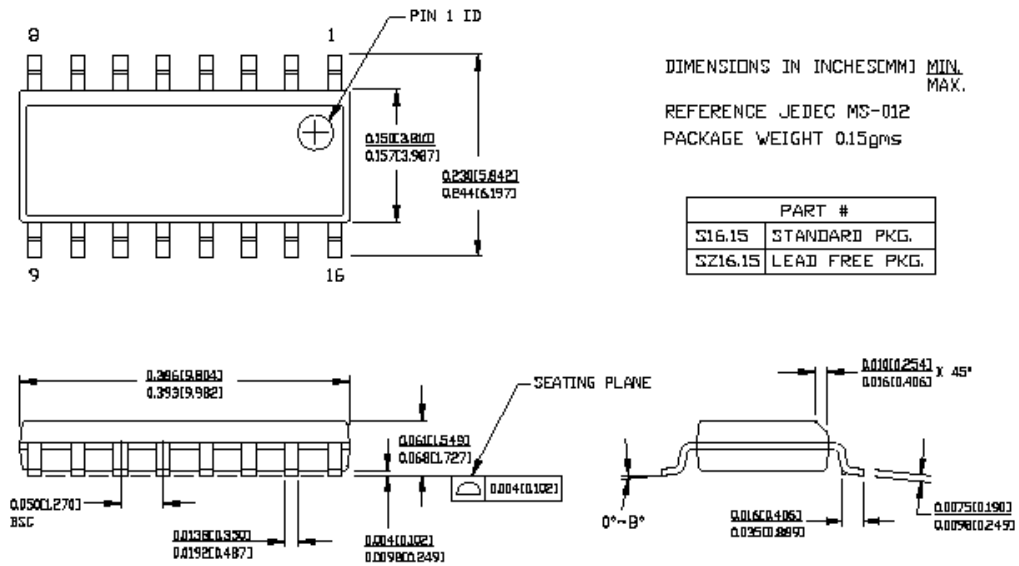
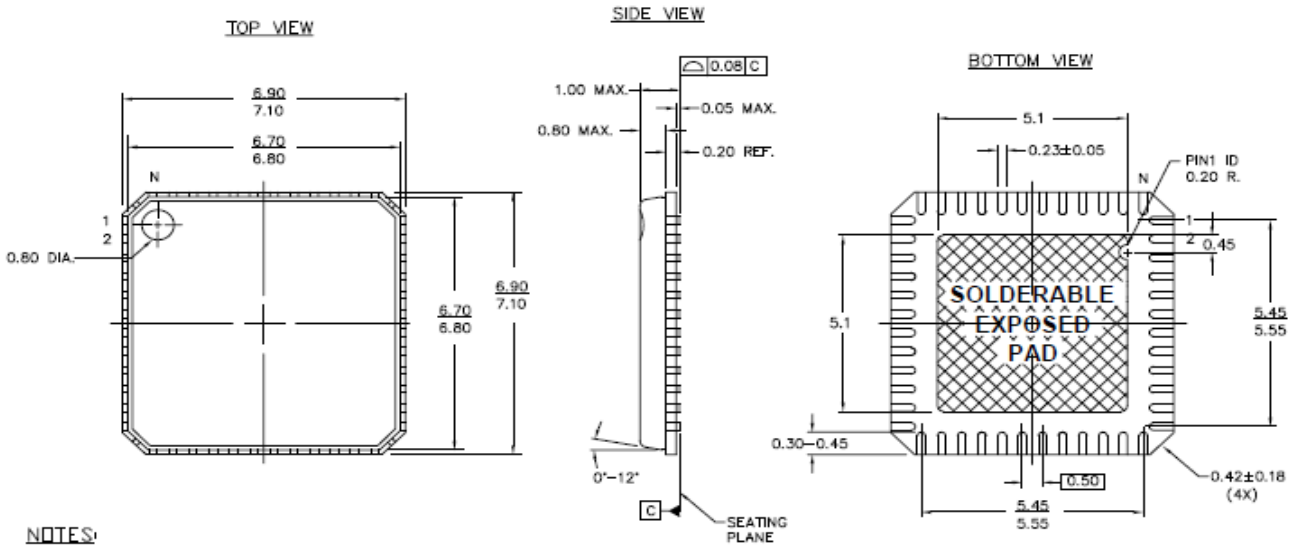


Figure 15. 48-Pin (7 × 7 × 1.0 mm) QFN



NOTES:

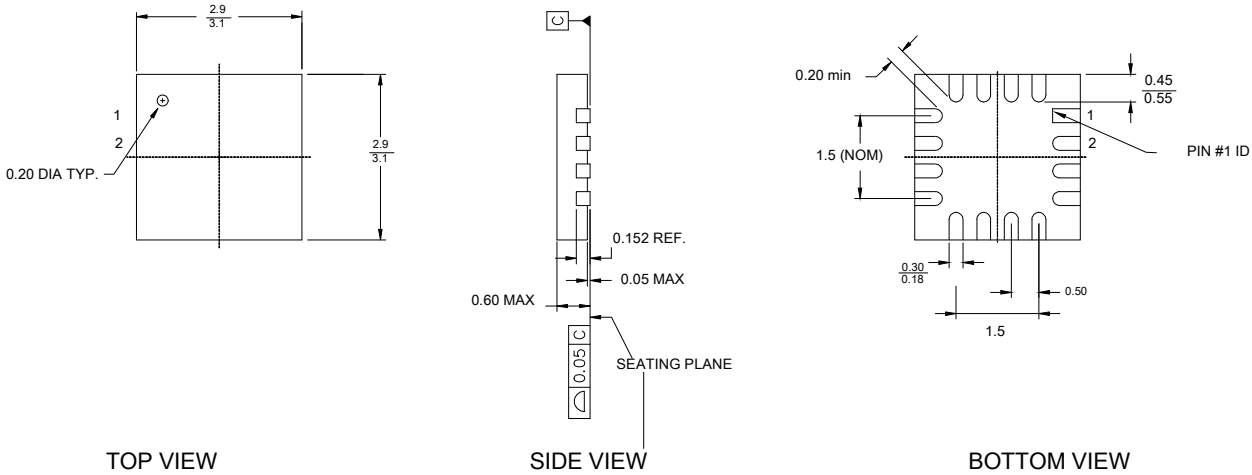
1. HATCH AREA IS SOLDERABLE EXPOSED METAL.
2. REFERENCE JEDEC#: MO-220
3. PACKAGE WEIGHT: 0.13g
4. ALL DIMENSIONS ARE IN MM [MIN/MAX]
5. PACKAGE CODE

PART #	DESCRIPTION
LF48A	STANDARD
LY48A	LEAD FREE

001-12919*C

[+] Feedback

Figure 16. 16-Pin QFN No E-Pad 3 × 3 × 0.6 mm Package Outline (Sawn)



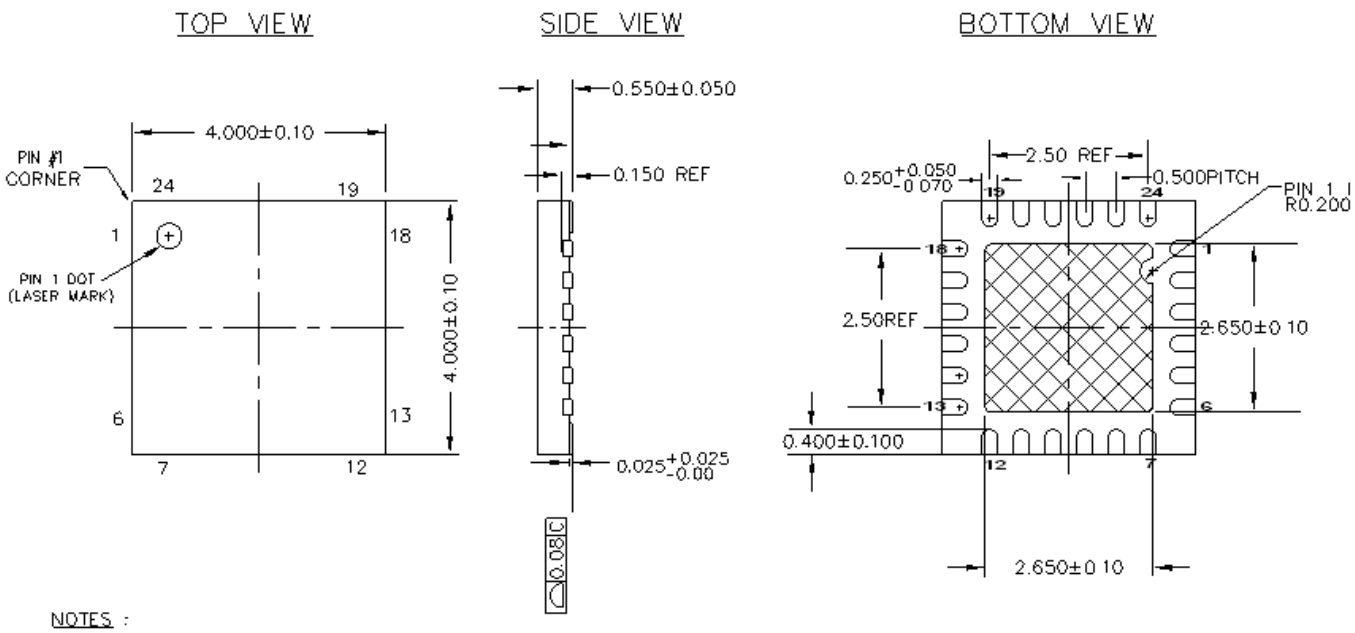
PART NO.	DESCRIPTION
LG16A	LEAD-FREE
LD16A	STANDARD

NOTES:

1. JEDEC # MO-220
2. Package Weight: 0.014g
3. DIMENSIONS IN MM, MIN MAX

001-09116 *E

Figure 17. 24-Pin (4 × 4 × 0.55 mm) Sawn QFN



NOTES :

1. HATCH IS SOLDERABLE EXPOSED METAL.
2. REFERENCE JEDEC # MO-248
3. UNIT PACKAGE WEIGHT : 0.024 grams
4. ALL DIMENSIONS ARE IN MILLIMETERS

001-13937 *C

[+] Feedback

Figure 18. 32-Pin QFN 5 × 5 × 0.55 mm (Sawn)

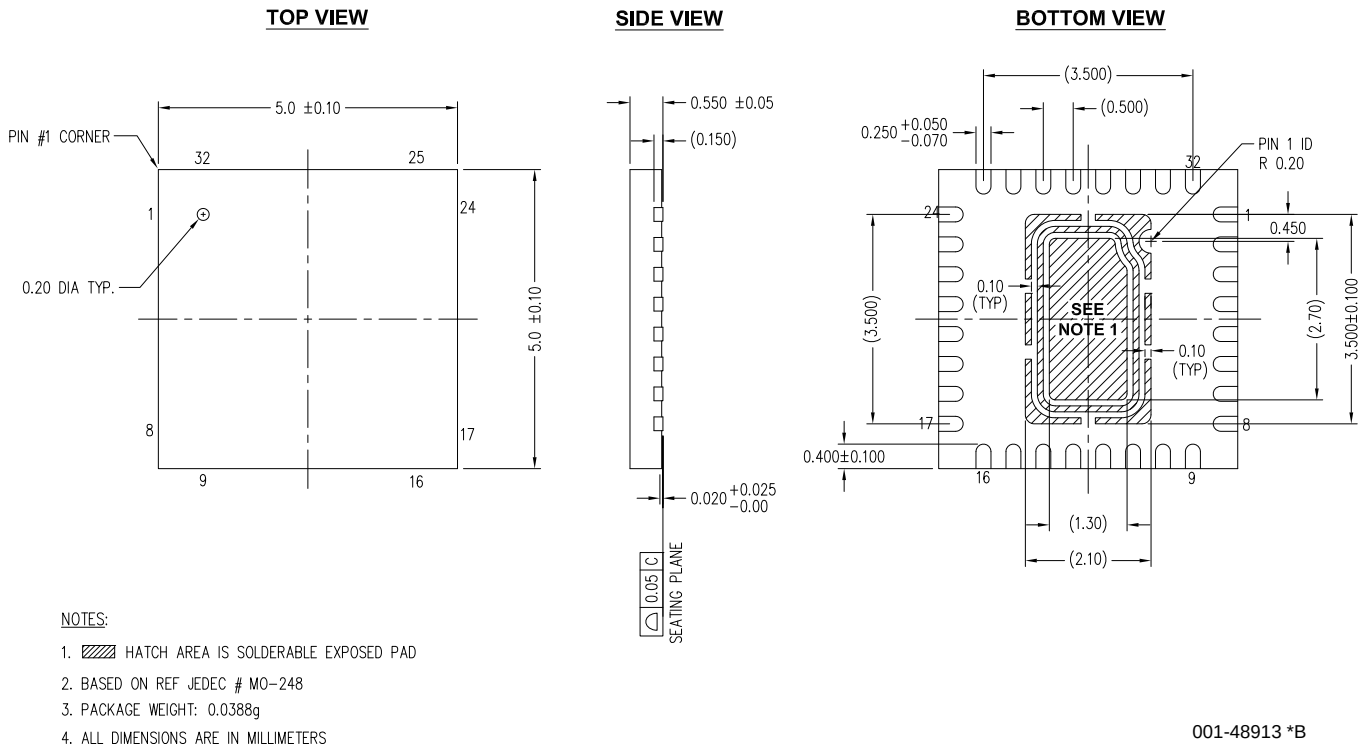
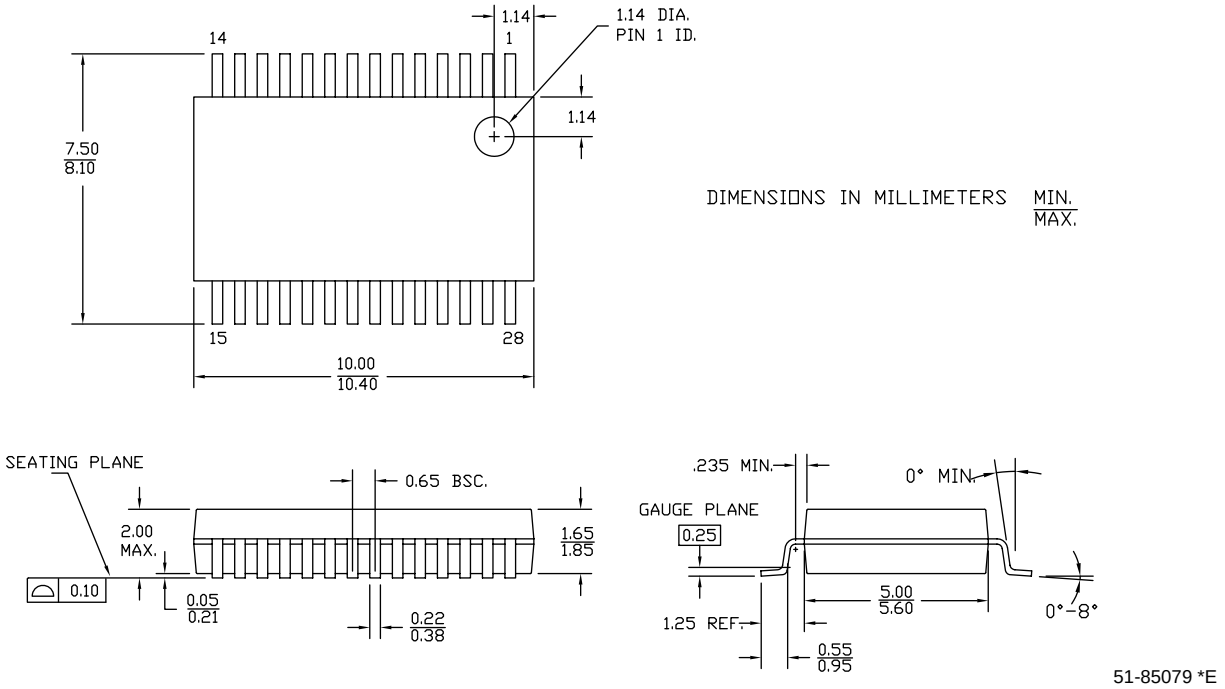
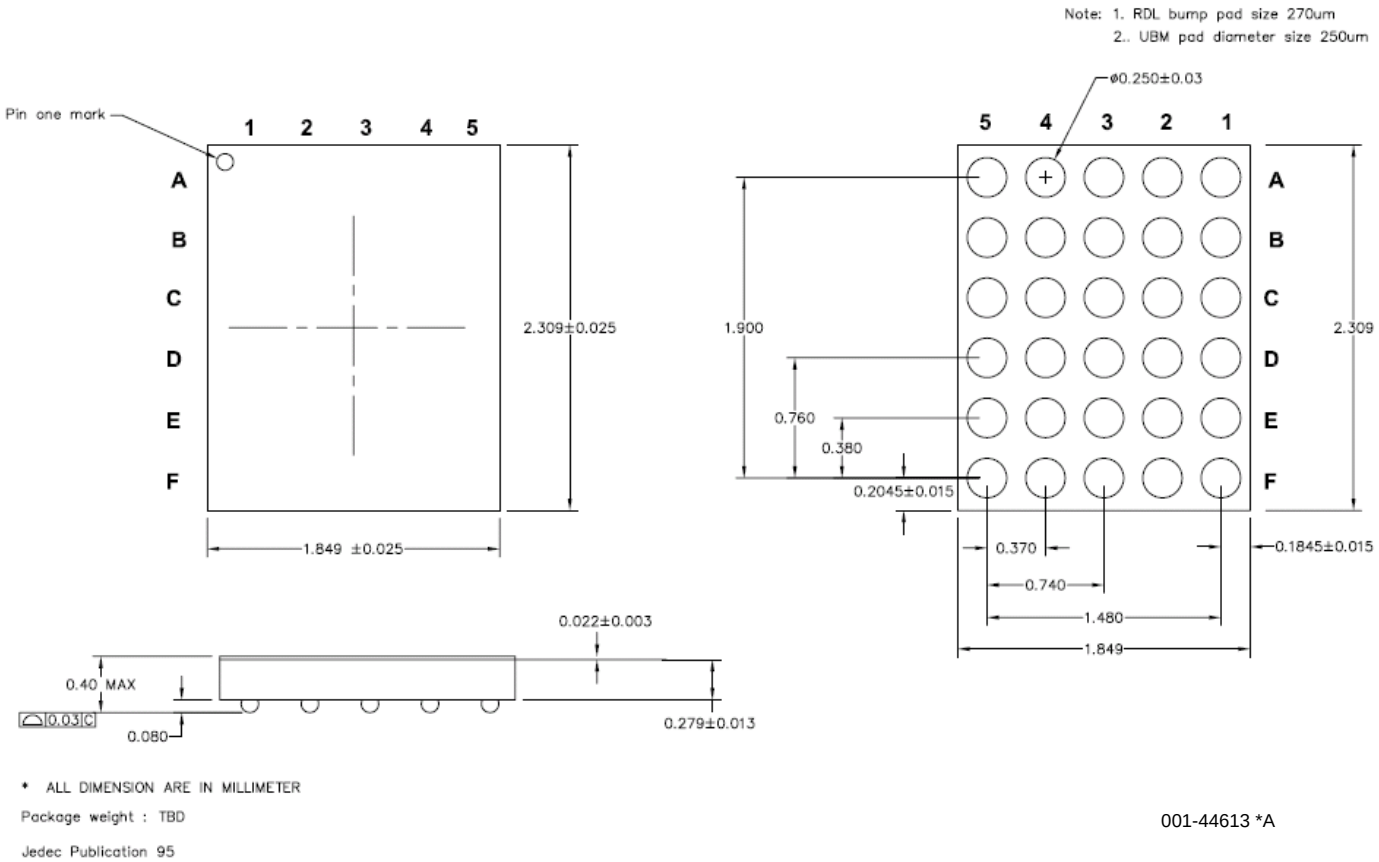


Figure 19. 28-Pin (210-Mil) SSOP



[+] Feedback

Figure 20. 30-Ball (1.85 × 2.31 × 0.40 mm) WLCSP



Important Note For information on the preferred dimensions for mounting the QFN packages, see the application note “Application Notes for Surface Mount Assembly of Amkor's MicroLeadFrame (MLF) Packages” available at http://www.amkor.com.

It is important to note that pinned vias for thermal conduction are not required for the low power 24, 32, and 48-pin QFN PSoC devices.

[+] Feedback

Thermal Impedances

Table 33 illustrates the minimum solder reflow peak temperature to achieve good solderability.

Table 33. Thermal Impedances Per Package

Package	Typical θ_{JA} [24]
8 SOIC	127 °C/W
16 SOIC	80 °C/W
16 QFN	46 °C/W
24 QFN[25]	25 °C/W
28 SSOP	96 °C/W
30 WLCSP	54 °C/W
32 QFN[25]	27 °C/W
48 QFN[25]	28 °C/W

Solder Reflow Specifications

Table 34 shows the solder reflow temperature limits that must not be exceeded.

Table 34. Solder Reflow Specifications

Package	Maximum Peak Temperature (T_C)	Maximum Time above T_C – 5 °C
8-Pin SOIC	260 °C	30 seconds
16-Pin SOIC	260 °C	30 seconds
16-Pin QFN	260 °C	30 seconds
24-Pin QFN	260 °C	30 seconds
28-Pin SSOP	260 °C	30 seconds
30-Pin WLCSP	260 °C	30 seconds
32-Pin QFN	260 °C	30 seconds
48-Pin QFN	260 °C	30 seconds

Notes

24. $T_J = T_A$ + Power × θ_{JA}.
25. To achieve the thermal impedance specified for the QFN package, refer to "Application Notes for Surface Mount Assembly of Amkor's MicroLeadFrame (Packages available at http://www.cypress.com.
26. Higher temperatures is required based on the solder melting point. Typical temperatures for solder are 220 ±5 °C with Sn-Pb or 245 ± 5 °C with Sn-Ag-Cu paste. Refer to the solder manufacturer specifications.

[+] Feedback

Development Tool Selection

Software

PSoC Designer™

At the core of the PSoC development software suite is PSoC Designer, used to generate PSoC firmware applications. PSoC Designer is available free of charge at http://www.cypress.com and includes a free C compiler.

PSoC Programmer

PSoC Programmer is flexible enough and is used on the bench in development and also suitable for factory programming. PSoC Programmer works either as a standalone programming application or operates directly from PSoC Designer. PSoC Programmer software is compatible with both PSoC ICE Cube In-Circuit Emulator and PSoC MiniProg. PSoC programmer is available free of charge at http://www.cypress.com.

Development Kits

All development kits are sold at the Cypress Online Store.

CY3215-DK Basic Development Kit

The CY3215-DK is for prototyping and development with PSoC Designer. This kit supports in-circuit emulation and the software interface enables users to run, halt, and single step the processor and view the content of specific memory locations. PSoC Designer supports the advance emulation features also. The kit includes:

- PSoC Designer Software CD
- ICE-Cube In-Circuit Emulator
- ICE Flex-Pod for CY8C29x66 Family
- Cat-5 Adapter
- Mini-Eval Programming Board
- 110 ~ 240V Power Supply, Euro-Plug Adapter
- iMAGEcraft C Compiler (Registration Required)
- ISSP Cable
- USB 2.0 Cable and Blue Cat-5 Cable
- 2 CY8C29466-24PXI 28-PDIP Chip Samples

Evaluation Tools

All evaluation tools are sold at the Cypress Online Store.

CY3210-MiniProg1

The CY3210-MiniProg1 kit enables the user to program PSoC devices via the MiniProg1 programming unit. The MiniProg is a small, compact prototyping programmer that connects to the PC via a provided USB 2.0 cable. The kit includes:

- MiniProg Programming Unit
- MiniEval Socket Programming and Evaluation Board
- 28-Pin CY8C29466-24PXI PDIP PSoC Device Sample
- 28-Pin CY8C27443-24PXI PDIP PSoC Device Sample
- PSoC Designer Software CD
- Getting Started Guide
- USB 2.0 Cable

CY3210-PSoCEval1

The CY3210-PSoCEval1 kit features an evaluation board and the MiniProg1 programming unit. The evaluation board includes an LCD module, potentiometer, LEDs, and plenty of bread-boarding space to meet all of your evaluation needs. The kit includes:

- Evaluation Board with LCD Module
- MiniProg Programming Unit
- 28-Pin CY8C29466-24PXI PDIP PSoC Device Sample (2)
- PSoC Designer Software CD
- Getting Started Guide
- USB 2.0 Cable

CY3214-PSoCEvalUSB

The CY3214-PSoCEvalUSB evaluation kit features a development board for the CY8C24794-24LFXI PSoC device. Special features of the board include both USB and capacitive sensing development and debugging support. This evaluation board also includes an LCD module, potentiometer, LEDs, an enunciator and plenty of bread boarding space to meet all of your evaluation needs. The kit includes:

- PSoCEvalUSB Board
- LCD Module
- MIniProg Programming Unit
- Mini USB Cable
- PSoC Designer and Example Projects CD
- Getting Started Guide
- Wire Pack

[+] Feedback

Device Programmers

All device programmers are purchased from the Cypress Online Store.

CY3216 Modular Programmer

The CY3216 Modular Programmer kit features a modular programmer and the MiniProg1 programming unit. The modular programmer includes three programming module cards and supports multiple Cypress products. The kit includes:

- Modular Programmer Base
- 3 Programming Module Cards
- MiniProg Programming Unit
- PSoC Designer Software CD
- Getting Started Guide
- USB 2.0 Cable

CY3207ISSP In-System Serial Programmer (ISSP)

The CY3207ISSP is a production programmer. It includes protection circuitry and an industrial case that is more robust than the MiniProg in a production programming environment. Note that CY3207ISSP needs special software and is not compatible with PSoC Programmer. The kit includes:

- CY3207 Programmer Unit
- PSoC ISSP Software CD
- 110 ~ 240V Power Supply, Euro-Plug Adapter
- USB 2.0 Cable

Accessories (Emulation and Programming)

Table 35. Emulation and Programming Accessories

Part Number	Pin Package	Flex-Pod Kit [27]	Foot Kit [28]	Prototyping Module	Adapter [29]
CY8C20234-12LKXI	16 QFN	Not Available	CY3250-16QFN-FK	CY3210-20X34	Not Available
CY8C20334-12LQXI	24 QFN	CY3250-20334QFN	CY3250-24QFN-FK	CY3210-20X34	AS-24-28-01ML-6
CY8C20634-12FDXI	30 WLCSP	Not Available		CY3210-20X34	Not Available

Notes
27. Dual function Digital I/O Pins also connect to the common analog mux.
28. This part may be used for in-circuit debugging. It is NOT available for production.
29. Programming adapter converts non-DIP package to DIP footprint. Specific details and ordering information for each of the adapters is available at http://www.emulation.com.

[+] Feedback

Ordering Information

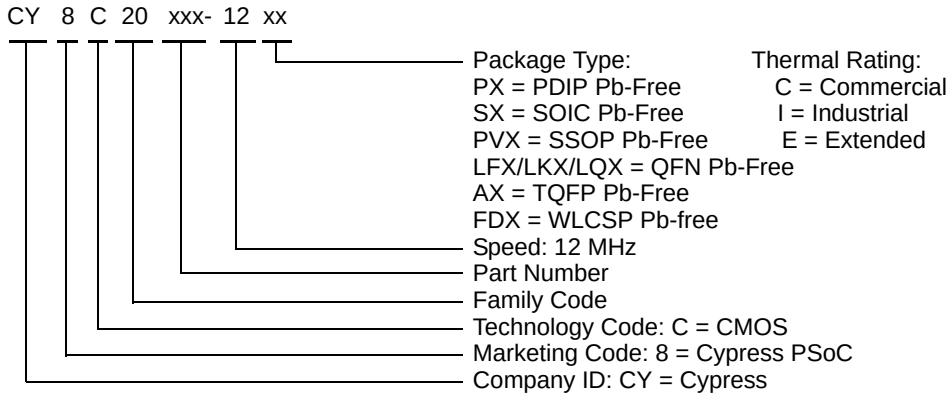
Table 36 lists the CY8C20234, CY8C20334, CY8C20434, CY8C20534, and CY8C20634 PSoC device's key package features and ordering codes.

Table 36. PSoC Device Key Features and Ordering Information

Ordering Code	Package	Flash (Bytes)	SRAM (Bytes)	Digital Blocks	CapSense-Blocks	Digital I/O Pins	Analog Inputs	Analog Outputs	XRES Pin
CY8C20134-12SXI	8-Pin SOIC	8 K	512	0	1	6	6	0	No
CY8C20234-12SXI	16-Pin SOIC	8 K	512	0	1	13	13	0	Yes
CY8C20534-12PVXI	28-Pin SSOP	8 K	512	0	1	24	24[27]	0	Yes
CY8C20534-12PVXIT	28-Pin SSOP	8 K	512	0	1	24	24[27]	0	Yes
CY8C20000-12LFXI	48-Pin OCD QFN[16]	8 K	512	0	1	28	28[27]	0	Yes
CY8C20234-12LKXI	16-Pin (3 × 3 mm 0.60 Max) Sawn QFN	8 K	512	0	1	13	13[27]	0	Yes
CY8C20234-12LKXIT	16-Pin (3 × 3 mm 0.60 Max) Sawn QFN (Tape and Reel)	8 K	512	0	1	13	13[27]	0	Yes
CY8C20334-12LQXI	24-Pin (4 × 4 mm 0.60 Max) Sawn QFN	8 K	512	0	1	20	20[27]	0	Yes
CY8C20334-12LQXIT	24-Pin (4 × 4 mm 0.60 Max) Sawn QFN (Tape and Reel)	8 K	512	0	1	20	20[27]	0	Yes
CY8C20434-12LQXI	32-Pin (5 × 5 mm 0.60 Max) Thin Sawn QFN	8 K	512	0	1	28	28	0	Yes
CY8C20434-12LQXIT	32-Pin (5 × 5 mm 0.60 Max) Thin Sawn QFN (Tape and Reel)	8 K	512	0	1	28	28	0	Yes
CY8C20634-12FDXI	30-Ball WLCSP	8 K	512	0	1	27	27	0	Yes
CY8C20634-12FDXIT	30-Ball WLCSP (Tape and Reel)	8 K	512	0	1	27	27	0	Yes

Note For Die sales information, contact a local Cypress sales office or Field Applications Engineer (FAE).

Ordering Code Definitions



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Acronyms

Acronyms Used

Table 37 lists the acronyms that are used in this document.

Table 37. Acronyms Used in this Datasheet

Acronym	Description	Acronym	Description
AC	alternating current	MIPS	million instructions per second
ADC	analog-to-digital converter	OCD	on-chip debug
API	application programming interface	PCB	printed circuit board
CMOS	complementary metal oxide semiconductor	PGA	programmable gain amplifier
CPU	central processing unit	POR	power on reset
EEPROM	electrically erasable programmable read-only memory	PPOR	precision power on reset
GPIO	general purpose I/O	PSoC®	Programmable System-on-Chip
ICE	in-circuit emulator	PWM	pulse width modulator
IDAC	current DAC	QFN	quad flat no leads
IDE	integrated development environment	SLIMO	slow IMO
ILO	internal low speed oscillator	SPI™	serial peripheral interface
IMO	internal main oscillator	SRAM	static random access memory
I/O	input/output	SROM	supervisory read only memory
ISSP	in-system serial programming	SSOP	shrink small-outline package
LCD	liquid crystal display	USB	universal serial bus
LDO		WDT	watchdog timer
LED	light-emitting diode	WLCSP	wafer level chip scale package
LVD	low voltage detect	XRES	external reset
MCU	microcontroller unit		

Reference Documents

PSoC® CY8C20x34 and PSoC® CY8C20x24 Technical Reference Manual (TRM) – 001-13033

Design Aids – Reading and Writing PSoC® Flash - AN2015 (001-40459)

Adjusting PSoC® Trims for 3.3 V and 2.7 V Operation – AN2012 (001-17397)

Understanding Datasheet Jitter Specifications for Cypress Timing Products – AN5054 (001-14503)

Application Notes for Surface Mount Assembly of Amkor's MicroLeadFrame (MLF) Packages – available at http://www.amkor.com.

[+] Feedback

Document Conventions

Units of Measure

Table 38 lists the unit sof measures.

Table 38. Units of Measure

Symbol	Unit of Measure	Symbol	Unit of Measure
°C	degree Celsius	ms	millisecond
pF	picofarad	ns	nanosecond
kHz	kilohertz	ps	picosecond
MHz	megahertz	µV	microvolts
kΩ	kilohm	mV	millivolts
Ω	ohm	V	volts
µA	microampere	W	watt
mA	milliampere	mm	millimeter
nA	nanoampere	%	percent
µs	microsecond		

Numeric Conventions

Hexadecimal numbers are represented with all letters in uppercase with an appended lowercase ‘h’ (for example, ‘14h’ or ‘3Ah’). Hexadecimal numbers may also be represented by a ‘0x’ prefix, the C coding convention. Binary numbers have an appended lowercase ‘b’ (for example, 01010100b’ or ‘01000011b’). Numbers not indicated by an ‘h’ or ‘b’ are decimals.

Glossary

active high
1. A logic signal having its asserted state as the logic 1 state.
2. A logic signal having the logic 1 state as the higher voltage of the two states.

analog blocks
The basic programmable opamp circuits. These are SC (switched capacitor) and CT (continuous time) blocks. These blocks can be interconnected to provide ADCs, DACs, multi-pole filters, gain stages, and much more.

analog-to-digital (ADC)
A device that changes an analog signal to a digital signal of corresponding magnitude. Typically, an ADC converts a voltage to a digital number. The digital-to-analog (DAC) converter performs the reverse operation.

Application programming interface (API)
A series of software routines that comprise an interface between a computer application and lower level services and functions (for example, user modules and libraries). APIs serve as building blocks for programmers that create software applications.

asynchronous
A signal whose data is acknowledged or acted upon immediately, irrespective of any clock signal.

Bandgap reference
A stable voltage reference design that matches the positive temperature coefficient of VT with the negative temperature coefficient of VBE, to produce a zero temperature coefficient (ideally) reference.

bandwidth
1. The frequency range of a message or information processing system measured in hertz.
2. The width of the spectral region over which an amplifier (or absorber) has substantial gain (or loss); it is sometimes represented more specifically as, for example, full width at half maximum.

bias
1. A systematic deviation of a value from a reference value.
2. The amount by which the average of a set of values departs from a reference value.
3. The electrical, mechanical, magnetic, or other force (field) applied to a device to establish a reference level to operate the device.

[+] Feedback

Glossary

block	1. A functional unit that performs a single function, such as an oscillator. 2. A functional unit that may be configured to perform one of several functions, such as a digital PSoC block or an analog PSoC block.
buffer	1. A storage area for data that is used to compensate for a speed difference, when transferring data from one device to another. Usually refers to an area reserved for IO operations, into which data is read, or from which data is written. 2. A portion of memory set aside to store data, often before it is sent to an external device or as it is received from an external device. 3. An amplifier used to lower the output impedance of a system.
bus	1. A named connection of nets. Bundling nets together in a bus makes it easier to route nets with similar routing patterns. 2. A set of signals performing a common function and carrying similar data. Typically represented using vector notation; for example, address[7:0]. 3. One or more conductors that serve as a common connection for a group of related devices.
clock	The device that generates a periodic signal with a fixed frequency and duty cycle. A clock is sometimes used to synchronize different logic blocks.
comparator	An electronic circuit that produces an output voltage or current whenever two input levels simultaneously satisfy predetermined amplitude requirements.
compiler	A program that translates a high level language, such as C, into machine language.
configuration space	In PSoC devices, the register space accessed when the XIO bit, in the CPU_F register, is set to ‘1’.
crystal oscillator	An oscillator in which the frequency is controlled by a piezoelectric crystal. Typically a piezoelectric crystal is less sensitive to ambient temperature than other circuit components.
cyclic redundancy check (CRC)	A calculation used to detect errors in data communications, typically performed using a linear feedback shift register. Similar calculations may be used for a variety of other purposes such as data compression.
data bus	A bi-directional set of signals used by a computer to convey information from a memory location to the central processing unit and vice versa. More generally, a set of signals used to convey data between digital functions.
debugger	A hardware and software system that allows you to analyze the operation of the system under development. A debugger usually allows the developer to step through the firmware one step at a time, set break points, and analyze memory.
dead band	A period of time when neither of two or more signals are in their active state or in transition.
digital blocks	The 8-bit logic blocks that can act as a counter, timer, serial receiver, serial transmitter, CRC generator, pseudo-random number generator, or SPI.
digital-to-analog (DAC)	A device that changes a digital signal to an analog signal of corresponding magnitude. The analog-to-digital (ADC) converter performs the reverse operation.
duty cycle	The relationship of a clock period high time to its low time, expressed as a percent.

[+] Feedback

Glossary

emulator	Duplicates (provides an emulation of) the functions of one system with a different system, so that the second system appears to behave like the first system.
External Reset (XRES)	An active high signal that is driven into the PSoC device. It causes all operation of the CPU and blocks to stop and return to a pre-defined state.
Flash	An electrically programmable and erasable, non-volatile technology that provides you the programmability and data storage of EPROMs, plus in-system erasability. Non-volatile means that the data is retained when power is OFF.
Flash block	The smallest amount of Flash ROM space that may be programmed at one time and the smallest amount of Flash space that may be protected. A Flash block holds 64 bytes.
frequency	The number of cycles or events per unit of time, for a periodic function.
gain	The ratio of output current, voltage, or power to input current, voltage, or power, respectively. Gain is usually expressed in dB.
I^2C	A two-wire serial computer bus by Philips Semiconductors (now NXP Semiconductors). I2C is an Inter-Integrated Circuit. It is used to connect low-speed peripherals in an embedded system. The original system was created in the early 1980s as a battery control interface, but it was later used as a simple internal bus system for building control electronics. I2C uses only two bi-directional pins, clock and data, both running at +5V and pulled high with resistors. The bus operates at 100 kbits/second in standard mode and 400 kbits/second in fast mode.
ICE	The in-circuit emulator that allows you to test the project in a hardware environment, while viewing the debugging device activity in a software environment (PSoC Designer).
input/output (I/O)	A device that introduces data into or extracts data from a system.
interrupt	A suspension of a process, such as the execution of a computer program, caused by an event external to that process, and performed in such a way that the process can be resumed.
interrupt service routine (ISR)	A block of code that normal code execution is diverted to when the M8C receives a hardware interrupt. Many interrupt sources may each exist with its own priority and individual ISR code block. Each ISR code block ends with the RETI instruction, returning the device to the point in the program where it left normal program execution.
jitter	1. A misplacement of the timing of a transition from its ideal position. A typical form of corruption that occurs on serial data streams. 2. The abrupt and unwanted variations of one or more signal characteristics, such as the interval between successive pulses, the amplitude of successive cycles, or the frequency or phase of successive cycles.
low-voltage detect (LVD)	A circuit that senses V_{DD} and provides an interrupt to the system when V_{DD} falls lower than a selected threshold.
M8C	An 8-bit Harvard-architecture microprocessor. The microprocessor coordinates all activity inside a PSoC by interfacing to the Flash, SRAM, and register space.
master device	A device that controls the timing for data exchanges between two devices. Or when devices are cascaded in width, the master device is the one that controls the timing for data exchanges between the cascaded devices and an external interface. The controlled device is called the ***slave device*.**

[+] Feedback

Glossary

microcontroller	An integrated circuit chip that is designed primarily for control systems and products. In addition to a CPU, a microcontroller typically includes memory, timing circuits, and IO circuitry. The reason for this is to permit the realization of a controller with a minimal quantity of chips, thus achieving maximal possible miniaturization. This in turn, reduces the volume and the cost of the controller. The microcontroller is normally not used for general-purpose computation as is a microprocessor.
mixed-signal	The reference to a circuit containing both analog and digital techniques and components.
modulator	A device that imposes a signal on a carrier.
noise	1. A disturbance that affects a signal and that may distort the information carried by the signal. 2. The random variations of one or more characteristics of any entity such as voltage, current, or data.
oscillator	A circuit that may be crystal controlled and is used to generate a clock frequency.
parity	A technique for testing transmitting data. Typically, a binary digit is added to the data to make the sum of all the digits of the binary data either always even (even parity) or always odd (odd parity).
Phase-locked loop (PLL)	An electronic circuit that controls an ***oscillator*** so that it maintains a constant phase angle relative to a reference signal.
pinouts	The pin number assignment: the relation between the logical inputs and outputs of the PSoC device and their physical counterparts in the printed circuit board (PCB) package. Pinouts involve pin numbers as a link between schematic and PCB design (both being computer generated files) and may also involve pin names.
port	A group of pins, usually eight.
Power on reset (POR)	A circuit that forces the PSoC device to reset when the voltage is lower than a pre-set level. This is a type of hardware reset.
PSoC®	Cypress Semiconductor's PSoC® is a registered trademark and Programmable System-on-Chip™ is a trademark of Cypress.
PSoC Designer™	The software for Cypress' Programmable System-on-Chip technology.
pulse width modulator (PWM)	An output in the form of duty cycle which varies as a function of the applied measurand
RAM	An acronym for random access memory. A data-storage device from which data can be read out and new data can be written in.
register	A storage device with a specific capacity, such as a bit or byte.
reset	A means of bringing a system back to a know state. See hardware reset and software reset.
ROM	An acronym for read only memory. A data-storage device from which data can be read out, but new data cannot be written in.
serial	1. Pertaining to a process in which all events occur one after the other. 2. Pertaining to the sequential or consecutive occurrence of two or more related activities in a single device or channel.

[+] Feedback

Glossary

settling time	The time it takes for an output signal or value to stabilize after the input has changed from one value to another.
shift register	A memory storage device that sequentially shifts a word either left or right to output a stream of serial data.
slave device	A device that allows another device to control the timing for data exchanges between two devices. Or when devices are cascaded in width, the slave device is the one that allows another device to control the timing of data exchanges between the cascaded devices and an external interface. The controlling device is called the master device.
SRAM	An acronym for static random access memory. A memory device where you can store and retrieve data at a high rate of speed. The term static is used because, after a value is loaded into an SRAM cell, it remains unchanged until it is explicitly altered or until power is removed from the device.
SROM	An acronym for supervisory read only memory. The SROM holds code that is used to boot the device, calibrate circuitry, and perform Flash operations. The functions of the SROM may be accessed in normal user code, operating from Flash.
stop bit	A signal following a character or block that prepares the receiving device to receive the next character or block.
synchronous	1. A signal whose data is not acknowledged or acted upon until the next active edge of a clock signal. 2. A system whose operation is synchronized by a clock signal.
tri-state	A function whose output can adopt three states: 0, 1, and Z (high-impedance). The function does not drive any value in the Z state and, in many respects, may be considered to be disconnected from the rest of the circuit, allowing another output to drive the same net.
UART	A UART or universal asynchronous receiver-transmitter translates between parallel bits of data and serial bits.
user modules	Pre-build, pre-tested hardware/firmware peripheral functions that take care of managing and configuring the lower level Analog and Digital PSoC Blocks. User Modules also provide high level ***API (Application Programming Interface)*** for the peripheral function.
user space	The bank 0 space of the register map. The registers in this bank are more likely to be modified during normal program execution and not just during initialization. Registers in bank 1 are most likely to be modified only during the initialization phase of the program.
V_{DD}	A name for a power net meaning "voltage drain." The most positive power supply signal. Usually 5 V or 3.3 V.
V_{SS}	A name for a power net meaning "voltage source." The most negative power supply signal.
watchdog timer	A timer that must be serviced periodically. If it is not serviced, the CPU resets after a specified period of time.

[+] Feedback

Document History Page

Document Title: CY8C20134, CY8C20234, CY8C20334, CY8C20434, CY8C20534, CY8C20634 PSoC® Programmable System-on-Chip™ Document Number: 001-05356				
Revision	**ECN**	**Orig. of Change**	**Submission Date**	**Description of Change**
**	404571	HMT	See ECN	New silicon and document (Revision **).
*A	418513	HMT	See ECN	Updated Electrical Specifications, including Storage Temperature and Maximum Input Clock Frequency. Updated Features and Analog System Overview. Modified 32-pin QFN E-PAD dimensions. Added new 32-pin QFN. Add High Output Drive indicator to all P1[x] pinouts. Updated trademarks.
*B	490071	HMT	See ECN	Made datasheet “Final”. Added new Development Tool section. Added OCD pinout and package diagram. Added 16-pin QFN. Updated 24-pin and 32-pin QFN package diagrams to 0.60 max thickness. Changed from commercial to industrial temperature range. Updated Storage Temperature specification and notes. Updated thermal resistance data. Added development tool kit part numbers. Finetuned features and electrical specifications.
*C	788177	HMT	See ECN	Added CapSense SNR requirement reference. Added Low Power Comparator (LPC) AC/DC electrical specifications tables. Added 2.7V minimum specifications. Updated figure standards. Updated Technical Training paragraph. Added QFN package clarifications and dimensions. Updated ECN-ed Amkor dimensioned QFN package diagram revisions.
*D	1356805	HMT/SFVTM P3/HCL/SFV	See ECN	Updated 24-pin QFN Theta JA. Added External Reset Pulse Width, TXRST, specification. Fixed 48-pin QFN.vsd. Updated the table introduction and high output voltage description in section two. The sentence: "Exceeding maximum ratings may shorten the battery life of the device.” does not apply to all datasheets. Therefore, the word "battery" is changed to "useful.” Took out tabs after table and figure numbers in titles and added two hard spaces. Updated the section, DC GPIO Specifications on page 18 with new text. Updated VOH5 and VOH6 to say, ”High Output Voltage, Port 1 Pins with 3.0V LDO Regulator Enabled.” Updated VOH7 and VOH8 with the text, “maximum of 20 mA source current in all I/Os.”Added 28-pin SSOP part, pinout, package. Updated specs. Modified dev. tool part numbers.
*E	2197347	UVS/AESA	See ECN	Added 32-pin Sawn QFN Pin diagram Removed package diagram: 32-Pin (5 × 5 mm) SAWN QFN(001-42168 *A) Updated Ordering Information table with CY8C20434-12LQXI and CY8C20434-12LQXIT ordering details. Corrected Table 16. DC Programming Specifications - Included above the table "Flash Endurance and Retention specifications with the use of the EEPROM User Module are valid only within the range: 25 °C +/-20C during the Flash Write operation. Refer the EEPROM User Module datasheet instructions for EEPROM Flash Write requirements outside of the 25 °C +/-20 °C temperature window."
*F	2542938	RLRM/AESA	07/30/2008	Corrected Ordering Information format. Updated package diagrams 001-13937 and 001-30999. Updated datasheet template. Corrected Figure 6 (28-pin diagram).
*G	2610469	SNV/PYRS	11/20/08	Updated V_{OH5}, V_{OH7}, and V_{OH9} specifications
*H	2693024	DPT/PYRS	04/16/2009	Changed title from PSoC® Mixed Signal Array to PSoC® Programmable System-on-Chip™ Replaced package outline drawing for 32-Pin Sawn QFN Updated “Development Tool Selection” on page 36 Updated “Development Tools” on page 5 and “Designing with PSoC Designer” on page 6 Updated “Getting Started” on page 5
*I	2717566	DRSW/AESA	06/11/2009	Updated AC Chip-Level, and AC Programming Specifications as follows: Modified F_{IMO6} (page 20), T_{WRITE} specifications (page 23) Added I_{OH}, I_{OL} (page 17), Flash endurance note (page 19), DCILO (page 20), F32K_U (page 20), $T_{POWERUP}$ (page 20), $T_{ERASEALL}$ (page 23), $T_{PROGRAM_HOT}$ (page 24), and $T_{PROGRAM_COLD}$ (page 24) specifications Added AC SPI Master and Slave Specifications Added 30-Ball WLCSP Package

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Document History Page

Document Title: CY8C20134, CY8C20234, CY8C20334, CY8C20434, CY8C20534, CY8C20634 PSoC® Programmable System-on-Chip™ Document Number: 001-05356				
Revision	**ECN**	**Orig. of Change**	**Submission Date**	**Description of Change**
*J	2825336	ISW	12/10/2009	Updated pin description table for 48-pin OCD. Updated Ordering information table to include CY8C20534-12PVXA parts. Updated package diagrams for 48-pin QFN, 16-pin QFN (sawn), 24-pin QFN (sawn), and 30-ball WLCSP specs.
*K	2892629	NJF	03/15/2010	Updated Programmable pin configuration details in Features. Updated Analog Multiplexer System. Updated Cypress website links. Updated PSoC Designer Software Subsystems. Added $T_{BAKETEMP}$ and $T_{BAKETIME}$ parameters in Absolute Maximum Ratings. Removed the following sections: DC Low Power Comparator Specifications, AC Analog Mux Bus Specifications, AC Low Power Comparator Specifications, Third Party Tools, and Build a PSoC Emulator into your Board. Modified Notes in Packaging Dimensions. Updated Ordering Code Definitions. Removed inactive parts from Ordering Information. Updated links in Sales, Solutions, and Legal Information.
*L	2872902	VMAD	04/06/10	Added part number CY8C20134 to the title. Added 8-pin and 16-pin SOIC pin and package details. Updated content to match current style guide and datasheet template. Moved acronyms and units of measure tables to page 35.
*M	3043170	NJF	09/30/10	Added PSoC Device Characteristics table . Added DC I^2C Specifications table. Added F_{32K_U} max limit. Added Tjit_IMO specification, removed existing jitter specifications. Updated Units of Measure, Acronyms, Glossary, and References sections. Updated solder reflow specifications. No specific changed were made to I^2C Timing Diagram. Updated for clearer understanding. Template and styles update.
*N	3173718	NJF	02/16/11	CY8C20134-12SX1I and CY8C20234-12SX2I typo error fixed in the ordering information table and changed in to CY8C20134-12SXI and CY8C20234-12SXI. Updated document version and date. Updated package diagram to 001-12919 *C.
*O	3248613	TOF	06/10/11	Under Table 13, the text "Table 13 lists the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C, 3.0 V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C, or 2.4 V to 3.0 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters apply to 5 V, 3.3 V, and 2.7 V at 25 °C. These are for design guidance only." changed to "Table 13 lists the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C, 3.0 V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C, or Table 14 for 2.4 V to 3.0 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters apply to 5 V, 3.3 V, and 2.7 V at 25 °C. These are for design guidance only". Updated Table 34 on page 35 table. Updated sections, "Getting Started", "Development Tools", and "Designing with PSoC Designer" to remove references to the system level designs. Updated package diagram 51-85066 to *E revision.

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