

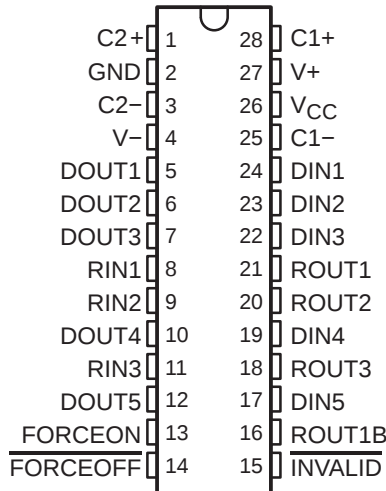
SN65C3238, SN75C3238

3-V TO 5.5-V MULTICHANNEL RS-232 COMPATIBLE LINE DRIVER/RECEIVER

SLLS352F – JUNE 1999 – REVISED OCTOBER 2004

- Auto-powerdown Plus
- Operate With 3-V to 5.5-V V_{CC} Supply
- Always-Active Noninverting Receiver Output (ROUT1B)
- Support Operation From 250 kbit/s to 1 Mbit/s
- Low Standby Current . . . 1 μ A Typ
- External Capacitors . . . $4 \times 0.1 \mu$ F
- Accept 5-V Logic Input With 3.3-V Supply
- Inter-Operable With SN65C3243, SN75C3243
- RS-232 Bus-Pin ESD Protection Exceeds ± 15 -kV Using Human-Body Model (HBM)
- Applications
 - Battery-Powered Systems, PDAs, Notebooks, Sub-Notebooks, Laptops, Palmtop PCs, Hand-Held Equipment, Modems, and Printers

DB, DW, OR PW PACKAGE
(TOP VIEW)



description/ordering information

The 'C3238 devices consist of five line drivers, three line receivers, and a dual charge-pump circuit with ± 15 -kV ESD protection pin to pin (serial-port connection pins, including GND). The charge pump and four small external capacitors allow operation from a single 3-V to 5.5-V supply. In addition, these devices include an always-active noninverting output (ROUT1B), which allows applications using the ring indicator to transmit data while the device is powered down. These devices operate at data signaling rates up to 1 Mbit/s and at an increased slew-rate range of 24 V/ μ s to 150 V/ μ s.

ORDERING INFORMATION

T_A	PACKAGE [†]		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–0°C to 70°C	SOIC (DW)	Tube of 20	SN75C3238DW	75C3238
		Reel of 1000	SN75C3238DWR	
	SSOP (DB)	Reel of 2000	SN75C3238DBR	75C3238
	TSSOP (PW)	Tube of 50	SN75C3238PW	CA3238
		Reel of 2000	SN75C3238PWR	
–40°C to 85°C	SOIC (DW)	Tube of 20	SN65C3238DW	65C3238
		Reel of 1000	SN65C3238DWR	
	SSOP (DB)	Reel of 2000	SN65C3238DBR	65C3238
	TSSOP (PW)	Tube of 50	SN65C3238PW	CB3238
		Reel of 2000	SN65C3238PWR	

[†] Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

 **TEXAS
INSTRUMENTS**

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description/ordering information (continued)

Flexible control options for power management are featured when the serial-port and driver inputs are inactive. The auto-powerdown plus feature functions when **FORCEON** is low and **FORCEOFF** is high. During this mode of operation, if the device does not sense valid signal transitions on all receiver and driver inputs for 30 s, the built-in charge-pump and drivers are powered down, reducing the supply current to 1 μ A. By disconnecting the serial port or placing the peripheral drivers off, auto-powerdown plus will occur if there is no activity in the logic levels for the driver inputs. Auto-powerdown plus can be disabled when **FORCEON** and **FORCEOFF** are high. With auto-powerdown plus enabled, the device automatically activates once a valid signal is applied to any receiver or driver input. **INVALID** is high (valid data) if any receiver input voltage is greater than 2.7 V or less than -2.7 V or has been between -0.3 V and 0.3 V for less than 30 μ s. **INVALID** is low (invalid data) if all receiver input voltages are between -0.3 V and 0.3 V for more than 30 μ s. Refer to Figure 5 for receiver input levels.

Function Tables

EACH DRIVER

INPUTS				OUTPUT	DRIVER STATUS
DIN	FORCEON	FORCEOFF	TIME ELAPSED SINCE LAST RIN OR DIN TRANSITION	DOUT	
X	X	L	X	Z	Powered off
L	H	H	X	H	Normal operation with auto-powerdown plus disabled
H	H	H	X	L	
L	L	H	<30 s	H	Normal operation with auto-powerdown plus enabled
H	L	H	<30 s	L	
L	L	H	>30 s	Z	Powered off by auto-powerdown plus feature
H	L	H	>30 s	Z	

H = high level, L = low level, X = irrelevant, Z = high impedance

EACH RECEIVER

INPUTS				OUTPUTS		RECEIVER STATUS
RIN2	RIN1, RIN3-RIN5	FORCEOFF	TIME ELAPSED SINCE LAST RIN OR DIN TRANSITION	ROUT1B	ROUT	
L	X	L	X	L	Z	Powered off while ROUT1B is active
H	X	L	X	H	Z	
L	L	H	<30 s	L	H	Normal operation with auto-powerdown plus disabled/enabled
L	H	H	<30 s	L	L	
H	L	H	<30 s	H	H	
H	H	H	<30 s	H	L	
Open	Open	H	>30 s	L	H	

H = high level, L = low level, X = irrelevant, Z = high impedance (off), Open = input disconnected or connected driver off

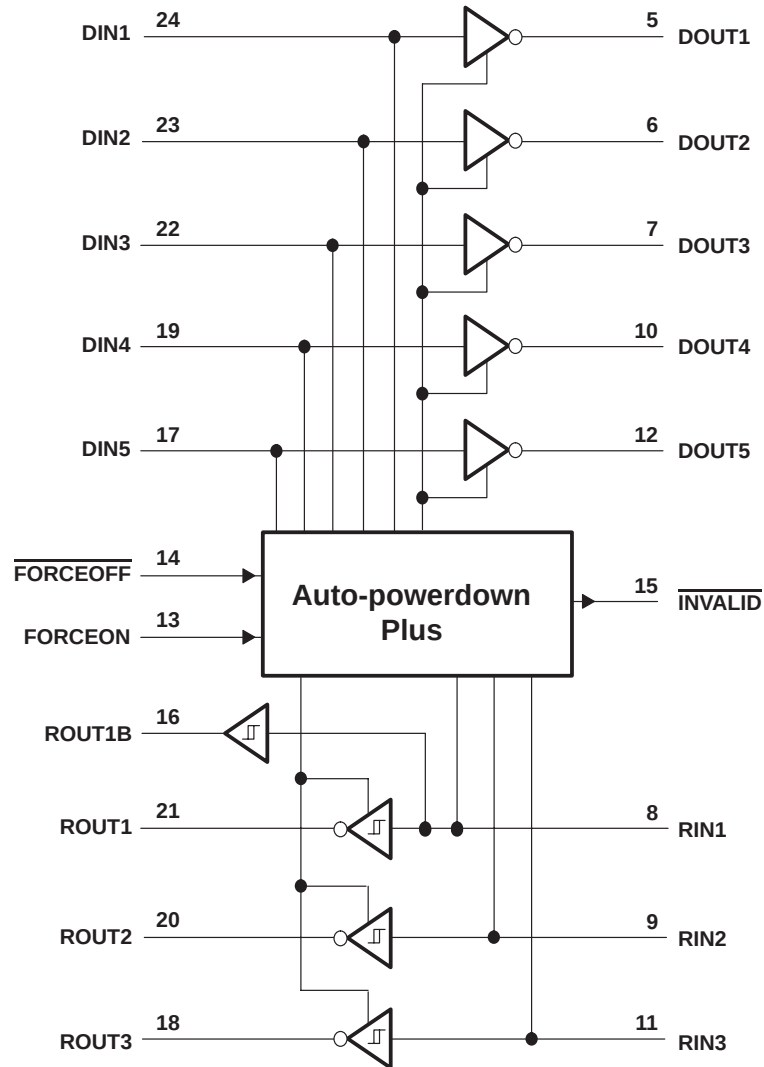


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logic diagram (positive logic)



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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V_{CC} (see Note 1)	–0.3 V to 6 V
Positive output supply voltage range, $V+$ (see Note 1)	–0.3 V to 7 V
Negative output supply voltage range, $V-$ (see Note 1)	0.3 V to –7 V
Supply voltage difference, $V+ - V-$ (see Note 1)	13 V
Input voltage range, V_I : Driver ($\overline{\text{FORCEOFF}}$, FORCEON)	–0.3 V to 6 V
Receiver	–25 V to 25 V
Output voltage range, V_O : Driver	–13.2 V to 13.2 V
Receiver (INVALID)	–0.3 V to $V_{CC} + 0.3$ V
Package thermal impedance, θ_{JA} (see Notes 2 and 3): DB package	62°C/W
DW package	46°C/W
PW package	62°C/W
Operating virtual junction temperature, T_J	150°C
Storage temperature range, T_{stg}	–65°C to 150°C

[†] Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltages are with respect to network GND.

2. Maximum power dissipation is a function of $T_J(\text{max})$, θ_{JA} , and T_A . The maximum allowable power dissipation at any allowable ambient temperature is $P_D = (T_J(\text{max}) - T_A)/\theta_{JA}$. Operating at the absolute maximum T_J of 150°C can affect reliability.

3. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Note 4 and Figure 6)

				MIN	NOM	MAX	UNIT
Supply voltage		$V_{CC} = 3.3$ V		3	3.3	3.6	V
		$V_{CC} = 5$ V		4.5	5	5.5	
V_{IH}	Driver and control high-level input voltage	DIN, $\overline{\text{FORCEOFF}}$, FORCEON	$V_{CC} = 3.3$ V	2			V
			$V_{CC} = 5$ V	2.4			
V_{IL}	Driver and control low-level input voltage	DIN, $\overline{\text{FORCEOFF}}$, FORCEON				0.8	V
V_I	Driver and control input voltage	DIN, $\overline{\text{FORCEOFF}}$, FORCEON		0		5.5	V
V_I	Receiver input voltage			–25		25	V
T_A	Operating free-air temperature	SN75C3238		0		70	°C
		SN65C3238		–40		85	

NOTE 4: Testing supply conditions are C1–C4 = 0.1 μ F at $V_{CC} = 3.3$ V $\pm$ 0.15 V; C1–C4 = 0.22 μ F at $V_{CC} = 3.3$ V $\pm$ 0.3 V; and C1 = 0.047 μ F and C2–C4 = 0.33 μ F at $V_{CC} = 5$ V $\pm$ 0.5 V.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Note 4 and Figure 6)

PARAMETER		TEST CONDITIONS	MIN	TYP [‡]	MAX	UNIT
I_I	Input leakage current	$\overline{\text{FORCEOFF}}$, FORCEON		± 0.01	± 1	μ A
I_{CC}	Supply current	Auto-powerdown plus disabled	No load, $\overline{\text{FORCEOFF}}$ and FORCEON at V_{CC}	0.5	2	mA
		Powered off	No load, $\overline{\text{FORCEOFF}}$ at GND	1	10	
		Auto-powerdown plus enabled	No load, $\overline{\text{FORCEOFF}}$ at V_{CC} , FORCEON at GND, All RIN are open or grounded	1	10	μ A

[‡] All typical values are at $V_{CC} = 3.3$ V or $V_{CC} = 5$ V, and $T_A = 25^\circ\text{C}$.

NOTE 4: Testing supply conditions are C1–C4 = 0.1 μ F at $V_{CC} = 3.3$ V $\pm$ 0.15 V; C1–C4 = 0.22 μ F at $V_{CC} = 3.3$ V $\pm$ 0.3 V; and C1 = 0.047 μ F and C2–C4 = 0.33 μ F at $V_{CC} = 5$ V $\pm$ 0.5 V.



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DRIVER SECTION

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Note 4 and Figure 6)

PARAMETER	TEST CONDITIONS	MIN	TYP [†]	MAX	UNIT
V _{OH} High-level output voltage	All DOUT at R _L = 3 kΩ to GND	5	5.4		V
V _{OL} Low-level output voltage	All DOUT at R _L = 3 kΩ to GND	–5	–5.4		V
I _{IH} High-level input current	V _I = V _{CC}		±0.01	±1	μA
I _{IL} Low-level input current	V _I at GND		±0.01	±1	μA
I _{OS} Short-circuit output current [‡]	V _{CC} = 3.6 V, V _O = 0 V		±35	±60	mA
	V _{CC} = 5.5 V, V _O = 0 V		±40	±90	
r _o Output resistance	V _{CC} , V ₊ , and V _– = 0 V, V _O = ±2 V	300	10M		Ω
I _{off} Output leakage current	FORCEOFF = GND, V _O = ±12 V, V _{CC} = 3 V to 3.6 V			±25	μA
	V _O = ±10 V, V _{CC} = 4.5 V to 5.5 V			±25	

[†] All typical values are at V_{CC} = 3.3 V or V_{CC} = 5 V, and T_A = 25°C.

[‡] Short-circuit durations should be controlled to prevent exceeding the device absolute power-dissipation ratings, and not more than one output should be shorted at a time.

NOTE 4: Testing supply conditions are C1–C4 = 0.1 μF at V_{CC} = 3.3 V ± 0.15 V; C1–C4 = 0.22 μF at V_{CC} = 3.3 V ± 0.3 V; and C1 = 0.047 μF and C2–C4 = 0.33 μF at V_{CC} = 5 V ± 0.5 V.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Note 4 and Figure 6)

PARAMETER	TEST CONDITIONS	MIN	TYP [†]	MAX	UNIT
Maximum data rate (see Figure 1)	R _L = 3 kΩ, One DOUT switching	C _L = 1000 pF	250		kbit/s
		C _L = 250 pF, V _{CC} = 3 V to 4.5 V	1000		
		C _L = 1000 pF, V _{CC} = 4.5 V to 5.5 V	1000		
t _{sk(p)} Pulse skew [§]	C _L = 150 pF to 2500 pF, R _L = 3 kΩ to 7 kΩ, See Figure 2		25		ns
SR(tr) Slew rate, transition region (see Figure 1)	C _L = 150 pF to 1000 pF, R _L = 3 kΩ to 7 kΩ, V _{CC} = 3.3 V	18		150	V/μs

[†] All typical values are at V_{CC} = 3.3 V or V_{CC} = 5 V, and T_A = 25°C.

[§] Pulse skew is defined as |t_{PLH} – t_{PHL}| of each channel of the same device.

NOTE 4: Testing supply conditions are C1–C4 = 0.1 μF at V_{CC} = 3.3 V ± 0.15 V; C1–C4 = 0.22 μF at V_{CC} = 3.3 V ± 0.3 V; and C1 = 0.047 μF and C2–C4 = 0.33 μF at V_{CC} = 5 V ± 0.5 V.



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RECEIVER SECTION

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Note 4 and Figure 6)

PARAMETER	TEST CONDITIONS	MIN	TYP [†]	MAX	UNIT
V _{OH} High-level output voltage	I _{OH} = -1 mA	V _{CC} - 0.6 V	V _{CC} - 0.1 V		V
V _{OL} Low-level output voltage	I _{OL} = 1.6 mA			0.4	V
V _{IT+} Positive-going input threshold voltage	V _{CC} = 3.3 V		1.5	2.4	V
	V _{CC} = 5 V		1.8	2.4	
V _{IT-} Negative-going input threshold voltage	V _{CC} = 3.3 V	0.6	1.2		V
	V _{CC} = 5 V	0.8	1.5		
V _{hys} Input hysteresis (V _{IT+} - V _{IT-})			0.3		V
I _{off} Output leakage current (except ROUT1B)	FORCEOFF = 0 V		±0.05	±10	μA
r _i Input resistance	V _I = ±3 V to ±25 V	3	5	7	kΩ

[†] All typical values are at V_{CC} = 3.3 V or V_{CC} = 5 V, and T_A = 25°C.

NOTE 4: Testing supply conditions are C1–C4 = 0.1 μF at V_{CC} = 3.3 V ± 0.15 V; C1–C4 = 0.22 μF at V_{CC} = 3.3 V ± 0.3 V; and C1 = 0.047 μF and C2–C4 = 0.33 μF at V_{CC} = 5 V ± 0.5 V.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Note 4)

PARAMETER	TEST CONDITIONS	MIN	TYP [†]	MAX	UNIT
t _{pLH} Propagation delay time, low- to high-level output	C _L = 150 pF, See Figure 3		150		ns
t _{pHL} Propagation delay time, high- to low-level output			150		ns
t _{en} Output enable time	C _L = 150 pF, R _L = 3 kΩ, See Figure 4		200		ns
t _{dis} Output disable time			200		ns
t _{sk(p)} Pulse skew [‡]	See Figure 3		50		ns

[†] All typical values are at V_{CC} = 3.3 V or V_{CC} = 5 V, and T_A = 25°C.

[‡] Pulse skew is defined as |t_{pLH} - t_{pHL}| of each channel of the same device.

NOTE 4: Testing supply conditions are C1–C4 = 0.1 μF at V_{CC} = 3.3 V ± 0.15 V; C1–C4 = 0.22 μF at V_{CC} = 3.3 V ± 0.3 V; and C1 = 0.047 μF and C2–C4 = 0.33 μF at V_{CC} = 5 V ± 0.5 V.

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AUTO-POWERDOWN PLUS SECTION

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 5)

PARAMETER	TEST CONDITIONS	MIN	TYP [†]	MAX	UNIT
V _{T+(valid)}	Receiver input threshold for INVALID high-level output voltage FORCEON = GND, FORCEOFF = V _{CC}			2.7	V
V _{T-(valid)}	Receiver input threshold for INVALID high-level output voltage FORCEON = GND, FORCEOFF = V _{CC}	-2.7			V
V _{T(invalid)}	Receiver input threshold for INVALID low-level output voltage FORCEON = GND, FORCEOFF = V _{CC}	-0.3		0.3	V
V _{OH}	INVALID high-level output voltage I _{OH} = -1 mA, FORCEON = GND, FORCEOFF = V _{CC}	V _{CC} - 0.6			V
V _{OL}	INVALID low-level output voltage I _{OL} = 1.6 mA, FORCEON = GND, FORCEOFF = V _{CC}			0.4	V

[†] All typical values are at V_{CC} = 3.3 V or V_{CC} = 5 V, and T_A = 25°C.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 5)

PARAMETER		MIN	TYP†	MAX	UNIT
tvalid	Propagation delay time, low- to high-level output		0.1		μs
tinvalid	Propagation delay time, high- to low-level output		50		μs
ten	Supply enable time		25		μs
tdis	Receiver or driver edge to auto-powerdown plus	15	30	60	s

[†] All typical values are at V_{CC} = 3.3 V or V_{CC} = 5 V, and T_A = 25°C.

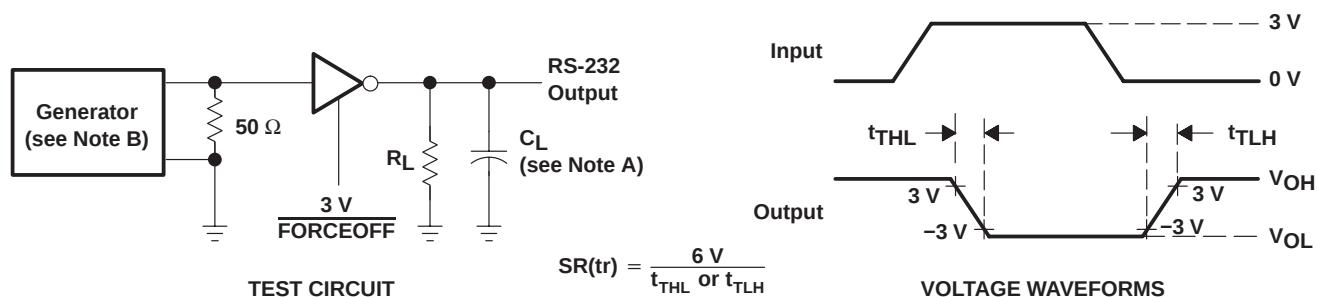


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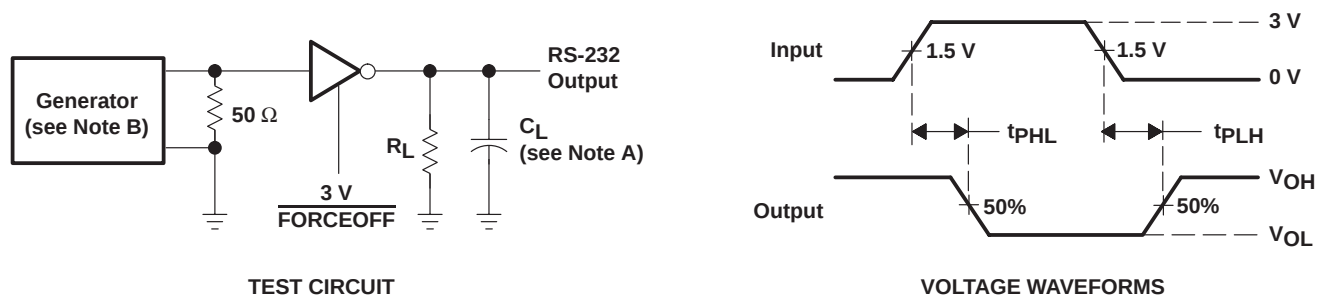
PARAMETER MEASUREMENT INFORMATION



NOTES: A. C_L includes probe and jig capacitance.

B. The pulse generator has the following characteristics: PRR = 1 Mbit/s, $Z_O = 50\ \Omega$, 50% duty cycle, $t_r \leq 10\text{ ns}$, $t_f \leq 10\text{ ns}$.

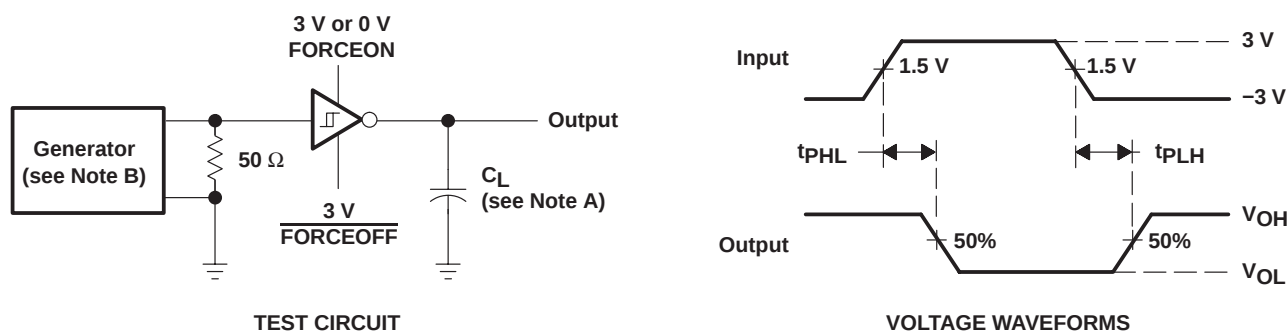
Figure 1. Driver Slew Rate



NOTES: A. C_L includes probe and jig capacitance.

B. The pulse generator has the following characteristics: PRR = 1 Mbit/s, $Z_O = 50\ \Omega$, 50% duty cycle, $t_r \leq 10\text{ ns}$, $t_f \leq 10\text{ ns}$.

Figure 2. Driver Pulse Skew



NOTES: A. C_L includes probe and jig capacitance.

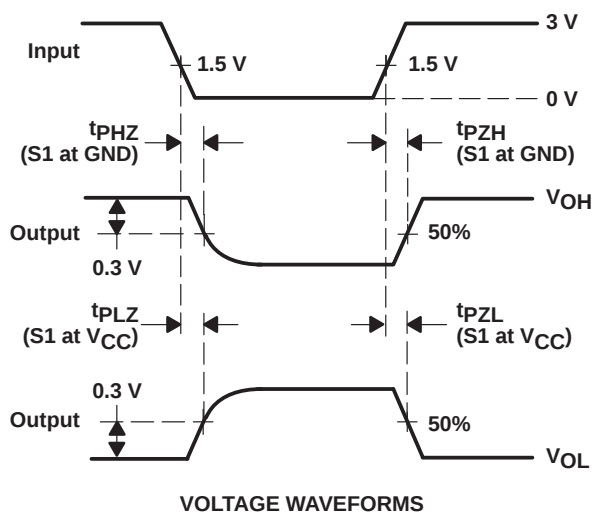
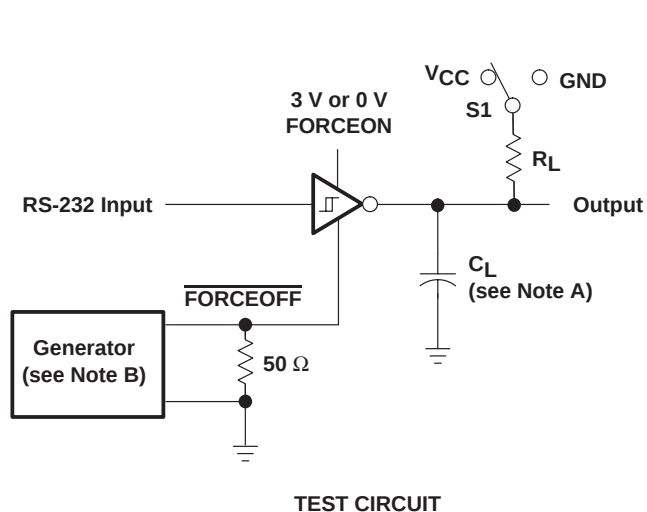
B. The pulse generator has the following characteristics: $Z_O = 50\ \Omega$, 50% duty cycle, $t_r \leq 10\text{ ns}$, $t_f \leq 10\text{ ns}$.

Figure 3. Receiver Propagation Delay Times

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PARAMETER MEASUREMENT INFORMATION



- NOTES: A. C_L includes probe and jig capacitance.
 B. The pulse generator has the following characteristics: $Z_O = 50\ \Omega$, 50% duty cycle, $t_r \leq 10\text{ ns}$, $t_f \leq 10\text{ ns}$.
 C. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 D. t_{PZL} and t_{PZH} are the same as t_{en} .

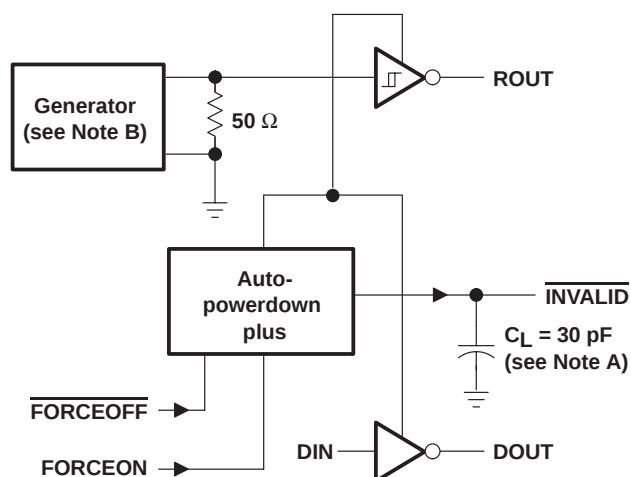
Figure 4. Receiver Enable and Disable Times

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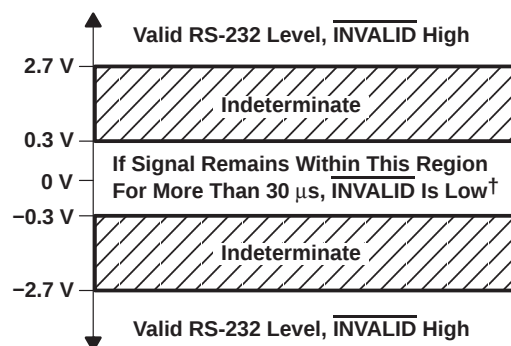
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PARAMETER MEASUREMENT INFORMATION

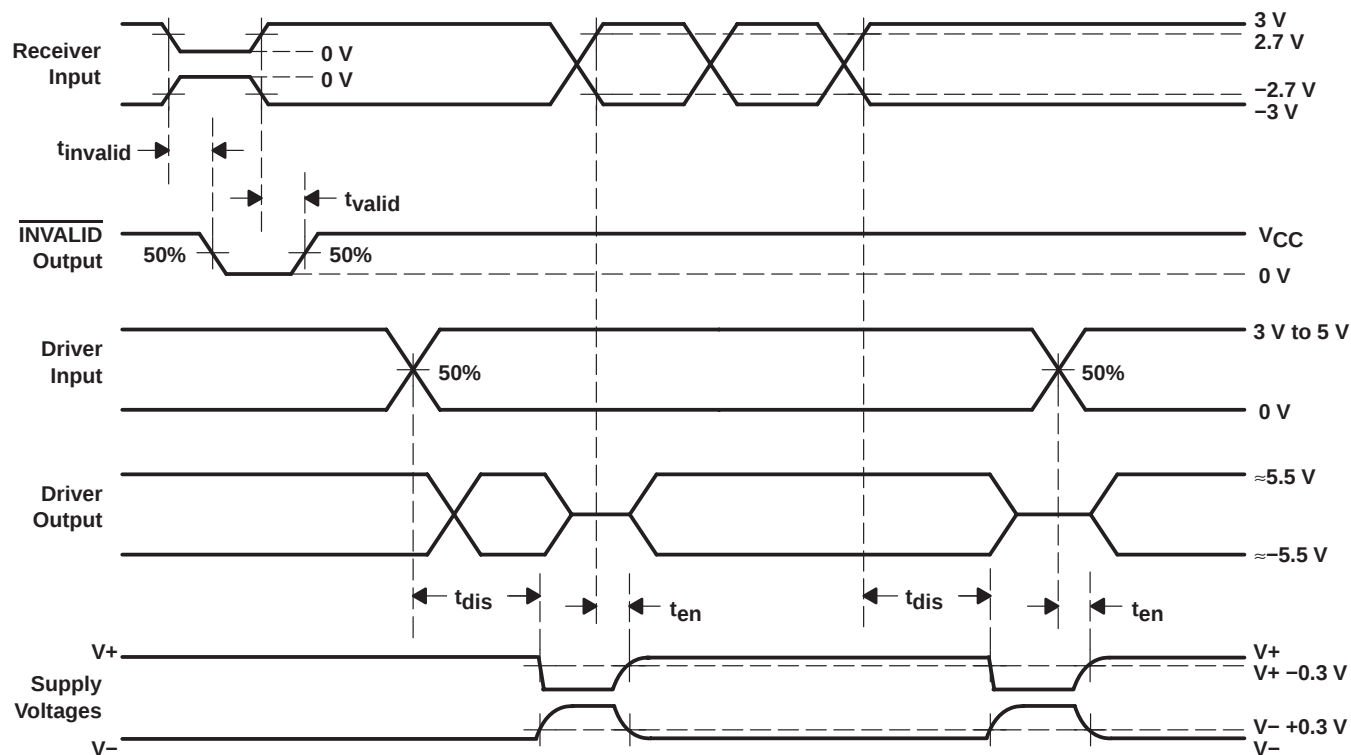


TEST CIRCUIT

- NOTES: A. C_L includes probe and jig capacitance.
B. The pulse generator has the following characteristics: PRR = 5 kbit/s, $Z_O = 50 \Omega$, 50% duty cycle, $t_r \leq 10$ ns, $t_f \leq 10$ ns.



† Auto-powerdown plus disables drivers and reduces supply current to 1 μ A.



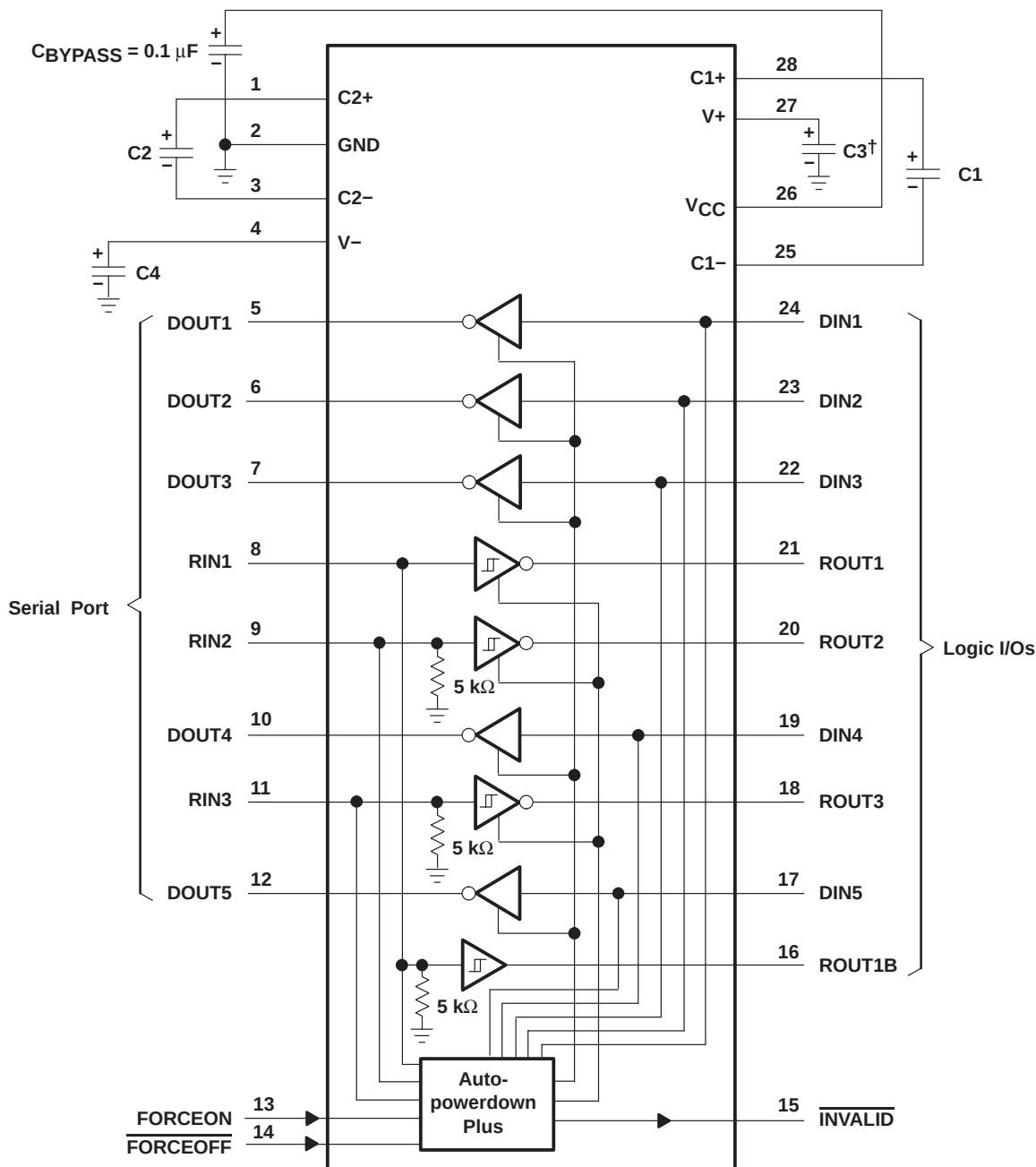
Voltage Waveforms and Timing Diagrams

Figure 5. $\overline{\text{INVALID}}$ Propagation Delay Times and Supply Enabling Time

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APPLICATION INFORMATION



V_{CC} vs CAPACITOR VALUES

V_{CC}	C1	C2, C3, and C4
3.3 V $\pm$ 0.15 V	0.1 μ F	0.1 μ F
3.3 V $\pm$ 0.3 V	0.22 μ F	0.22 μ F
5 V $\pm$ 0.5 V	0.047 μ F	0.33 μ F
3 V to 5.5 V	0.22 μ F	1 μ F

Figure 6. Typical Operating Circuit and Capacitor Values

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
SN65C3238DB	PREVIEW	SSOP	DB	28	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN65C3238DBR	ACTIVE	SSOP	DB	28	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN65C3238DBRE4	ACTIVE	SSOP	DB	28	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN65C3238DBRG4	ACTIVE	SSOP	DB	28	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN65C3238DW	ACTIVE	SOIC	DW	28	20	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN65C3238DWE4	ACTIVE	SOIC	DW	28	20	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN65C3238DWG4	ACTIVE	SOIC	DW	28	20	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN65C3238DWR	ACTIVE	SOIC	DW	28	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN65C3238DWRE4	ACTIVE	SOIC	DW	28	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN65C3238DWRG4	ACTIVE	SOIC	DW	28	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN65C3238PW	ACTIVE	TSSOP	PW	28	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN65C3238PWE4	ACTIVE	TSSOP	PW	28	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN65C3238PWG4	ACTIVE	TSSOP	PW	28	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN65C3238PWR	ACTIVE	TSSOP	PW	28	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN65C3238PWRE4	ACTIVE	TSSOP	PW	28	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN65C3238PWRG4	ACTIVE	TSSOP	PW	28	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN75C3238DB	PREVIEW	SSOP	DB	28	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN75C3238DBR	ACTIVE	SSOP	DB	28	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN75C3238DBRE4	ACTIVE	SSOP	DB	28	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN75C3238DBRG4	ACTIVE	SSOP	DB	28	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN75C3238DW	ACTIVE	SOIC	DW	28	20	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN75C3238DWE4	ACTIVE	SOIC	DW	28	20	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN75C3238DWG4	ACTIVE	SOIC	DW	28	20	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN75C3238DWR	ACTIVE	SOIC	DW	28	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN75C3238DWRE4	ACTIVE	SOIC	DW	28	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
SN75C3238DWRG4	ACTIVE	SOIC	DW	28	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN75C3238PW	ACTIVE	TSSOP	PW	28	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN75C3238PWE4	ACTIVE	TSSOP	PW	28	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN75C3238PWG4	ACTIVE	TSSOP	PW	28	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN75C3238PWR	ACTIVE	TSSOP	PW	28	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN75C3238PWRE4	ACTIVE	TSSOP	PW	28	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN75C3238PWRG4	ACTIVE	TSSOP	PW	28	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

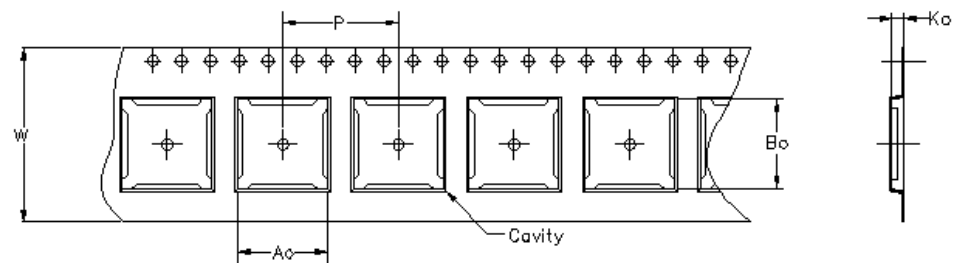
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

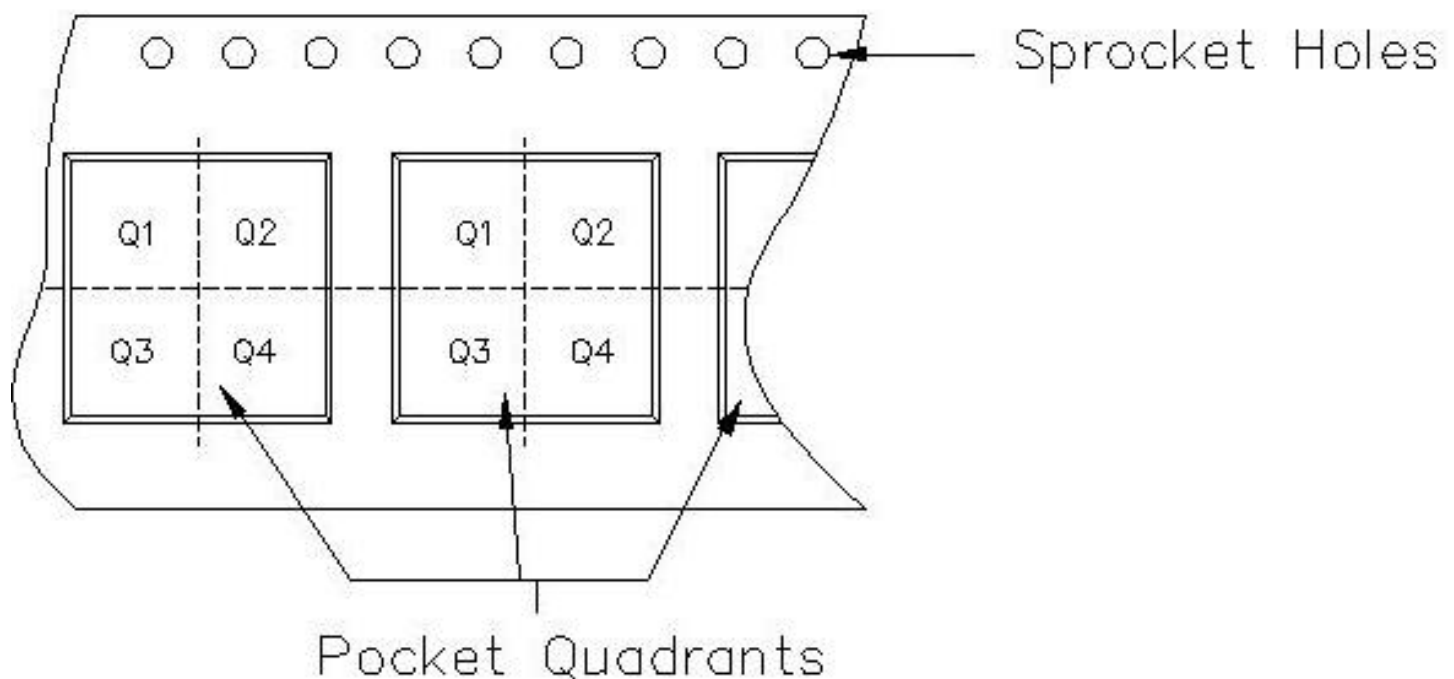
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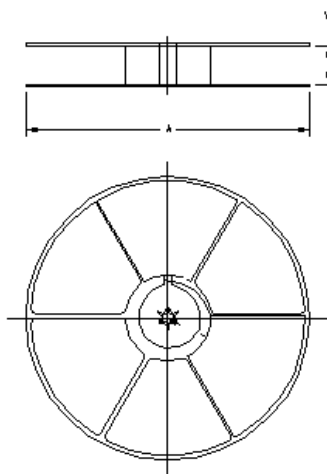
Carrier tape design is defined largely by the component length, width, and thickness.

A_o = Dimension designed to accommodate the component width.
B_o = Dimension designed to accommodate the component length.
K_o = Dimension designed to accommodate the component thickness.
W = Overall width of the carrier tape.
P = Pitch between successive cavity centers.



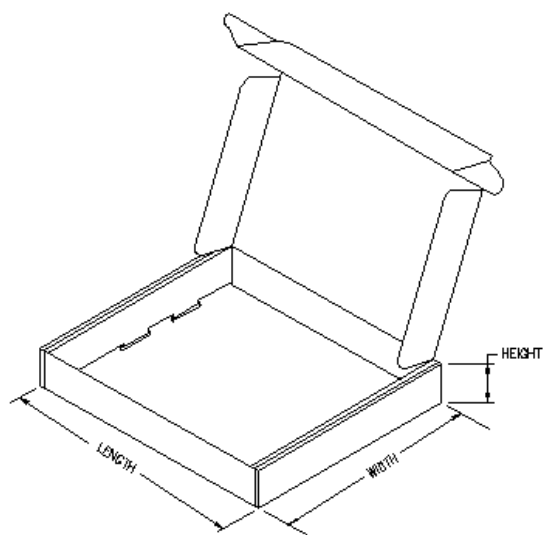
TAPE AND REEL INFORMATION

Device	Package	Pins	Site	Reel Diameter (mm)	Reel Width (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN65C3238DBR	DB	28	MLA	330	16	8.2	10.5	2.5	12	16	Q1
SN65C3238DWR	DW	28	TAI	330	32	11.35	18.67	3.1	16	32	Q1
SN65C3238PWR	PW	28	TAI	330	16	6.9	10.2	1.8	12	16	Q1
SN65C3238PWR	PW	28	MLA	330	16	7.1	10.4	1.6	12	16	Q1
SN75C3238DBR	DB	28	MLA	330	16	8.2	10.5	2.5	12	16	Q1
SN75C3238DWR	DW	28	TAI	330	32	11.35	18.67	3.1	16	32	Q1
SN75C3238PWR	PW	28	TAI	330	16	6.9	10.2	1.8	12	16	Q1
SN75C3238PWR	PW	28	MLA	330	16	7.1	10.4	1.6	12	16	Q1



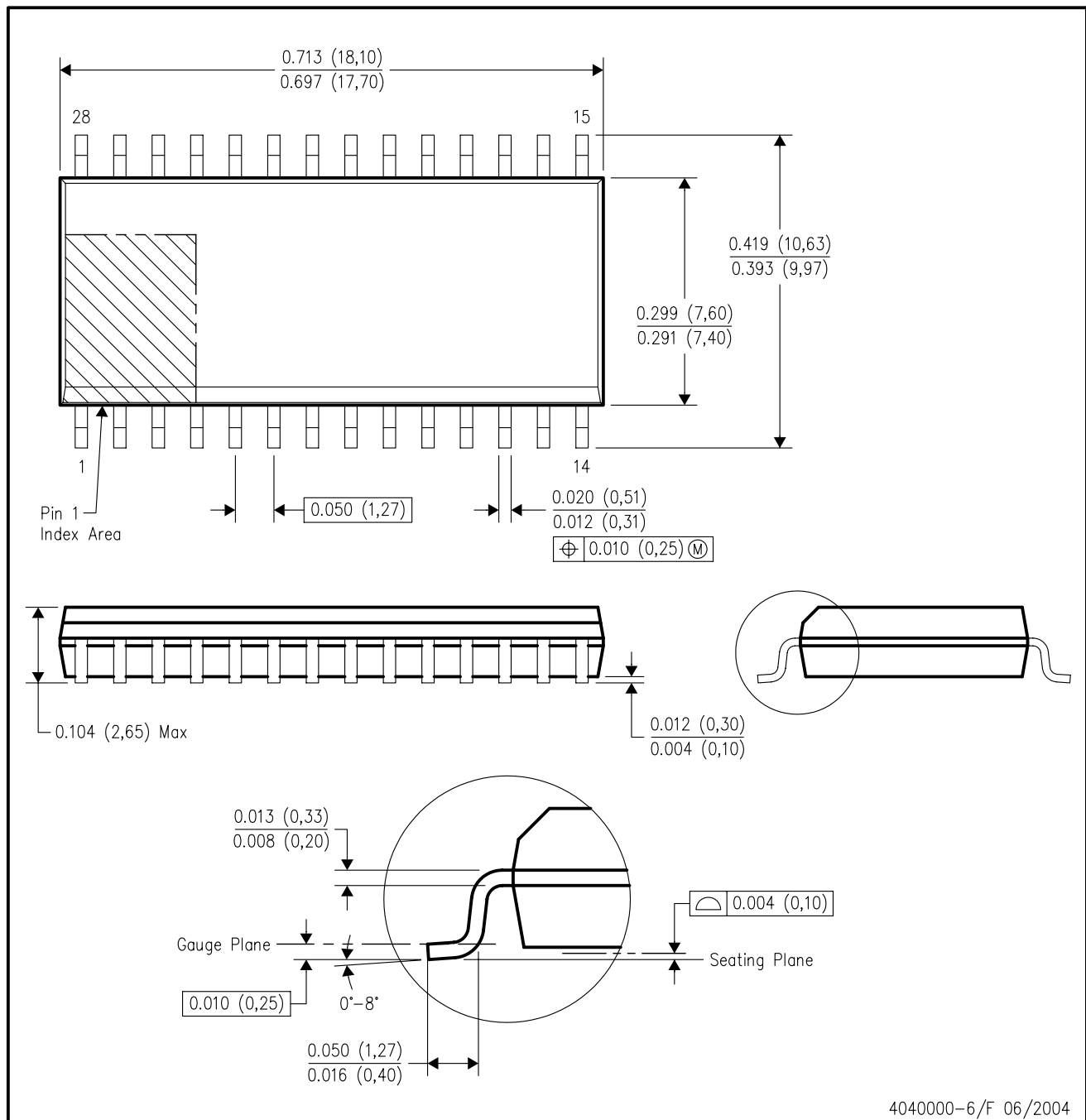
TAPE AND REEL BOX INFORMATION

Device	Package	Pins	Site	Length (mm)	Width (mm)	Height (mm)
SN65C3238DBR	DB	28	MLA	346.0	346.0	33.0
SN65C3238DWR	DW	28	TAI	346.0	346.0	49.0
SN65C3238PWR	PW	28	TAI	346.0	346.0	33.0
SN65C3238PWR	PW	28	MLA	346.0	346.0	33.0
SN75C3238DBR	DB	28	MLA	346.0	346.0	33.0
SN75C3238DWR	DW	28	TAI	346.0	346.0	49.0
SN75C3238PWR	PW	28	TAI	346.0	346.0	33.0
SN75C3238PWR	PW	28	MLA	346.0	346.0	33.0



DW (R-PDSO-G28)

PLASTIC SMALL-OUTLINE PACKAGE



4040000-6/F 06/2004

DB (R-PDSO-G**)

PLASTIC SMALL-OUTLINE

28 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-150

PW (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-153

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