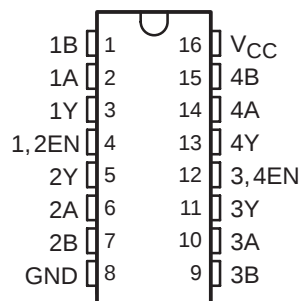


SN65175, SN75175 QUADRUPLE DIFFERENTIAL LINE RECEIVERS

SLLS145C – OCTOBER 1990 – REVISED NOVEMBER 2006

- Meet or Exceed the Requirements of ANSI Standard EIA/TIA-422-B, RS-423-B, and RS-485
- Meet ITU Recommendations V.10, V.11, X.26, and X.27
- Designed for Multipoint Bus Transmission on Long Bus Lines in Noisy Environments
- 3-State Outputs
- Common-Mode Input Voltage Range –12 V to 12 V
- Input Sensitivity . . . ± 200 mV
- Input Hysteresis . . . 50 mV Typ
- High Input Impedance . . . 12 k Ω Min
- Operate From Single 5-V Supply
- Low-Power Requirements
- Plug-In Replacement for MC3486

D OR N PACKAGE
(TOP VIEW)



description

The SN65175 and SN75175 are monolithic quadruple differential line receivers with 3-state outputs. They are designed to meet the requirements of ANSI Standards EIA/TIA-422-B, RS-423-B, and RS-485, and several ITU recommendations. These standards are for balanced multipoint bus transmission at rates up to 10 megabits per second. Each of the two pairs of receivers has a common active-high enable.

The receivers feature high input impedance, input hysteresis for increased noise immunity, and input sensitivity of ± 200 mV over a common-mode input voltage range of ± 12 V. The SN65175 and SN75175 are designed for optimum performance when used with the SN75172 or SN75174 quadruple differential line drivers.

The SN65175 is characterized for operation from -40°C to 85°C . The SN75175 is characterized for operation from 0°C to 70°C .

FUNCTION TABLE
(each receiver)

DIFFERENTIAL A – B	ENABLE	OUTPUT Y
$V_{ID} \geq 0.2$ V	H	H
-0.2 V $< V_{ID} < 0.2$ V	H	?
$V_{ID} \leq -0.2$ V	H	L
X	L	Z
Open circuit	H	?

H = high level, L = low level, ? = indeterminate,
X = irrelevant, Z = high impedance (off)



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

**TEXAS
INSTRUMENTS**

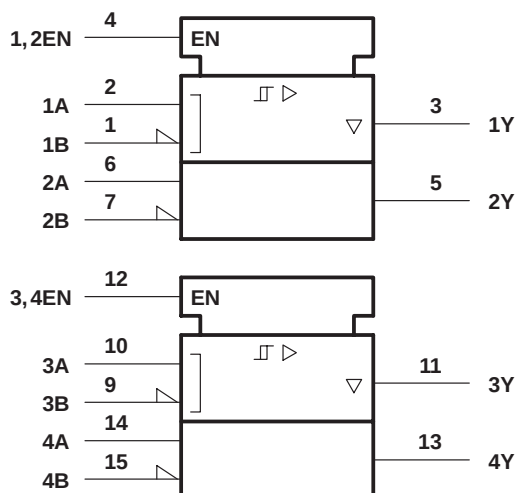
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

Copyright © 2006, Texas Instruments Incorporated

SN65175, SN75175 QUADRUPLE DIFFERENTIAL LINE RECEIVERS

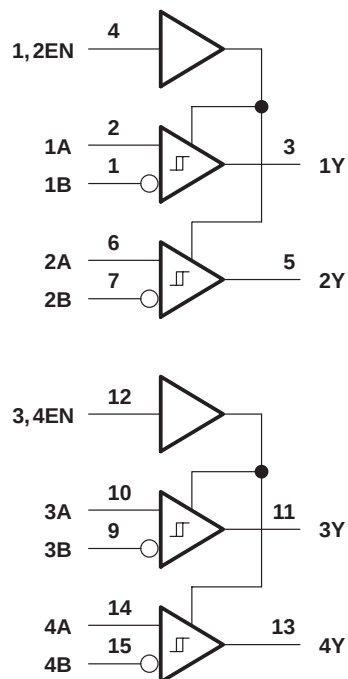
SLLS145C – OCTOBER 1990 – REVISED NOVEMBER 2006

logic symbol†

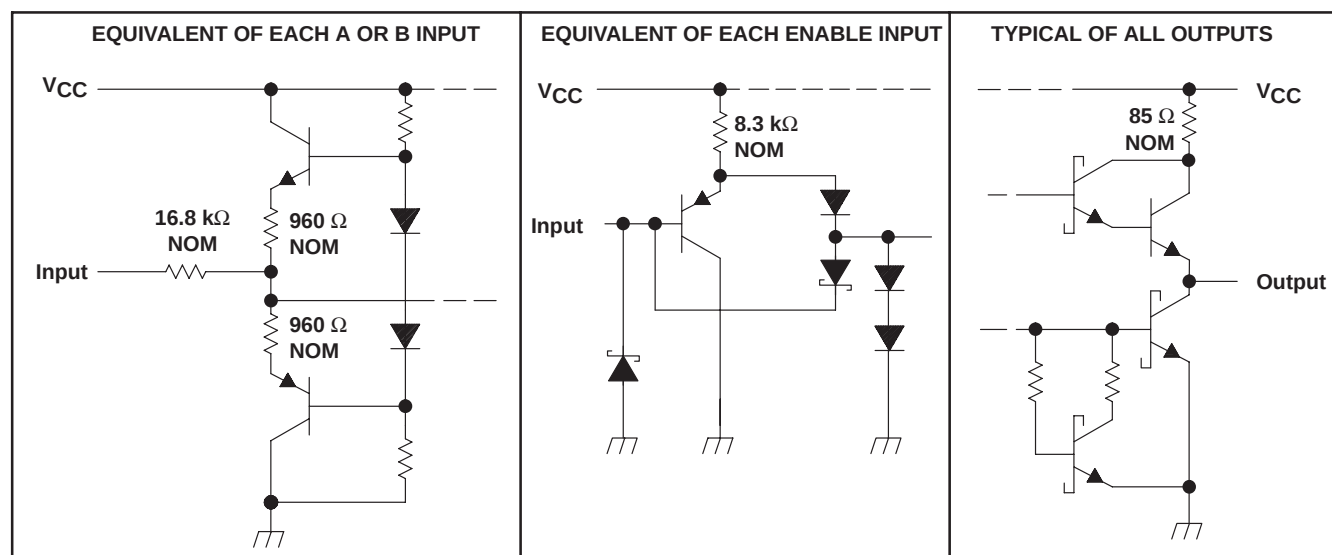


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



schematics of inputs and outputs



SN65175, SN75175 QUADRUPLE DIFFERENTIAL LINE RECEIVERS

SLLS145C – OCTOBER 1990 – REVISED NOVEMBER 2006

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage V_I , (A or B inputs)	± 25 V
Differential input voltage, V_{ID} (see Note 2)	± 25 V
Enable input voltage, V_I , EN	7 V
Low-level output current, I_{OL}	50 mA
Continuous total dissipation	See Dissipation Rating Table
Operating free-air temperature range, T_A : SN65175	-40°C to 85°C
SN75175	0°C to 70°C
Storage temperature range, T_{stg}	-65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. All voltage values, except differential input voltage, are with respect to network ground terminal.
2. Differential-input voltage is measured at the noninverting input with respect to the corresponding inverting input.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25^{\circ}\text{C}$ POWER RATING	DERATING FACTOR	$T_A = 70^{\circ}\text{C}$ POWER RATING	$T_A = 85^{\circ}\text{C}$ POWER RATING
D	950 mW	7.6 mW/ $^{\circ}\text{C}$	608 mW	494 mW
N	1150 mW	9.2 mW/ $^{\circ}\text{C}$	736 mW	598 mW

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}		4.75	5	5.25	V
Common-mode input voltage, V_{IC}				± 12	V
Differential input voltage, V_{ID}				± 12	V
High-level enable-input voltage, V_{IH}		2			V
Low-level enable-input voltage, V_{IL}				0.8	V
High-level output current, I_{OH}				-400	μA
Low-level output current, I_{OL}				16	mA
Operating free-air temperature, T_A	SN65175	-40		85	$^{\circ}\text{C}$
	SN75175	0		70	



SN65175, SN75175

QUADRUPLE DIFFERENTIAL LINE RECEIVERS

SLLS145C – OCTOBER 1990 – REVISED NOVEMBER 2006

electrical characteristics over recommended ranges of common-mode input voltage, supply voltage and operating free-air temperature

PARAMETER	TEST CONDITIONS	MIN	TYP [†]	MAX	UNIT
V _{IT+} Positive-going input threshold voltage	V _O = 2.7 V, I _O = -0.4 mA			0.2	V
V _{IT-} Negative-going input threshold voltage	V _O = 0.5 V, I _O = 16 mA	-0.2 [‡]			V
V _{hys} Hysteresis voltage (V _{IT+} - V _{IT-})	See Figure 4		50		mV
V _{IK} Enable-input clamp voltage	I _I = -18 mA			-1.5	V
V _{OH} High-level output voltage	V _{ID} = 200 mV, I _{OH} = -400 µA, See Figure 1		2.7		V
V _{OL} Low-level output voltage	V _{ID} = -200 mV, See Figure 1			0.45	V
				0.5	
I _{OZ} High-impedance-state output current	V _O = 0.4 V to 2.4 V			±20	µA
I _I Line input current	Other input at 0 V, See Note 3			1	mA
				-0.8	
I _{IH} High-level enable-input current	V _{IH} = 2.7 V			20	µA
I _{IL} Low-level enable-input current	V _{IL} = 0.4 V			-100	µA
r _i Input resistance			12		kΩ
I _{OS} Short-circuit output current [§]		-15		-85	mA
I _{CC} Supply current	Outputs disabled			70	mA

[†] All typical values are at V_{CC} = 5 V, T_A = 25°C.

[‡] The algebraic convention, in which the less positive (more negative) limit is designated as minimum, is used in this data sheet for threshold voltage levels only.

[§] Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.

NOTE 3: Refer to ANSI Standards EIA/TIA-422-B, RS-423-B, and RS-485 for exact conditions.

switching characteristics, V_{CC} = 5 V, C_L = 15 pF, T_A = 25°C

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t _{PLH} Propagation delay time, low- to high-level output	See Figure 2		22	35	ns
t _{PHL} Propagation delay time, high- to low-level output			25	35	ns
t _{PZH} Output enable time to high level	See Figure 3		13	30	ns
t _{PZL} Output enable time to low level			19	30	ns
t _{PHZ} Output disable time from high level	See Figure 3		26	35	ns
t _{PLZ} Output disable time from low level			25	35	ns



PARAMETER MEASUREMENT INFORMATION

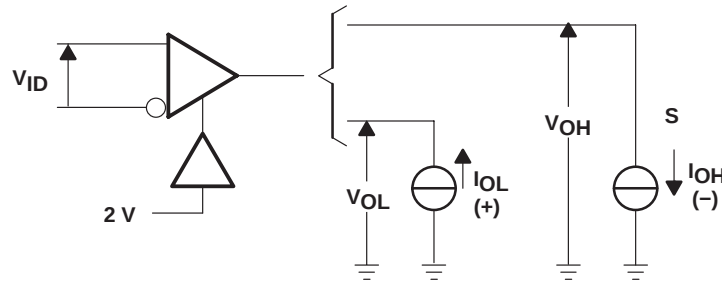
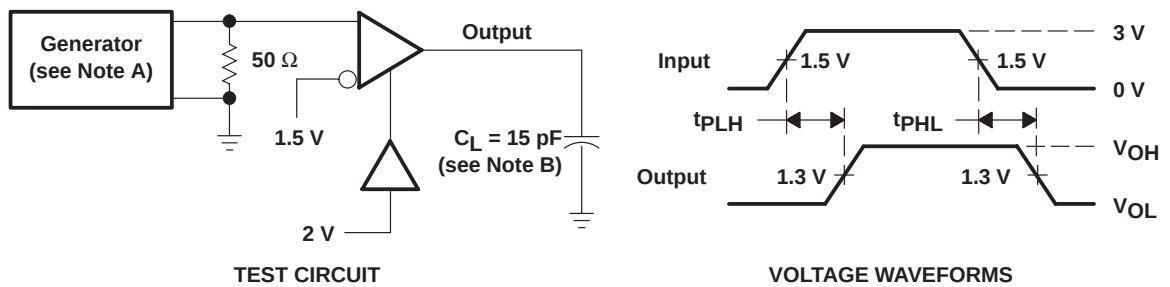


Figure 1. V_{OH} , V_{OL}



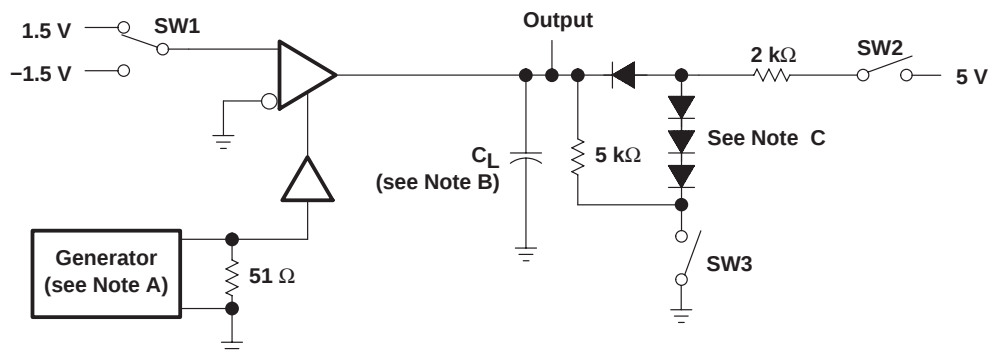
- NOTES: A. The input pulse is supplied by a generator having the following characteristics: $\text{PRR} \leq 1\ \text{MHz}$, duty cycle = 50%, $t_r \leq 6\ \text{ns}$, $t_f \leq 6\ \text{ns}$, $Z_O = 50\ \Omega$.
B. C_L includes probe and stray capacitance.

Figure 2. Test Circuit and Voltage Waveforms

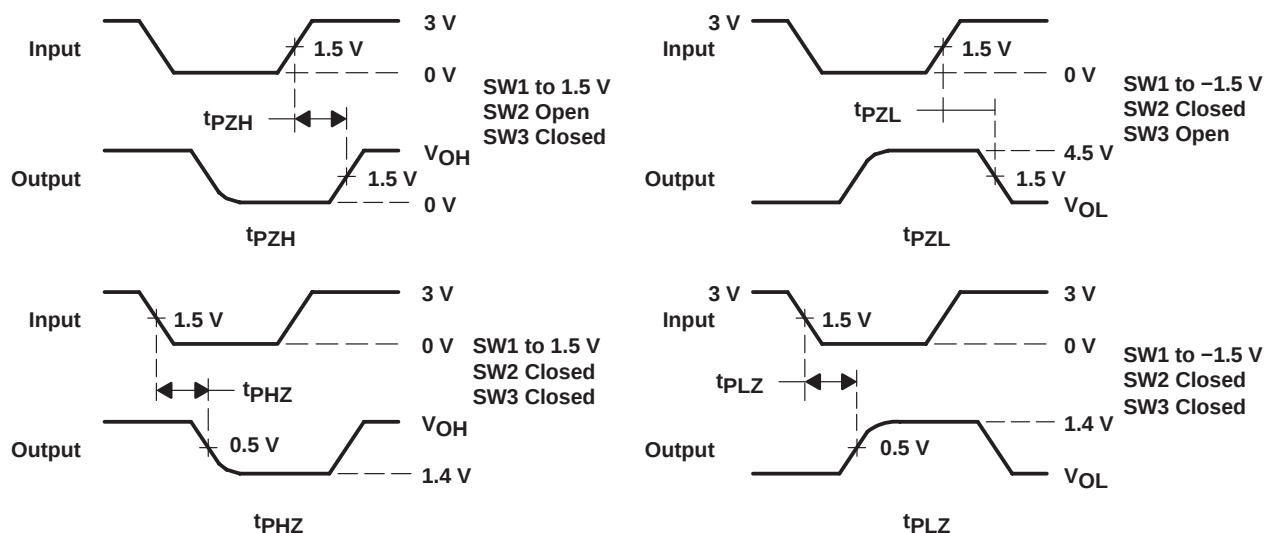
SN65175, SN75175 QUADRUPLE DIFFERENTIAL LINE RECEIVERS

SLLS145C – OCTOBER 1990 – REVISED NOVEMBER 2006

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT



VOLTAGE WAVEFORMS

- NOTES: A. The input pulse is supplied by a generator having the following characteristics: $PRR \leq 1 \text{ MHz}$, duty cycle = 50%, $t_f \leq 6 \text{ ns}$, $t_r \leq 6 \text{ ns}$, $Z_O = 50 \Omega$.
 B. C_L includes probe and stray capacitance.
 C. All diodes are 1N916 or equivalent.

Figure 3. Test Circuit and Voltage Waveforms

TYPICAL CHARACTERISTICS

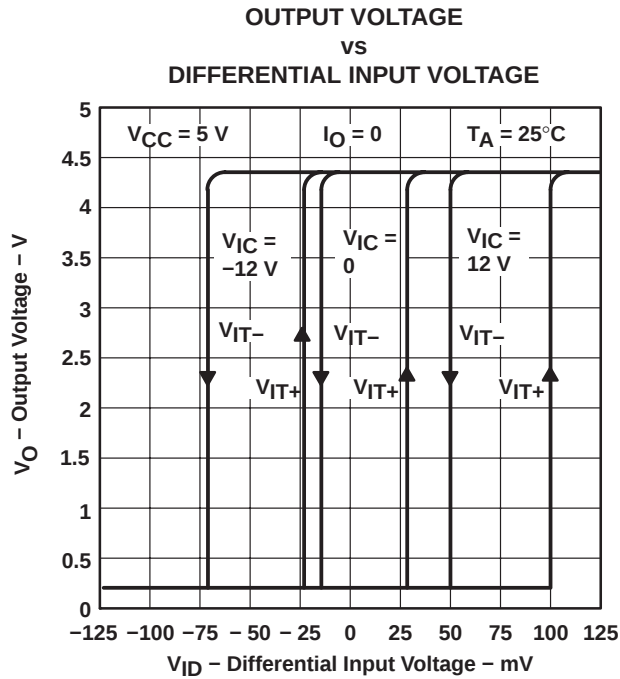


Figure 4

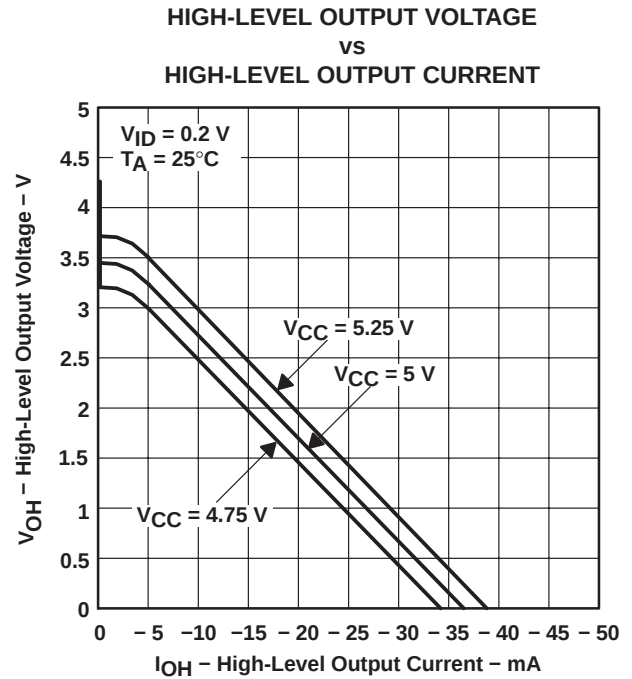


Figure 5

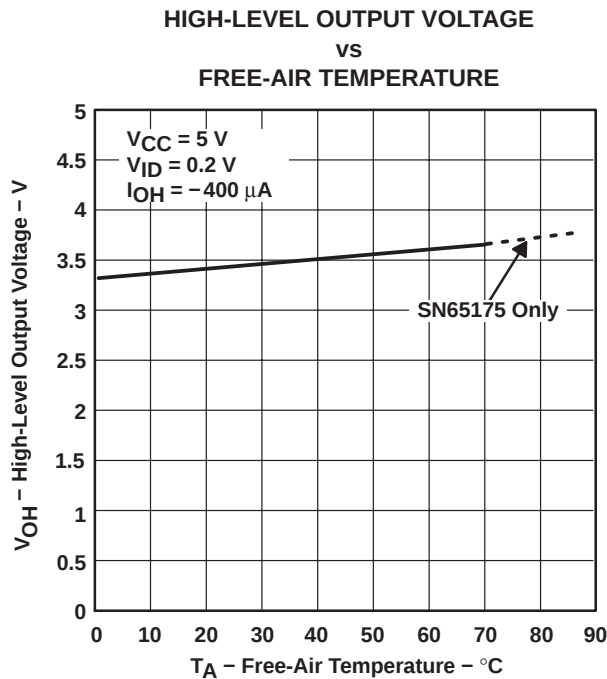


Figure 6

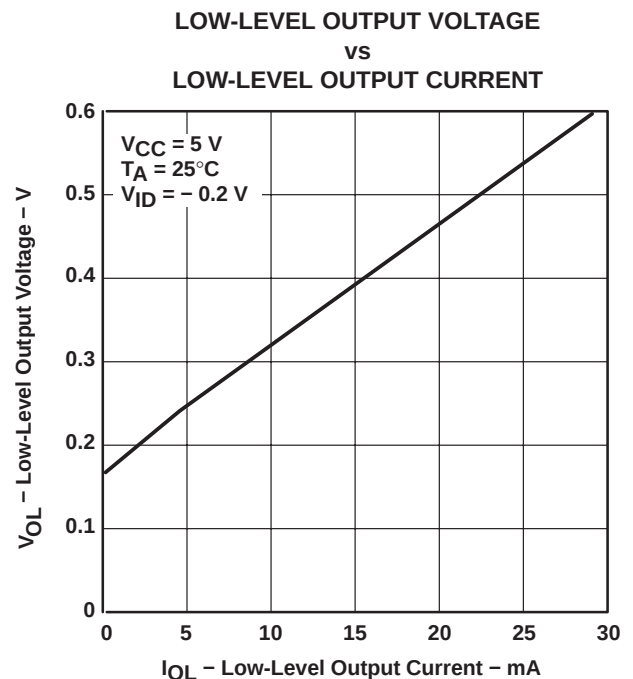


Figure 7

SN65175, SN75175

QUADRUPLE DIFFERENTIAL LINE RECEIVERS

SLLS145C – OCTOBER 1990 – REVISED NOVEMBER 2006

TYPICAL CHARACTERISTICS

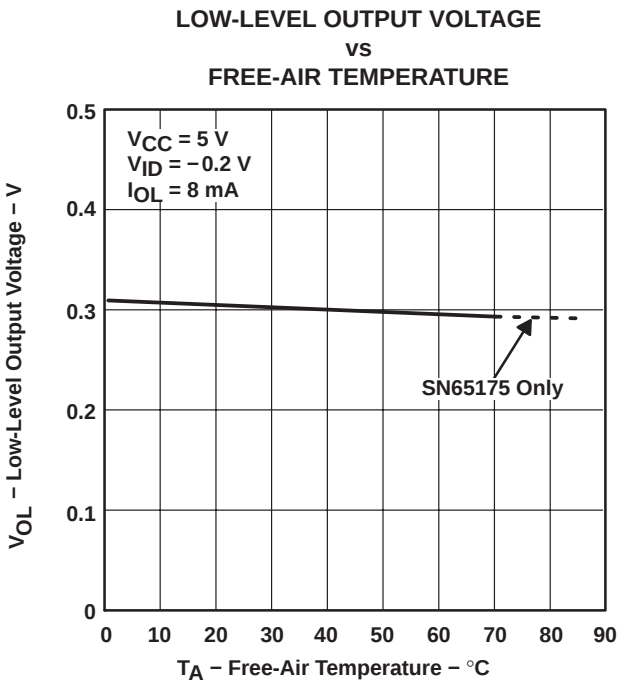


Figure 8

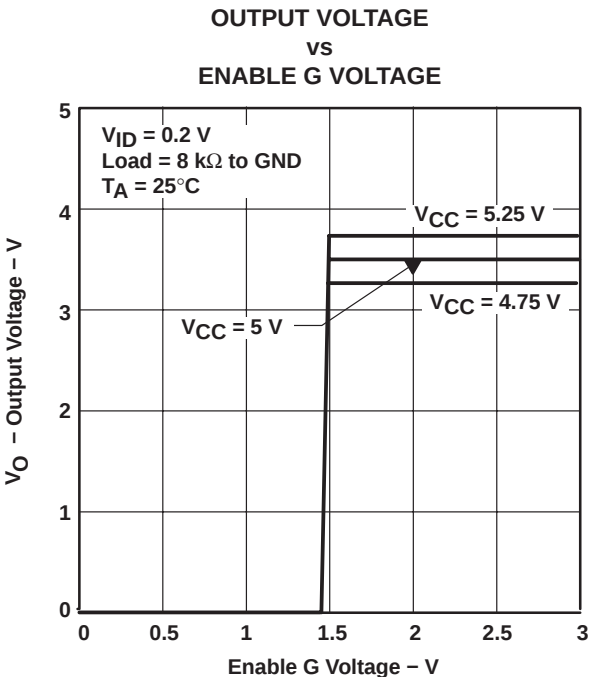


Figure 9

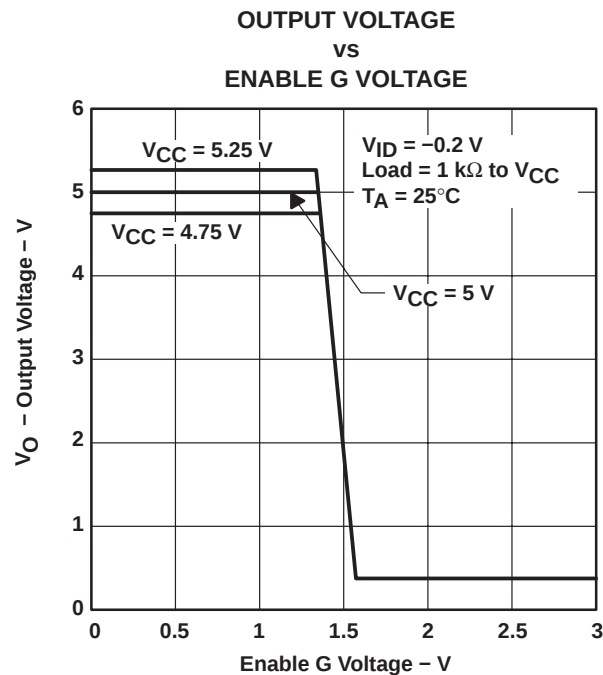


Figure 10

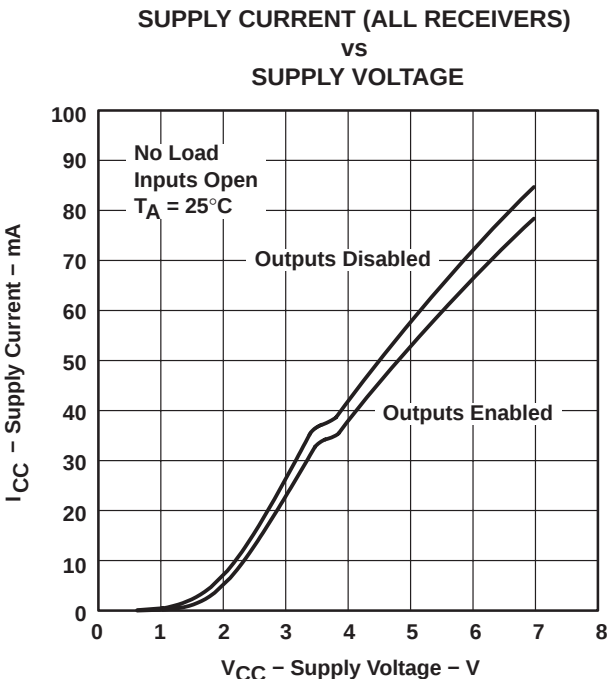
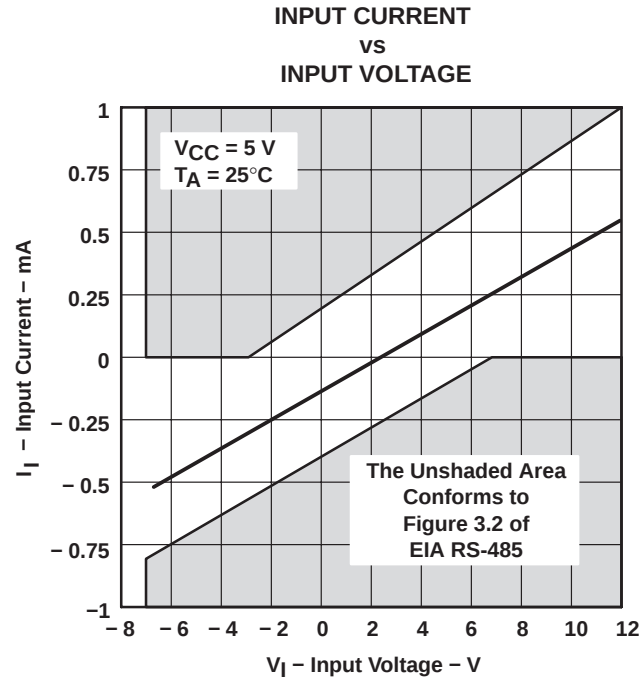
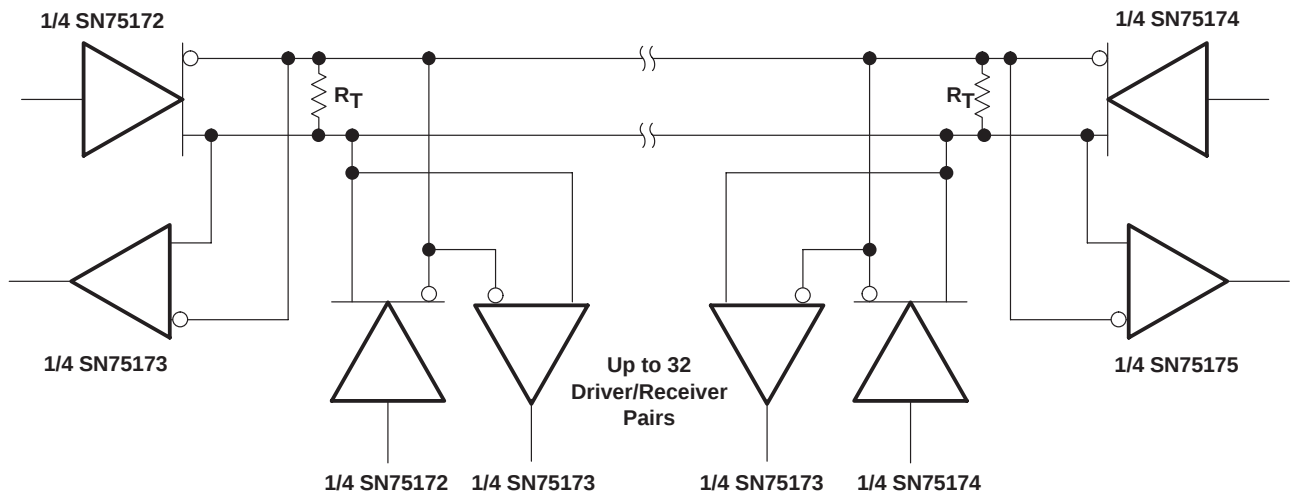


Figure 11

TYPICAL CHARACTERISTICS



APPLICATION INFORMATION



NOTE A: The line should be terminated at both ends in its characteristic impedance ($R_T = Z_0$). Stub lengths off the main line should be kept as short as possible.

Figure 13. Typical Application Circuit

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
SN65175D	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN65175DE4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN65175DG4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN65175DR	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN65175DRE4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN65175DRG4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN75175D	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN75175DE4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN75175DG4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN75175DR	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN75175DRE4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN75175DRG4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN75175J	OBSOLETE	CDIP	J	16		TBD	Call TI	Call TI
SN75175N	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN75175NE4	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN75175NSR	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN75175NSRE4	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

J (R-GDIP-T**)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



PINS ** DIM	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



4040083/F 03/03

- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. This package is hermetically sealed with a ceramic lid using glass frit.
 - D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
 - E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

N (R-PDIP-T**)

16 PINS SHOWN

PLASTIC DUAL-IN-LINE PACKAGE



PINS ** DIM	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS-001 VARIATION	AA	BB	AC	AD



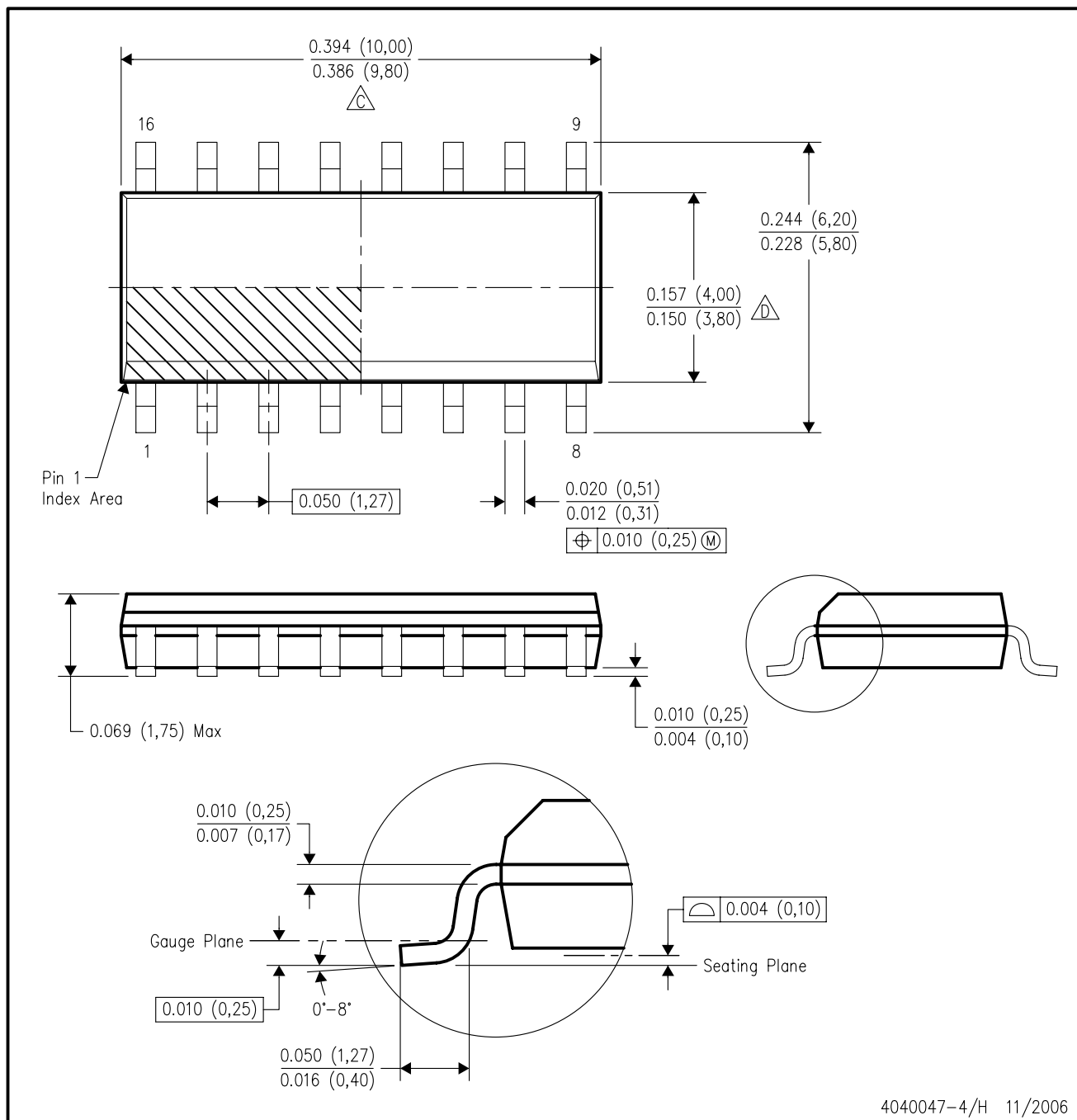
4040049/E 12/2002

NOTES:

- A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
-  Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 The 20 pin end lead shoulder width is a vendor option, either half or full width.

D (R-PDSO-G16)

PLASTIC SMALL-OUTLINE PACKAGE



NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 (0,15) per end.
- D. Body width does not include interlead flash. Interlead flash shall not exceed .017 (0,43) per side.
- E. Reference JEDEC MS-012 variation AC.

MECHANICAL DATA

NS (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third-party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Following are URLs where you can obtain information on other Texas Instruments products and application solutions:

Products		Applications	
Amplifiers	amplifier.ti.com	Audio	www.ti.com/audio
Data Converters	dataconverter.ti.com	Automotive	www.ti.com/automotive
DSP	dsp.ti.com	Broadband	www.ti.com/broadband
Interface	interface.ti.com	Digital Control	www.ti.com/digitalcontrol
Logic	logic.ti.com	Military	www.ti.com/military
Power Mgmt	power.ti.com	Optical Networking	www.ti.com/opticalnetwork
Microcontrollers	microcontroller.ti.com	Security	www.ti.com/security
Low Power Wireless	www.ti.com/lpw	Telephony	www.ti.com/telephony
		Video & Imaging	www.ti.com/video
		Wireless	www.ti.com/wireless

Mailing Address: Texas Instruments
Post Office Box 655303 Dallas, Texas 75265

Copyright © 2006, Texas Instruments Incorporated