SLLS060B - FEBRUARY 1990 - REVISED MAY 1995

- Meets or Exceeds the Requirements of IBM[™] System 360/370 Input/Output Interface Specification GA22-6974-3
- Minimum Output Voltage of 3.11 V at I_{OH} = -59.3 mA
- Fault-Flag Circuit Output Signals Driver Output Fault
- Fault-Detection Current-Limit Circuit Minimizes Power Dissipation During a Fault Condition
- Dual Common Enable
- Individual Fault Flags
- Designed to Replace the MC3481

description

The SN75126 quadruple line driver is designed to meet the IBM 360/370 I/O specification A22-6974-3. The output voltage is 3.11 V minimum (at $I_{OH} = -59.3$ mA) over the recommended ranges of supply voltage (4.5 V to 5.95 V) and temperature. Driver outputs use a fault-detection current-limit circuit to allow high drive current but still minimize power dissipation when the output is shorted to ground. The SN75126 is compatible with standard TTL logic and supply voltages.

Fault-flag circuitry is designed to sense and signal a line short on any Y line. Upon detecting an output fault condition, the fault-flag circuit forces the driver output into a low state and signals a fault condition by causing the fault-flag output to go low.

The SN75126 can drive a 50- Ω load or a 90- Ω load as used in many I/O systems. Optimum performance can be achieved when the device is used with either the SN75128 or SN75129 line receivers. Also, see the SN751730 for new 360/370 interface designs.

The SN75126 is characterized for operation from 0°C to 70°C.

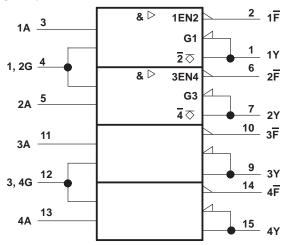
D OR N PACKAGE (TOP VIEW)								
1Y [1F [1A [1,2G [2A [2Y [GND]	1 2 3 4 5 6 7 8	υ	16 15 14 13 12 11 10 9	VCC 4Y 4F 4A 3,4G 3A 3F 3Y				
l				l				

FUNCTION TABLE							
INP	JTS	OUT	PUTS				
G	Α	Y	F				
L	Х	L	Н				
н	Н	н	н				
н	Н	S	L				

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logic symbol[†]



[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

$1A \frac{3}{4}$

2 1F

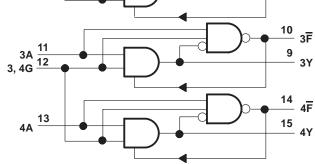
1 1 1Y

6 2F

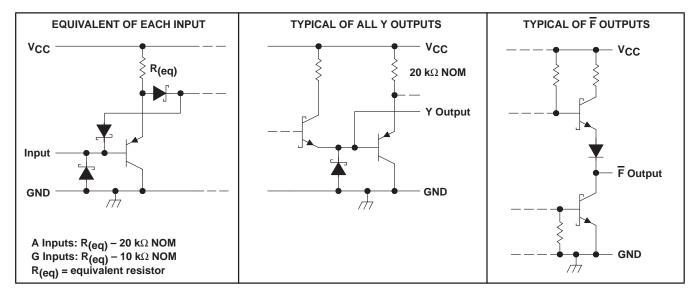
7

2Y

logic diagram (positive logic)



schematics of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage, V _{CC} Input voltage, V _I	
Continuous total power dissipation	
Operating free-air temperature range, T _A	0°C to 70°C
Storage temperature range, T _{stg}	– 65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.



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DISSIPATION RATING TABLE								
PACKAGE	$T_{A} \le 25^{\circ}C$ POWER RATING	DERATING FACTOR ABOVE T _A = 25°C	T _A = 70°C POWER RATING					
D	950 mW	7.6 mW/°C	608 mW					
Ν	1150 mW	9.2 mW/°C	736 mW					

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V _{CC}	4.5	5	5.95	V
High-level input voltage, VIH	2			V
Low-level input voltage, VIL			0.8	V
High-level output current, I _{OH}			-59.3	mA
Operating free-air temperature, T _A	0		70	°C

electrical characteristics over recommended operating free-air temperature range

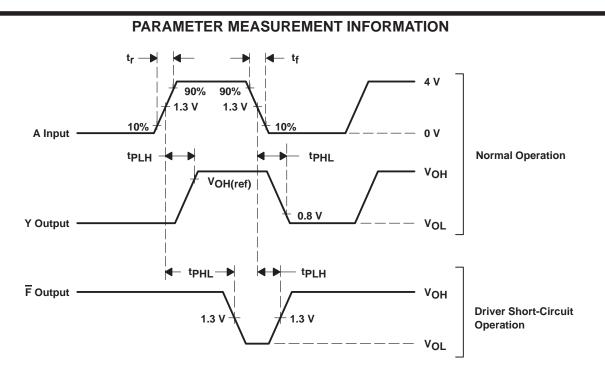
	PARAMETER			TEST CONDITION	IS	MIN	MAX	UNIT	
VIK	Input clamp voltage	A,G	V _{CC} = 4.5 V,	lj = – 18 mA			-1.5	V	
		Y	V _{CC} = 4.5 V,	I _{OH} = -59.3 mA,	V _{IH} = 2 V	3.11			
VOH	High-level output voltage	Y	V _{CC} = 5.25 V,	I _{OH} = -41 mA,	V _{IH} = 2 V	3.9		V	
		F	V _{CC} = 4.5 V,	I _{OH} = -400 μA,	V _{IH} = 2 V	2.5			
		Y	V _{CC} = 5.5 V,	$I_{OL} = -240 \ \mu A$,	V _{IL} = 0.8 V		0.15		
VOL	Low-level output voltage	Y	V _{CC} = 5.95 V,	$I_{OL} = -1 \text{ mA},$	$V_{IL} = 0.8 V$		0.15	v	
VOL	Low level output voltage	F	V _{CC} = 4.5 V, V _{IH} = 2 V	I <mark>OL</mark> = 8 mA,	Y at 0 V,		0.5	v	
	Off state subsut suggest	Y	V _{CC} = 4.5 V,	$V_{\parallel} = 0,$	V _O = 3.11 V		100	μA	
^I O(off)	Off-state output current	Y	$V_{CC} = 0,$	$V_{\parallel} = 0,$	V _O = 3.11 V		200		
lj Inpu	lonut ourroot	А					100	A	
	Input current	G	V _{CC} = 4.5 V,	V _I = 5.5 V			200	μA	
I	High-level input current	А	V _{CC} = 4.5 V,		20				
ЧН	nigh-level input current	G	VCC = 4.5 V,	V _I = 2.7 V			40	μA	
۱	Low-level input current	А	$V_{CC} = 5.95 \text{ V}, \qquad V_{I} = 0.4 \text{ V}$			-250	μA		
ΊL		G	VCC = 0.00 V,	v] = 0.4 v			-500	μΛ	
		Y	V _{CC} = 5.5 V,	$V_{O} = 0,$	V _{IH} = 2.7 V		-5		
	Short-circuit output current	F	V _{CC} = 5.5 V,	$V_{O} = 0$		-15	-100	mA	
los	Short-circuit output current	Y	V _{CC} = 5.95 V,	$V_{O} = 0,$	VIH = 2.7 V		-5	mA	
		F	V _{CC} = 5.95 V,	$V_{O} = 0$		-15	-110		
10.011	Supply current, all outputs high		V _{CC} = 5.5 V,	No load,	V _{IH} = 2 V		70	mA	
ICCH			V _{CC} = 5.95 V,	No load,	V _{IH} = 2 V		80		
	Supply current, Y outputs low		V _{CC} = 5.5 V,	No load,	V _{IL} = 0.8 V		55	mΔ	
ICCL			V _{CC} = 5.95 V,	No load,	V _{IL} = 0.8 V		70	mA	



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switching characteristics at $T_A = 25^{\circ}C$

	PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	MAX	UNIT
^t PLH	Propagation delay time, low- to high-level output			$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V},$ R ₁ = 50 Ω ,		40	ns
t _{PHL}	Propagation delay time, high- to low-level output	A Y		$C_{L} = 50 \text{ pF},$		37	ns
t <u>PLH</u> tPHL	Ratio of propagation delay times			$V_{OH(ref)} = 3.11 V,$ See Figures 1 and 2	0.3	3	
^t PLH	Propagation delay time, low- to high-level output	A	Y	$V_{CC} = 5.25$ V to 5.95 V, R _L = 90 Ω, C _L = 50 pF,		45	ns
^t PHL	Propagation delay time, high- to low-level output			VOH(ref) = 3.9 V, See Figures 1 and 2		45	ns
^t PLH	Propagation delay time, low- to high-level output	A	F	$V_{CC} = 5 V,$ $C_L = 15 pF,$ $D_L = 2 t C$		60	ns
^t PHL	Propagation delay time, high- to low-level output			$R_L = 2 k\Omega$, See Figures 1 and 2		100	ns



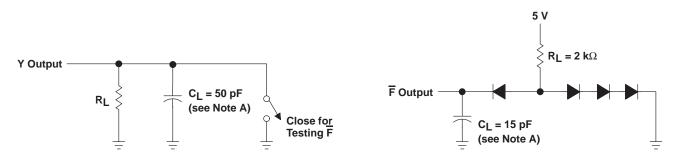
NOTE: The input pulse is supplied by a generator having the following characteristics: PRR \leq 1 MHz, duty cycle \leq 50%, t_f \leq 6 ns, t_f \leq 6 ns, Z_Q \approx 50 Ω .

Figure 1. Input and Output Voltage Waveforms



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PARAMETER MEASUREMENT INFORMATION



NOTE A: C_L includes probe and stray capacitance.

Figure 2. Switching Characteristics Load Circuits



PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
SN75126N	OBSOLETE	PDIP	Ν	16	TBD	Call TI	Call TI

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS) or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details. TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

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⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



NOTES:

- A. All linear dimensions are in inches (millimeters).B. This drawing is subject to change without notice.
- Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
- \triangle The 20 pin end lead shoulder width is a vendor option, either half or full width.



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Mailing Address:

Texas Instruments

Post Office Box 655303 Dallas, Texas 75265

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