

# SN54F109, SN74F109 DUAL J-K POSITIVE-EDGE-TRIGGERED FLIP-FLOPS WITH CLEAR AND PRESET

SDFS047A – MARCH 1987 – REVISED OCTOBER 1993

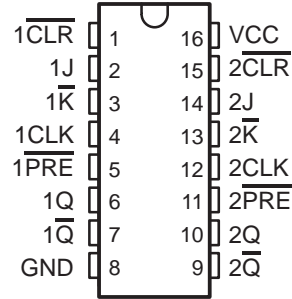
- Package Options Include Plastic Small-Outline Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs

## description

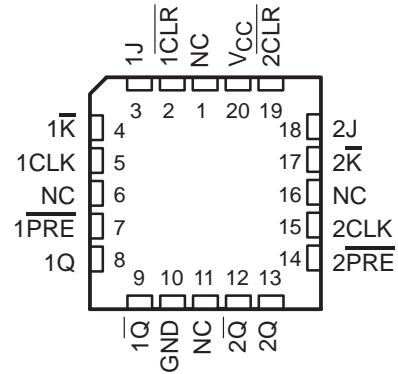
These devices contain two independent J-K positive-edge-triggered flip-flops. A low level at the preset (PRE) or clear (CLR) inputs sets or resets the outputs regardless of the levels of the other inputs. When PRE and CLR are inactive (high), data at the J and K input meeting the setup-time requirements are transferred to the outputs on the positive-going edge of the clock pulse. Clock triggering occurs at a voltage level and is not directly related to the rise time of the clock pulse. Following the hold time interval, data at the J and K inputs may be changed without affecting the levels at the outputs. These versatile flip-flops can perform as toggle flip-flops by grounding K and tying J high. They also can perform as D-type flip-flops if J and K are tied together.

The SN54F109 is characterized for operation over the full military temperature range of -55°C to 125°C. The SN74F109 is characterized for operation from 0°C to 70°C.

SN54F109 . . . J PACKAGE  
SN74F109 . . . D OR N PACKAGE  
(TOP VIEW)



SN54F109 . . . FK PACKAGE  
(TOP VIEW)



NC – No internal connection

FUNCTION TABLE

INPUTS					OUTPUTS	
PRE	CLR	CLK	J	K	Q	Q
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H†	H†
H	H	↑	L	L	L	H
H	H	↑	H	L	Toggle	
H	H	↑	L	H	Q <sub>0</sub>	Q <sub>0</sub>
H	H	↑	H	H	H	L
H	H	L	X	X	Q <sub>0</sub>	Q <sub>0</sub>

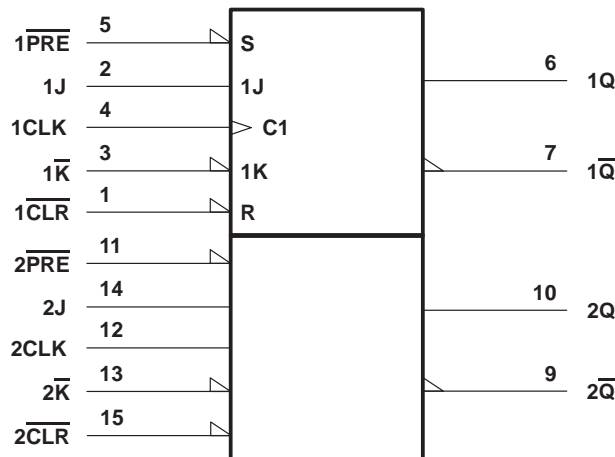
† The output levels are not guaranteed to meet the minimum levels for V<sub>OH</sub>. Furthermore, this configuration is nonstable; that is, it will not persist when PRE or CLR returns to its inactive (high) level.

# SN54F109, SN74F109

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### logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.  
Pin numbers shown are for the D, J, and N packages.

### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, $V_{CC}$	–0.5 V to 7 V
Input voltage range, $V_I$ (see Note 1)	–1.2 V to 7 V
Input current range	–30 mA to 5 mA
Voltage range applied to any output in the high state	–0.5 V to $V_{CC}$
Current into any output in the low state	40 mA
Operating free-air temperature range: SN54F109	–55°C to 125°C
SN74F109	0°C to 70°C
Storage temperature range	–65°C to 150°C

‡ Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input voltage ratings may be exceeded provided the input current ratings are observed.

### recommended operating conditions

		SN54F109			SN74F109			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
$V_{CC}$	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
$V_{IH}$	High-level input voltage	2			2			V
$V_{IL}$	Low-level input voltage			0.8			0.8	V
$I_{IK}$	Input clamp current			–18			–18	mA
$I_{OH}$	High-level output current			–1			–1	mA
$I_{OL}$	Low-level output current			20			20	mA
$T_A$	Operating free-air temperature	–55		125	0		70	°C

# SN54F109, SN74F109

## DUAL J-K POSITIVE-EDGE-TRIGGERED FLIP-FLOPS

### WITH CLEAR AND PRESET

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**electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)**

PARAMETER	TEST CONDITIONS	SN54F109			SN74F109			UNIT
		MIN	TYP†	MAX	MIN	TYP†	MAX	
$V_{IK}$	$V_{CC} = 4.5\text{ V}$ , $I_I = -18\text{ mA}$			-1.2			-1.2	V
$V_{OH}$	$V_{CC} = 4.5\text{ V}$ , $I_{OH} = -1\text{ mA}$	2.5	3.4		2.5	3.4		V
	$V_{CC} = 4.75\text{ V}$ , $I_{OH} = -1\text{ mA}$				2.7			
$V_{OL}$	$V_{CC} = 4.5\text{ V}$ , $I_{OL} = 20\text{ mA}$		0.3	0.5		0.3	0.5	V
$I_I$	$V_{CC} = 5.5\text{ V}$ , $V_I = 7\text{ V}$			0.1			0.1	mA
$I_{IH}$	$V_{CC} = 5.5\text{ V}$ , $V_I = 2.7\text{ V}$			20			20	μA
$I_{IL}$	J, $\overline{K}$ , CLK			-0.6			-0.6	mA
	$\overline{PRE}$ or $\overline{CLR}$			-1.8			-1.8	
$I_{OS}^\ddagger$	$V_{CC} = 5.5\text{ V}$ , $V_O = 0$	-60		-150	-60		-150	mA
$I_{CC}$	$V_{CC} = 5.5\text{ V}$ , See Note 2		11.7	17		11.7	17	mA

† All typical values are at  $V_{CC} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$ .

‡ Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.

NOTE 2:  $I_{CC}$  is measured with J,  $\overline{K}$ , CLK, and  $\overline{PRE}$  grounded then with J,  $\overline{K}$ , CLK, and  $\overline{CLR}$  grounded.

**timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)**

			V <sub>CC</sub> = 5 V, T <sub>A</sub> = 25°C		SN54F109		SN74F109		UNIT
			‘F74						
			MIN	MAX	MIN	MAX	MIN	MAX	
f <sub>clock</sub>	Clock frequency		0	100	0	70	0	90	MHz
t <sub>w</sub>	Pulse duration		CLK high, $\overline{\text{PRE}}$ or $\overline{\text{CLR}}$ low	4	4	4	ns		
			CLK low	5	5	5			
t <sub>su</sub>	Setup time, data before CLK↑	High	3	3	3	ns			
		Low	3	3	3				
	Setup time, inactive-state before CLK↑§	$\overline{\text{PRE}}$ or $\overline{\text{CLR}}$ to CLK	2	2	2				
t <sub>h</sub>	Hold time, data after CLK↑	High	1	1	1	ns			
		Low	1	1	1				

§ Inactive-state setup time is also referred to as recovery time.

**switching characteristics (see Note 3)**

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V <sub>CC</sub> = 5 V, C <sub>L</sub> = 50 pF, R <sub>L</sub> = 500 Ω, T <sub>A</sub> = 25°C			V <sub>CC</sub> = 4.5 V to 5.5 V, C <sub>L</sub> = 50 pF, R <sub>L</sub> = 500 Ω, T <sub>A</sub> = MIN to MAX†				UNIT
			‘F109			SN54F109		SN74F109		
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f <sub>max</sub>			100	150		70		90		MHz
t <sub>PLH</sub>	CLK	Q or $\overline{Q}$	3	4.9	7	3	9	3	8	ns
t <sub>PHL</sub>			3.6	5.8	8	3.6	10.5	3.6	9.2	
t <sub>PLH</sub>	$\overline{\text{PRE}}$ or $\overline{\text{CLR}}$	Q or $\overline{Q}$	2.4	4.8	7	2.4	9	2.4	8	ns
t <sub>PHL</sub>			2.7	6.6	9	2.7	11.5	2.7	10.5	

¶ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

NOTE 3: Load circuits and waveforms are shown in Section 1.



**PACKAGING INFORMATION**

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/Ball Finish	MSL Peak Temp <sup>(3)</sup>
5962-9758001Q2A	ACTIVE	LCCC	FK	20	1	None	Call TI	Level-NC-NC-NC
5962-9758001QEA	ACTIVE	CDIP	J	16	1	None	Call TI	Level-NC-NC-NC
5962-9758001QFA	ACTIVE	CFP	W	16	1	None	Call TI	Level-NC-NC-NC
JM38510/34102B2A	ACTIVE	LCCC	FK	20	1	None	Call TI	Level-NC-NC-NC
JM38510/34102BEA	ACTIVE	CDIP	J	16	1	None	Call TI	Level-NC-NC-NC
JM38510/34102BFA	ACTIVE	CFP	W	16	1	None	Call TI	Level-NC-NC-NC
SN74F109D	ACTIVE	SOIC	D	16	40	Pb-Free (RoHS)	CU NIPDAU	Level-2-260C-1 YEAR/ Level-1-235C-UNLIM
SN74F109DR	ACTIVE	SOIC	D	16	2500	Pb-Free (RoHS)	CU NIPDAU	Level-2-260C-1 YEAR/ Level-1-235C-UNLIM
SN74F109N	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	Level-NC-NC-NC
SNJ54F109FK	ACTIVE	LCCC	FK	20	1	None	Call TI	Level-NC-NC-NC
SNJ54F109J	ACTIVE	CDIP	J	16	1	None	Call TI	Level-NC-NC-NC
SNJ54F109W	ACTIVE	CFP	W	16	1	None	Call TI	Level-NC-NC-NC

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBsolete:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - May not be currently available - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**None:** Not yet available Lead (Pb-Free).

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean "Pb-Free" and in addition, uses package materials that do not contain halogens, including bromine (Br) or antimony (Sb) above 0.1% of total product weight.

<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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