

## Features

- True dual port memory enables simultaneous access to the shared array from each port
- Synchronous pipelined operation with single data rate (SDR) operation on each port
  - SDR interface at 200 MHz
  - Up to 28.8 Gb/s bandwidth (200 MHz × 72-bit × 2 ports)
- Selectable pipelined or flow-through mode
- 1.5 V or 1.8 V core power supply
- Commercial and Industrial temperature
- IEEE 1149.1 JTAG boundary scan
- Available in 484-ball PBGA (× 72) and 256-ball FBGA (× 36 and × 18) packages
- FullFlex72 family
  - 36-Mbit: 512 K × 72 (CYD36S72V18)
  - 18-Mbit: 256 K × 72 (CYD18S72V18)
  - 9-Mbit: 128 K × 72 (CYD09S72V18)
- FullFlex36 family
  - 36-Mbit: 1 M × 36 (CYD36S36V18)
  - 18-Mbit: 512 K × 36 (CYD18S36V18)
  - 9-Mbit: 256 K × 36 (CYD09S36V18)
  - 2-Mbit: 64 K × 36 (CYD02S36V18)
- FullFlex18 family
  - 36-Mbit: 2 M × 18 (CYD36S18V18)
  - 18-Mbit: 1 M × 18 (CYD18S18V18)
  - 9-Mbit: 512 K × 18 (CYD09S18V18)
- Built in deterministic access control to manage address collisions
  - Deterministic flag output upon collision detection
  - Collision detection on back-to-back clock cycles
  - First busy address readback
- Advanced features for improved high speed data transfer and flexibility
  - Variable impedance matching (VIM)
  - Echo clocks
  - Selectable LVTTTL (3.3 V), Extended HSTL (1.4 V to 1.9 V), 1.8 V LVCMOS, or 2.5 V LVCMOS IO on each port
  - Burst counters for sequential memory access
  - Mailbox with interrupt flags for message passing
  - Dual chip enables for easy depth expansion

## Functional Description

The FullFlex™ dual port SRAM families consist of 2-Mbit, 9-Mbit, 18-Mbit, and 36-Mbit synchronous, true dual port static RAMs that are high speed, low power 1.8 V or 1.5 V CMOS. Two ports are provided, enabling simultaneous access to the array. Simultaneous access to a location triggers deterministic access control. For FullFlex72 these ports operate independently with 72-bit bus widths and each port is independently configured for two pipelined stages. Each port is also configured to operate in pipelined or flow through mode.

The advanced features include the following:

- Built in deterministic access control to manage address collisions during simultaneous access to the same memory location
- Variable Impedance Matching (VIM) to improve data transmission by matching the output driver impedance to the line impedance
- Echo clocks to improve data transfer

To reduce the static power consumption, chip enables power down the internal circuitry. The number of latency cycles before a change in CE0 or CE1 enables or disables the databus matches the number of cycles of read latency selected for the device. For a valid write or read to occur, activate both chip enable inputs on a port.

Each port contains an optional burst counter on the input address register. After externally loading the counter with the initial address, the counter increments the address internally.

Additional device features include a mask register and a mirror register to control counter increments and wrap around. The counter interrupt (CNTINT) flags notify the host that the counter reaches maximum count value on the next clock cycle. The host reads the burst counter internal address, mask register address, and busy address on the address lines. The host also loads the counter with the address stored in the mirror register by using the retransmit functionality. Mailbox interrupt flags are used for message passing, and JTAG boundary scan and asynchronous Master Reset (MRST) are also available. The [Logic Block Diagram on page 2](#) shows these features.

The FullFlex72 is offered in a 484-ball plastic BGA package. The FullFlex36 and FullFlex18 are available in 256-ball fine pitch BGA package except the 36-Mbit devices which are offered in 484-ball plastic BGA package.

The Logic Block Diagram for FullFlex72, FullFlex36, and FullFlex18 family follows: [1, 2, 3]

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**Figure 1. FullFlex72 SDR 484-ball BGA Pinout (Top View)**

|    | 1                   | 2                   | 3                               | 4      | 5      | 6      | 7      | 8      | 9         | 10        | 11                  | 12                  | 13        | 14        | 15     | 16     | 17     | 18     | 19     | 20                              | 21                  | 22                  |
|----|---------------------|---------------------|---------------------------------|--------|--------|--------|--------|--------|-----------|-----------|---------------------|---------------------|-----------|-----------|--------|--------|--------|--------|--------|---------------------------------|---------------------|---------------------|
| A  | DNU                 | DQ61L               | DQ59L                           | DQ57L  | DQ54L  | DQ51L  | DQ48L  | DQ45L  | DQ42L     | DQ39L     | DQ36L               | DQ36R               | DQ39R     | DQ42R     | DQ45R  | DQ48R  | DQ51R  | DQ54R  | DQ57R  | DQ59R                           | DQ61R               | DNU                 |
| B  | DQ63L               | DQ62L               | DQ60L                           | DQ58L  | DQ55L  | DQ52L  | DQ49L  | DQ46L  | DQ43L     | DQ40L     | DQ37L               | DQ37R               | DQ40R     | DQ43R     | DQ46R  | DQ49R  | DQ52R  | DQ55R  | DQ58R  | DQ60R                           | DQ62R               | DQ63R               |
| C  | DQ65L               | DQ64L               | VSS                             | VSS    | DQ56L  | DQ53L  | DQ50L  | DQ47L  | DQ44L     | DQ41L     | DQ38L               | DQ38R               | DQ41R     | DQ44R     | DQ47R  | DQ50R  | DQ53R  | DQ56R  | VSS    | VSS                             | DQ64R               | DQ65R               |
| D  | DQ67L               | DQ66L               | VSS                             | VSS    | VSS    | CQ1L   | CQ1L   | VSS    | LOWSPDL   | PORTSTD0L | ZQ0L <sup>[4]</sup> | BUSYL               | CNTINTL   | PORTSTD1L | DNU    | CQ1R   | CQ1R   | VSS    | VSS    | VSS                             | DQ66R               | DQ67R               |
| E  | DQ69L               | DQ68L               | VDDIOL                          | VSS    | VSS    | VDDIOL | VDDIOL | VDDIOL | VDDIOL    | VDDIOL    | VTTL                | VTTL                | VTTL      | VDDIOR    | VDDIOR | VDDIOR | VDDIOR | DNU    | VSS    | VDDIOR                          | DQ68R               | DQ69R               |
| F  | DQ71L               | DQ70L               | CE1L                            | CE0L   | VDDIOL | VDDIOL | VDDIOL | VDDIOL | VDDIOL    | VCORE     | VCORE               | VCORE               | VCORE     | VDDIOR    | VDDIOR | VDDIOR | VDDIOR | VDDIOR | CE0R   | CE1R                            | DQ70R               | DQ71R               |
| G  | A0L                 | A1L                 | RETL                            | BE4L   | VDDIOL | VDDIOL | VREFL  | VSS    | VSS       | VSS       | VSS                 | VSS                 | VSS       | VSS       | VSS    | VREFR  | VDDIOR | VDDIOR | BE4R   | RETR                            | A1R                 | A0R                 |
| H  | A2L                 | A3L                 | $\overline{\text{WRPL}}$        | BE5L   | VDDIOL | VDDIOL | VSS    | VSS    | VSS       | VSS       | VSS                 | VSS                 | VSS       | VSS       | VSS    | VSS    | VDDIOR | VDDIOR | BE5R   | WRPR                            | A3R                 | A2R                 |
| J  | A4L                 | A5L                 | READYL                          | BE6L   | VDDIOL | VDDIOL | VSS    | VSS    | VSS       | VSS       | VSS                 | VSS                 | VSS       | VSS       | VSS    | VSS    | VDDIOR | VDDIOR | BE6R   | READYR                          | A5R                 | A4R                 |
| K  | A6L                 | A7L                 | ZQ1L <sup>[4, 5]</sup>          | BE7L   | VTTL   | VCORE  | VSS    | VSS    | VSS       | VSS       | VSS                 | VSS                 | VSS       | VSS       | VSS    | VSS    | VCORE  | VDDIOR | BE7R   | ZQ1R <sup>[4, 5]</sup>          | A7R                 | A6R                 |
| L  | A8L                 | A9L                 | CL                              | OEL    | VTTL   | VCORE  | VSS    | VSS    | VSS       | VSS       | VSS                 | VSS                 | VSS       | VSS       | VSS    | VSS    | VCORE  | VTTL   | OER    | CR                              | A9R                 | A8R                 |
| M  | A10L                | A11L                | VSS                             | BE3L   | VTTL   | VCORE  | VSS    | VSS    | VSS       | VSS       | VSS                 | VSS                 | VSS       | VSS       | VSS    | VSS    | VCORE  | VTTL   | BE3R   | VSS                             | A11R                | A10R                |
| N  | A12L                | A13L                | ADSL                            | BE2L   | VDDIOL | VCORE  | VSS    | VSS    | VSS       | VSS       | VSS                 | VSS                 | VSS       | VSS       | VSS    | VSS    | VCORE  | VTTL   | BE2R   | ADSR                            | A13R                | A12R                |
| P  | A14L                | A15L                | CNT/MSKL                        | BE1L   | VDDIOL | VDDIOL | VSS    | VSS    | VSS       | VSS       | VSS                 | VSS                 | VSS       | VSS       | VSS    | VSS    | VDDIOR | VDDIOR | BE1R   | CNT/MSKR                        | A15R                | A14R                |
| R  | A16L <sup>[8]</sup> | A17L <sup>[7]</sup> | CNTENL                          | BE0L   | VDDIOL | VDDIOL | VSS    | VSS    | VSS       | VSS       | VSS                 | VSS                 | VSS       | VSS       | VSS    | VSS    | VDDIOR | VDDIOR | BE0R   | CNTENR                          | A17R <sup>[7]</sup> | A16R <sup>[8]</sup> |
| T  | A18L <sup>[6]</sup> | DNU                 | CNTRSTL                         | INTL   | VDDIOL | VDDIOL | VREFL  | VSS    | VSS       | VSS       | VSS                 | VSS                 | VSS       | VSS       | VSS    | VREFR  | VDDIOR | VDDIOR | INTR   | CNTRSTR                         | DNU                 | A18R <sup>[6]</sup> |
| U  | DQ35L               | DQ34L               | $\text{R}/\overline{\text{WL}}$ | CQENL  | VDDIOL | VDDIOL | VDDIOL | VDDIOL | VDDIOL    | VCORE     | VCORE               | VCORE               | VCORE     | VDDIOR    | VDDIOR | VDDIOR | VDDIOR | VDDIOR | CQENR  | $\text{R}/\overline{\text{WR}}$ | DQ34R               | DQ35R               |
| V  | DQ33L               | DQ32L               | FTSELL                          | VDDIOL | DNU    | VDDIOL | VDDIOL | VDDIOL | VDDIOL    | VTTL      | VTTL                | VTTL                | VDDIOR    | VDDIOR    | VDDIOR | VDDIOR | VDDIOR | TRST   | VDDIOR | FTSELR                          | DQ32R               | DQ33R               |
| W  | DQ31L               | DQ30L               | VSS                             | MRST   | VSS    | CQ0L   | CQ0L   | DNU    | PORTSTD1R | CNTINTR   | BUSYR               | ZQ0R <sup>[4]</sup> | PORTSTD0R | LOWSPDR   | VSS    | CQ0R   | CQ0R   | VSS    | TDI    | TDO                             | DQ30R               | DQ31R               |
| Y  | DQ29L               | DQ28L               | VSS                             | VSS    | DQ20L  | DQ17L  | DQ14L  | DQ11L  | DQ8L      | DQ5L      | DQ2L                | DQ2R                | DQ5R      | DQ8R      | DQ11R  | DQ14R  | DQ17R  | DQ20R  | TMS    | TCK                             | DQ28R               | DQ29R               |
| AA | DQ27L               | DQ26L               | DQ24L                           | DQ22L  | DQ19L  | DQ16L  | DQ13L  | DQ10L  | DQ7L      | DQ4L      | DQ1L                | DQ1R                | DQ4R      | DQ7R      | DQ10R  | DQ13R  | DQ16R  | DQ19R  | DQ22R  | DQ24R                           | DQ26R               | DQ27R               |
| AB | DNU                 | DQ25L               | DQ23L                           | DQ21L  | DQ18L  | DQ15L  | DQ12L  | DQ9L   | DQ6L      | DQ3L      | DQ0L                | DQ0R                | DQ3R      | DQ6R      | DQ9R   | DQ12R  | DQ15R  | DQ18R  | DQ21R  | DQ23R                           | DQ25R               | DNU                 |

**Notes**

4. Leave this ball unconnected to disable VIM.
5. This ball is applicable only for 36-Mbit and DNU for 18-Mbit and lower densities.
6. Leave this Ball unconnected for CYD18S72V18 and CYD09S72V18.
7. Leave this Ball unconnected for CYD09S72V18.
8. Leave this Ball unconnected for CYD04S72V18.

**Figure 2. FullFlex36 SDR 484-ball BGA Pinout (Top View)<sup>[9]</sup>**

|    | 1    | 2    | 3                    | 4      | 5      | 6      | 7      | 8      | 9         | 10        | 11                   | 12                   | 13        | 14        | 15     | 16     | 17     | 18     | 19     | 20                   | 21   | 22   |
|----|------|------|----------------------|--------|--------|--------|--------|--------|-----------|-----------|----------------------|----------------------|-----------|-----------|--------|--------|--------|--------|--------|----------------------|------|------|
| A  | DNU  | DNU  | DNU                  | DNU    | DNU    | DQ33L  | DQ30L  | DQ27L  | DQ24L     | DQ21L     | DQ18L                | DQ18R                | DQ21R     | DQ24R     | DQ27R  | DQ30R  | DQ33R  | DNU    | DNU    | DNU                  | DNU  | DNU  |
| B  | DNU  | DNU  | DNU                  | DNU    | DNU    | DQ34L  | DQ31L  | DQ28L  | DQ25L     | DQ22L     | DQ19L                | DQ19R                | DQ22R     | DQ25R     | DQ28R  | DQ31R  | DQ34R  | DNU    | DNU    | DNU                  | DNU  | DNU  |
| C  | DNU  | DNU  | VSS                  | VSS    | DNU    | DQ35L  | DQ32L  | DQ29L  | DQ26L     | DQ23L     | DQ20L                | DQ20R                | DQ23R     | DQ26R     | DQ29R  | DQ32R  | DQ35R  | DNU    | VSS    | VSS                  | DNU  | DNU  |
| D  | DNU  | DNU  | VSS                  | VSS    | VSS    | CQ1L   | CQ1L   | VSS    | LOWSPDL   | PORTSTD0L | ZQ0L <sup>[10]</sup> | BUSYL                | CNTINTL   | PORTSTD1L | DNU    | CQ1R   | CQ1R   | VSS    | VSS    | VSS                  | DNU  | DNU  |
| E  | DNU  | DNU  | VDDIOL               | VSS    | VSS    | VDDIOL | VDDIOR | VDDIOR | VDDIOR    | VDDIOR    | VTTL                 | VTTL                 | VTTL      | VDDIOL    | VDDIOL | VDDIOL | VDDIOL | DNU    | VSS    | VDDIOR               | DNU  | DNU  |
| F  | DNU  | DNU  | CE1L                 | CE0L   | VDDIOL | VDDIOL | VDDIOR | VDDIOR | VDDIOR    | VCORE     | VCORE                | VCORE                | VCORE     | VDDIOL    | VDDIOL | VDDIOL | VDDIOR | VDDIOR | CE0R   | CE1R                 | DNU  | DNU  |
| G  | A0L  | A1L  | RETL                 | BE2L   | VDDIOL | VDDIOL | VREFL  | VSS    | VSS       | VSS       | VSS                  | VSS                  | VSS       | VSS       | VSS    | VREFR  | VDDIOR | VDDIOR | BE2R   | RETR                 | A1R  | A0R  |
| H  | A2L  | A3L  | WRPL                 | BE3L   | VDDIOL | VDDIOL | VSS    | VSS    | VSS       | VSS       | VSS                  | VSS                  | VSS       | VSS       | VSS    | VSS    | VDDIOR | VDDIOR | BE3R   | WRPR                 | A3R  | A2R  |
| J  | A4L  | A5L  | READYL               | DNU    | VDDIOL | VDDIOL | VSS    | VSS    | VSS       | VSS       | VSS                  | VSS                  | VSS       | VSS       | VSS    | VSS    | VDDIOR | VDDIOR | DNU    | READYR               | A5R  | A4R  |
| K  | A6L  | A7L  | ZQ1L <sup>[10]</sup> | DNU    | VTTL   | VCORE  | VSS    | VSS    | VSS       | VSS       | VSS                  | VSS                  | VSS       | VSS       | VSS    | VSS    | VCORE  | VDDIOR | DNU    | ZQ1R <sup>[10]</sup> | A7R  | A6R  |
| L  | A8L  | A9L  | CL                   | OEL    | VTTL   | VCORE  | VSS    | VSS    | VSS       | VSS       | VSS                  | VSS                  | VSS       | VSS       | VSS    | VSS    | VCORE  | VTTL   | OER    | CR                   | A9R  | A8R  |
| M  | A10L | A11L | VSS                  | DNU    | VTTL   | VCORE  | VSS    | VSS    | VSS       | VSS       | VSS                  | VSS                  | VSS       | VSS       | VSS    | VSS    | VCORE  | VTTL   | DNU    | VSS                  | A11R | A10R |
| N  | A12L | A13L | ADSL                 | DNU    | VDDIOL | VCORE  | VSS    | VSS    | VSS       | VSS       | VSS                  | VSS                  | VSS       | VSS       | VSS    | VSS    | VCORE  | VTTL   | DNU    | ADSR                 | A13R | A12R |
| P  | A14L | A15L | CNT/MSKL             | BE1L   | VDDIOL | VDDIOL | VSS    | VSS    | VSS       | VSS       | VSS                  | VSS                  | VSS       | VSS       | VSS    | VSS    | VDDIOR | VDDIOR | BE1R   | CNT/MSKR             | A15R | A14R |
| R  | A16L | A17L | CNTENL               | BE0L   | VDDIOL | VDDIOL | VSS    | VSS    | VSS       | VSS       | VSS                  | VSS                  | VSS       | VSS       | VSS    | VSS    | VDDIOR | VDDIOR | BE0R   | CNTENR               | A17R | A16R |
| T  | A18L | A19L | CNTRSTL              | INTL   | VDDIOL | VDDIOL | VREFL  | VSS    | VSS       | VSS       | VSS                  | VSS                  | VSS       | VSS       | VSS    | VREFR  | VDDIOR | VDDIOR | INTR   | CNTRSTR              | A19R | A18R |
| U  | DNU  | DNU  | R/WL                 | CQENL  | VDDIOL | VDDIOL | VDDIOR | VDDIOR | VDDIOR    | VCORE     | VCORE                | VCORE                | VCORE     | VDDIOL    | VDDIOL | VDDIOL | VDDIOR | VDDIOR | CQENR  | R/WR                 | DNU  | DNU  |
| V  | DNU  | DNU  | FTSELL               | VDDIOL | DNU    | VDDIOR | VDDIOR | VDDIOR | VDDIOR    | VTTL      | VTTL                 | VTTL                 | VDDIOL    | VDDIOL    | VDDIOL | VDDIOR | TRST   | VDDIOR | FTSELR | DNU                  | DNU  |      |
| W  | DNU  | DNU  | VSS                  | MRST   | VSS    | CQ0L   | CQ0L   | DNU    | PORTSTD1R | CNTINTR   | BUSYR                | ZQ0R <sup>[10]</sup> | PORTSTD0R | LOWSPDR   | VSS    | CQ0R   | CQ0R   | VSS    | TDI    | TDO                  | DNU  | DNU  |
| Y  | DNU  | DNU  | VSS                  | VSS    | DNU    | DQ17L  | DQ14L  | DQ11L  | DQ8L      | DQ5L      | DQ2L                 | DQ2R                 | DQ5R      | DQ8R      | DQ11R  | DQ14R  | DQ17R  | DNU    | TMS    | TCK                  | DNU  | DNU  |
| AA | DNU  | DNU  | DNU                  | DNU    | DNU    | DQ16L  | DQ13L  | DQ10L  | DQ7L      | DQ4L      | DQ1L                 | DQ1R                 | DQ4R      | DQ7R      | DQ10R  | DQ13R  | DQ16R  | DNU    | DNU    | DNU                  | DNU  | DNU  |
| AB | DNU  | DNU  | DNU                  | DNU    | DNU    | DQ15L  | DQ12L  | DQ9L   | DQ6L      | DQ3L      | DQ0L                 | DQ0R                 | DQ3R      | DQ6R      | DQ9R   | DQ12R  | DQ15R  | DNU    | DNU    | DNU                  | DNU  | DNU  |

**Notes**

9. Use this pinout only for device CYD36S36V18 of the FullFlex36 family.  
 10. Leave this ball unconnected to disable VIM.

**Figure 3. FullFlex18 SDR 484-ball BGA Pinout (Top View)<sup>[11]</sup>**

|    | 1    | 2    | 3                    | 4      | 5      | 6      | 7      | 8      | 9         | 10        | 11                   | 12                   | 13        | 14        | 15     | 16     | 17     | 18     | 19     | 20                   | 21   | 22   |
|----|------|------|----------------------|--------|--------|--------|--------|--------|-----------|-----------|----------------------|----------------------|-----------|-----------|--------|--------|--------|--------|--------|----------------------|------|------|
| A  | DNU  | DNU  | DNU                  | DNU    | DNU    | DNU    | DNU    | DNU    | DQ15L     | DQ12L     | DQ9L                 | DQ9R                 | DQ12R     | DQ15R     | DNU    | DNU    | DNU    | DNU    | DNU    | DNU                  | DNU  | DNU  |
| B  | DNU  | DNU  | DNU                  | DNU    | DNU    | DNU    | DNU    | DNU    | DQ16L     | DQ13L     | DQ10L                | DQ10R                | DQ13R     | DQ16R     | DNU    | DNU    | DNU    | DNU    | DNU    | DNU                  | DNU  | DNU  |
| C  | DNU  | DNU  | VSS                  | VSS    | DNU    | DNU    | DNU    | DNU    | DQ17L     | DQ14L     | DQ11L                | DQ11R                | DQ14R     | DQ17R     | DNU    | DNU    | DNU    | DNU    | VSS    | VSS                  | VSS  | DNU  |
| D  | DNU  | DNU  | VSS                  | VSS    | VSS    | CQ1L   | CQ1L   | VSS    | LOWSPDL   | PORTSTD0L | ZQ0L <sup>[12]</sup> | BUSYL                | CNTINTL   | PORTSTD1L | DNU    | CQ1R   | CQ1R   | VSS    | VSS    | VSS                  | DNU  | DNU  |
| E  | DNU  | DNU  | VDDIOL               | VSS    | VSS    | VDDIOL | VDDIOR | VDDIOR | VDDIOR    | VDDIOR    | VTTL                 | VTTL                 | VTTL      | VDDIOL    | VDDIOL | VDDIOL | VDDIOL | DNU    | VSS    | VDDIOR               | DNU  | DNU  |
| F  | DNU  | DNU  | CE1L                 | CE0L   | VDDIOL | VDDIOL | VDDIOR | VDDIOR | VDDIOR    | VCORE     | VCORE                | VCORE                | VCORE     | VDDIOL    | VDDIOL | VDDIOL | VDDIOR | VDDIOR | CE0R   | CE1R                 | DNU  | DNU  |
| G  | A0L  | A1L  | RETL                 | BE1L   | VDDIOL | VDDIOL | VREFL  | VSS    | VSS       | VSS       | VSS                  | VSS                  | VSS       | VSS       | VSS    | VREFR  | VDDIOR | VDDIOR | BE1R   | RETR                 | A1R  | A0R  |
| H  | A2L  | A3L  | WRPL                 | DNU    | VDDIOL | VDDIOL | VSS    | VSS    | VSS       | VSS       | VSS                  | VSS                  | VSS       | VSS       | VSS    | VSS    | VDDIOR | VDDIOR | DNU    | WRPR                 | A3R  | A2R  |
| J  | A4L  | A5L  | READYL               | DNU    | VDDIOL | VDDIOL | VSS    | VSS    | VSS       | VSS       | VSS                  | VSS                  | VSS       | VSS       | VSS    | VSS    | VDDIOR | VDDIOR | DNU    | READYR               | A5R  | A4R  |
| K  | A6L  | A7L  | ZQ1L <sup>[12]</sup> | DNU    | VTTL   | VCORE  | VSS    | VSS    | VSS       | VSS       | VSS                  | VSS                  | VSS       | VSS       | VSS    | VSS    | VCORE  | VDDIOR | DNU    | ZQ1R <sup>[12]</sup> | A7R  | A6R  |
| L  | A8L  | A9L  | CL                   | OEL    | VTTL   | VCORE  | VSS    | VSS    | VSS       | VSS       | VSS                  | VSS                  | VSS       | VSS       | VSS    | VSS    | VCORE  | VTTL   | OER    | CR                   | A9R  | A8R  |
| M  | A10L | A11L | VSS                  | DNU    | VTTL   | VCORE  | VSS    | VSS    | VSS       | VSS       | VSS                  | VSS                  | VSS       | VSS       | VSS    | VSS    | VCORE  | VTTL   | DNU    | VSS                  | A11R | A10R |
| N  | A12L | A13L | ADSL                 | DNU    | VDDIOL | VCORE  | VSS    | VSS    | VSS       | VSS       | VSS                  | VSS                  | VSS       | VSS       | VSS    | VSS    | VCORE  | VTTL   | DNU    | ADSR                 | A13R | A12R |
| P  | A14L | A15L | CNT/MSKL             | DNU    | VDDIOL | VDDIOL | VSS    | VSS    | VSS       | VSS       | VSS                  | VSS                  | VSS       | VSS       | VSS    | VSS    | VDDIOR | VDDIOR | DNU    | CNT/MSKR             | A15R | A14R |
| R  | A16L | A17L | CNTENL               | BE0L   | VDDIOL | VDDIOL | VSS    | VSS    | VSS       | VSS       | VSS                  | VSS                  | VSS       | VSS       | VSS    | VSS    | VDDIOR | VDDIOR | BE0R   | CNTENR               | A17R | A16R |
| T  | A18L | A19L | CNTRSTL              | INTL   | VDDIOL | VDDIOL | VREFL  | VSS    | VSS       | VSS       | VSS                  | VSS                  | VSS       | VSS       | VSS    | VREFR  | VDDIOR | VDDIOR | INTR   | CNTRSTR              | A19R | A18R |
| U  | A20L | DNU  | R/WL                 | CQENL  | VDDIOL | VDDIOL | VDDIOR | VDDIOR | VDDIOR    | VCORE     | VCORE                | VCORE                | VCORE     | VDDIOL    | VDDIOL | VDDIOL | VDDIOR | VDDIOR | CQENR  | R/WL                 | DNU  | A20R |
| V  | DNU  | DNU  | FTSELL               | VDDIOL | DNU    | VDDIOR | VDDIOR | VDDIOR | VDDIOR    | VTTL      | VTTL                 | VTTL                 | VDDIOL    | VDDIOL    | VDDIOL | VDDIOR | VDDIOR | TRST   | VDDIOR | FTSELR               | DNU  | DNU  |
| W  | DNU  | DNU  | VSS                  | MRST   | VSS    | CQ0L   | CQ0L   | DNU    | PORTSTD1R | CNTINTR   | BUSYR                | ZQ0R <sup>[12]</sup> | PORTSTD0R | LOWSPDR   | VSS    | CQ0R   | CQ0R   | VSS    | TDI    | TDO                  | DNU  | DNU  |
| Y  | DNU  | DNU  | VSS                  | VSS    | DNU    | DNU    | DNU    | DNU    | DQ8L      | DQ5L      | DQ2L                 | DQ2R                 | DQ5R      | DQ8R      | DNU    | DNU    | DNU    | DNU    | TMS    | TCK                  | DNU  | DNU  |
| AA | DNU  | DNU  | DNU                  | DNU    | DNU    | DNU    | DNU    | DNU    | DQ7L      | DQ4L      | DQ1L                 | DQ1R                 | DQ4R      | DQ7R      | DNU    | DNU    | DNU    | DNU    | DNU    | DNU                  | DNU  | DNU  |
| AB | DNU  | DNU  | DNU                  | DNU    | DNU    | DNU    | DNU    | DNU    | DQ6L      | DQ3L      | DQ0L                 | DQ0R                 | DQ3R      | DQ6R      | DNU    | DNU    | DNU    | DNU    | DNU    | DNU                  | DNU  | DNU  |

**Notes**

11. Use this pinout only for device CYD36S18V18 of the FullFlex18 family.  
 12. Leave this ball unconnected to disable VIM.

**Figure 4. FullFlex36 SDR 256-ball BGA (Top View)**

|   | 1                    | 2                    | 3                                   | 4                                  | 5                                | 6                                  | 7      | 8                               | 9                               | 10                   | 11                                 | 12                                | 13                                 | 14                                  | 15                   | 16                   |
|---|----------------------|----------------------|-------------------------------------|------------------------------------|----------------------------------|------------------------------------|--------|---------------------------------|---------------------------------|----------------------|------------------------------------|-----------------------------------|------------------------------------|-------------------------------------|----------------------|----------------------|
| A | DQ32L                | DQ30L                | DQ28L                               | DQ26L                              | DQ24L                            | DQ22L                              | DQ20L  | DQ18L                           | DQ18R                           | DQ20R                | DQ22R                              | DQ24R                             | DQ26R                              | DQ28R                               | DQ30R                | DQ32R                |
| B | DQ33L                | DQ31L                | DQ29L                               | DQ27L                              | DQ25L                            | DQ23L                              | DQ21L  | DQ19L                           | DQ19R                           | DQ21R                | DQ23R                              | DQ25R                             | DQ27R                              | DQ29R                               | DQ31R                | DQ33R                |
| C | DQ34L                | DQ35L                | $\overline{\text{RET}}\text{L}$     | $\overline{\text{INT}}\text{L}$    | CQ1L                             | $\overline{\text{CQ}}\text{1L}$    | DNU    | $\overline{\text{TR}}\text{ST}$ | $\overline{\text{MR}}\text{ST}$ | ZQ0R <sup>[13]</sup> | $\overline{\text{CQ}}\text{1R}$    | CQ1R                              | $\overline{\text{INTR}}$           | $\overline{\text{RETR}}$            | DQ35R                | DQ34R                |
| D | A0L                  | A1L                  | $\overline{\text{WR}}\text{PL}$     | VREFL                              | $\overline{\text{FT}}\text{SEL}$ | $\overline{\text{LOW}}\text{SPDL}$ | VSS    | VTTL                            | VTTL                            | VSS                  | $\overline{\text{LOW}}\text{SPDR}$ | $\overline{\text{FT}}\text{SELR}$ | VREFR                              | $\overline{\text{WR}}\text{PR}$     | A1R                  | A0R                  |
| E | A2L                  | A3L                  | $\overline{\text{CE}}\text{0L}$     | CE1L                               | VDDIOL                           | VDDIOL                             | VDDIOL | VCORE                           | VCORE                           | VDDIOR               | VDDIOR                             | VDDIOR                            | CE1R                               | $\overline{\text{CE}}\text{0R}$     | A3R                  | A2R                  |
| F | A4L                  | A5L                  | $\overline{\text{CNT}}\text{INTL}$  | $\overline{\text{BE}}\text{3L}$    | VDDIOL                           | VSS                                | VSS    | VSS                             | VSS                             | VSS                  | VSS                                | VDDIOR                            | $\overline{\text{BE}}\text{3R}$    | $\overline{\text{CNT}}\text{INTR}$  | A5R                  | A4R                  |
| G | A6L                  | A7L                  | $\overline{\text{BUS}}\text{YL}$    | $\overline{\text{BE}}\text{2L}$    | ZQ0L <sup>[13]</sup>             | VSS                                | VSS    | VSS                             | VSS                             | VSS                  | VSS                                | VDDIOR                            | $\overline{\text{BE}}\text{2R}$    | $\overline{\text{BUS}}\text{YR}$    | A7R                  | A6R                  |
| H | A8L                  | A9L                  | CL                                  | VTTL                               | VCORE                            | VSS                                | VSS    | VSS                             | VSS                             | VSS                  | VSS                                | VCORE                             | VTTL                               | CR                                  | A9R                  | A8R                  |
| J | A10L                 | A11L                 | VSS                                 | PORTSTD1L                          | VCORE                            | VSS                                | VSS    | VSS                             | VSS                             | VSS                  | VSS                                | VCORE                             | PORTSTD1R                          | VSS                                 | A11R                 | A10R                 |
| K | A12L                 | A13L                 | $\overline{\text{OE}}\text{L}$      | $\overline{\text{BE}}\text{1L}$    | VDDIOL                           | VSS                                | VSS    | VSS                             | VSS                             | VSS                  | VSS                                | VDDIOR                            | $\overline{\text{BE}}\text{1R}$    | $\overline{\text{OE}}\text{R}$      | A13R                 | A12R                 |
| L | A14L                 | A15L                 | $\overline{\text{AD}}\text{SL}$     | $\overline{\text{BE}}\text{0L}$    | VDDIOL                           | VSS                                | VSS    | VSS                             | VSS                             | VSS                  | VSS                                | VDDIOR                            | $\overline{\text{BE}}\text{0R}$    | $\overline{\text{AD}}\text{SR}$     | A15R                 | A14R                 |
| M | A16L <sup>[16]</sup> | A17L <sup>[15]</sup> | $\overline{\text{R}}\text{WL}$      | CQENL                              | VDDIOL                           | VDDIOL                             | VDDIOL | VCORE                           | VCORE                           | VDDIOR               | VDDIOR                             | VDDIOR                            | CQENR                              | $\overline{\text{R}}\text{WR}$      | A17R <sup>[15]</sup> | A16R <sup>[16]</sup> |
| N | A18L <sup>[14]</sup> | DNU                  | $\overline{\text{CNT}}\text{/MSKL}$ | VREFL                              | PORTSTD0L                        | $\overline{\text{READY}}\text{L}$  | DNU    | VTTL                            | VTTL                            | DNU                  | $\overline{\text{READY}}\text{R}$  | PORTSTD0R                         | VREFR                              | $\overline{\text{CNT}}\text{/MSKR}$ | DNU                  | A18R <sup>[14]</sup> |
| P | DQ16L                | DQ17L                | $\overline{\text{CNT}}\text{ENL}$   | $\overline{\text{CNTR}}\text{STL}$ | CQ0L                             | $\overline{\text{CQ}}\text{0L}$    | TCK    | TMS                             | TDO                             | TDI                  | $\overline{\text{CQ}}\text{0R}$    | CQ0R                              | $\overline{\text{CNTR}}\text{STR}$ | $\overline{\text{CNT}}\text{ENR}$   | DQ17R                | DQ16R                |
| R | DQ15L                | DQ13L                | DQ11L                               | DQ9L                               | DQ7L                             | DQ5L                               | DQ3L   | DQ1L                            | DQ1R                            | DQ3R                 | DQ5R                               | DQ7R                              | DQ9R                               | DQ11R                               | DQ13R                | DQ15R                |
| T | DQ14L                | DQ12L                | DQ10L                               | DQ8L                               | DQ6L                             | DQ4L                               | DQ2L   | DQ0L                            | DQ0R                            | DQ2R                 | DQ4R                               | DQ6R                              | DQ8R                               | DQ10R                               | DQ12R                | DQ14R                |

**Notes**

13. Leave this ball unconnected to disable VIM.  
 14. Leave this ball unconnected for CYD09S36V18 and CYD02S36V18.  
 15. Leave this ball unconnected for CYD02S36V18.  
 16. Leave this ball unconnected for CYD02S36V18.

**Figure 5. FullFlex18 SDR 256-ball BGA (Top View)**

|   | 1                    | 2                    | 3                            | 4                        | 5                    | 6                           | 7      | 8                        | 9                        | 10                   | 11                          | 12        | 13                          | 14                           | 15                   | 16                   |
|---|----------------------|----------------------|------------------------------|--------------------------|----------------------|-----------------------------|--------|--------------------------|--------------------------|----------------------|-----------------------------|-----------|-----------------------------|------------------------------|----------------------|----------------------|
| A | DNU                  | DNU                  | DNU                          | DQ17L                    | DQ16L                | DQ13L                       | DQ12L  | DQ9L                     | DQ9R                     | DQ12R                | DQ13R                       | DQ16R     | DQ17R                       | DNU                          | DNU                  | DNU                  |
| B | DNU                  | DNU                  | DNU                          | DNU                      | DQ15L                | DQ14L                       | DQ11L  | DQ10L                    | DQ10R                    | DQ11R                | DQ14R                       | DQ15R     | DNU                         | DNU                          | DNU                  | DNU                  |
| C | DNU                  | DNU                  | $\overline{\text{RETL}}$     | $\overline{\text{INTL}}$ | CQ1L                 | $\overline{\text{CQ1L}}$    | DNU    | $\overline{\text{TRST}}$ | $\overline{\text{MRST}}$ | ZQ0R <sup>[17]</sup> | $\overline{\text{CQ1R}}$    | CQ1R      | $\overline{\text{INTR}}$    | $\overline{\text{RETR}}$     | DNU                  | DNU                  |
| D | A0L                  | A1L                  | $\overline{\text{WRPL}}$     | VREFL                    | FTSELL               | $\overline{\text{LOWSPDL}}$ | VSS    | VTTL                     | VTTL                     | VSS                  | $\overline{\text{LOWSPDR}}$ | FTSELR    | VREFR                       | $\overline{\text{WRPR}}$     | A1R                  | A0R                  |
| E | A2L                  | A3L                  | $\overline{\text{CE0L}}$     | CE1L                     | VDDIOL               | VDDIOL                      | VDDIOL | VCORE                    | VCORE                    | VDDIOR               | VDDIOR                      | VDDIOR    | CE1R                        | $\overline{\text{CE0R}}$     | A3R                  | A2R                  |
| F | A4L                  | A5L                  | $\overline{\text{CNTINTL}}$  | DNU                      | VDDIOL               | VSS                         | VSS    | VSS                      | VSS                      | VSS                  | VSS                         | VDDIOR    | DNU                         | $\overline{\text{CNTINTR}}$  | A5R                  | A4R                  |
| G | A6L                  | A7L                  | $\overline{\text{BUSYL}}$    | DNU                      | ZQ0L <sup>[17]</sup> | VSS                         | VSS    | VSS                      | VSS                      | VSS                  | VSS                         | VDDIOR    | DNU                         | $\overline{\text{BUSYR}}$    | A7R                  | A6R                  |
| H | A8L                  | A9L                  | CL                           | VTTL                     | VCORE                | VSS                         | VSS    | VSS                      | VSS                      | VSS                  | VSS                         | VCORE     | VTTL                        | CR                           | A9R                  | A8R                  |
| J | A10L                 | A11L                 | VSS                          | PORTSTD1L                | VCORE                | VSS                         | VSS    | VSS                      | VSS                      | VSS                  | VSS                         | VCORE     | PORTSTD1R                   | VSS                          | A11R                 | A10R                 |
| K | A12L                 | A13L                 | $\overline{\text{OEL}}$      | $\overline{\text{BE1L}}$ | VDDIOL               | VSS                         | VSS    | VSS                      | VSS                      | VSS                  | VSS                         | VDDIOR    | $\overline{\text{BE1R}}$    | $\overline{\text{OER}}$      | A13R                 | A12R                 |
| L | A14L                 | A15L                 | $\overline{\text{ADSL}}$     | $\overline{\text{BE0L}}$ | VDDIOL               | VSS                         | VSS    | VSS                      | VSS                      | VSS                  | VSS                         | VDDIOR    | $\overline{\text{BE0R}}$    | $\overline{\text{ADSR}}$     | A15R                 | A14R                 |
| M | A16L                 | A17L                 | $\overline{\text{R/WL}}$     | CQENL                    | VDDIOL               | VDDIOL                      | VDDIOL | VCORE                    | VCORE                    | VDDIOR               | VDDIOR                      | VDDIOR    | CQENR                       | $\overline{\text{R/WR}}$     | A17R                 | A16R                 |
| N | A18L <sup>[19]</sup> | A19L <sup>[18]</sup> | $\overline{\text{CNT/MSKL}}$ | VREFL                    | PORTSTD0L            | $\overline{\text{READYL}}$  | DNU    | VTTL                     | VTTL                     | DNU                  | $\overline{\text{READYR}}$  | PORTSTD0R | VREFR                       | $\overline{\text{CNT/MSKR}}$ | A19R <sup>[18]</sup> | A18R <sup>[19]</sup> |
| P | DNU                  | DNU                  | CNTENL                       | CNTRSTL                  | CQ0L                 | CQ0L                        | TCK    | TMS                      | TDO                      | TDI                  | $\overline{\text{CQ0R}}$    | CQ0R      | $\overline{\text{CNTRSTR}}$ | $\overline{\text{CNTENR}}$   | DNU                  | DNU                  |
| R | DNU                  | DNU                  | DNU                          | DNU                      | DQ6L                 | DQ5L                        | DQ2L   | DQ1L                     | DQ1R                     | DQ2R                 | DQ5R                        | DQ6R      | DNU                         | DNU                          | DNU                  | DNU                  |
| T | DNU                  | DNU                  | DNU                          | DQ8L                     | DQ7L                 | DQ4L                        | DQ3L   | DQ0L                     | DQ0R                     | DQ3R                 | DQ4R                        | DQ7R      | DQ8R                        | DNU                          | DNU                  | DNU                  |

**Notes**

17. Leave this ball unconnected to disable VIM.  
 18. Leave this ball unconnected for CYD09S18V18.  
 19. Leave this ball unconnected for CYD04S18V18.

## Selection Guide

| Parameter                                                     | -200                | -167                | Unit |
|---------------------------------------------------------------|---------------------|---------------------|------|
| $f_{MAX}^{[21]}$                                              | 200                 | 167                 | MHz  |
| Maximum access time (clock to data)                           | 3.3                 | 4.0                 | ns   |
| Typical operating current $I_{CC}$                            | 800 <sup>[20]</sup> | 700 <sup>[20]</sup> | mA   |
| Typical standby current for $I_{SB3}$ (both ports CMOS level) | 210 <sup>[20]</sup> | 210 <sup>[20]</sup> | mA   |

## Pin Definitions

| Left Port              | Right Port             | Description                                                                                                                                                                                                                                                                                                                                                       |
|------------------------|------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| A[20:0] <sub>L</sub>   | A[20:0] <sub>R</sub>   | <b>Address inputs.</b> <sup>[22]</sup>                                                                                                                                                                                                                                                                                                                            |
| DQ[71:0] <sub>L</sub>  | DQ[71:0] <sub>R</sub>  | <b>Data bus input and output.</b> <sup>[23]</sup>                                                                                                                                                                                                                                                                                                                 |
| $\overline{BE}[7:0]_L$ | $\overline{BE}[7:0]_R$ | <b>Byte select inputs.</b> <sup>[24]</sup> Asserting these signals enables read and write operations to the corresponding bytes of the memory array.                                                                                                                                                                                                              |
| $\overline{BUSY}_L$    | $\overline{BUSY}_R$    | <b>Port busy output.</b> When there is an address match and both chip enables are active for both ports, an external BUSY signal is asserted on the fifth clock cycles from when the collision occurs.                                                                                                                                                            |
| C <sub>L</sub>         | C <sub>R</sub>         | <b>Clock signal.</b> Maximum clock input rate is $f_{MAX}$ .                                                                                                                                                                                                                                                                                                      |
| $\overline{CE0}_L$     | $\overline{CE0}_R$     | <b>Active LOW chip enable input.</b>                                                                                                                                                                                                                                                                                                                              |
| CE1 <sub>L</sub>       | CE1 <sub>R</sub>       | <b>Active HIGH chip enable input.</b>                                                                                                                                                                                                                                                                                                                             |
| CQEN <sub>L</sub>      | CQEN <sub>R</sub>      | <b>Echo clock enable input.</b> Assert HIGH to enable echo clocking on respective port.                                                                                                                                                                                                                                                                           |
| CQ0 <sub>L</sub>       | CQ0 <sub>R</sub>       | <b>Echo clock signal output for DQ[35:0] for FullFlex72 devices.</b> Echo clock signal output for DQ[17:0] for FullFlex36 devices. Echo clock signal output for DQ[8:0] for FullFlex18 devices.                                                                                                                                                                   |
| $\overline{CQ0}_L$     | $\overline{CQ0}_R$     | <b>Inverted echo clock signal output for DQ[35:0] for FullFlex72 devices.</b> Inverted echo clock signal output for DQ[17:0] for FullFlex36 devices. Inverted echo clock signal output for DQ[8:0] for FullFlex18 devices.                                                                                                                                        |
| CQ1 <sub>L</sub>       | CQ1 <sub>R</sub>       | <b>Echo clock signal output for DQ[71:36] for FullFlex72 devices.</b> Echo clock signal output for DQ[35:18] for FullFlex36 devices. Echo clock signal output for DQ[17:9] for FullFlex18 devices.                                                                                                                                                                |
| $\overline{CQ1}_L$     | $\overline{CQ1}_R$     | <b>Inverted echo clock signal output for DQ[71:36] for FullFlex72 devices.</b> Inverted echo clock signal output for DQ[35:18] for FullFlex36 devices. Inverted echo clock signal output for DQ[17:9] for FullFlex18 devices.                                                                                                                                     |
| ZQ[1:0] <sub>L</sub>   | ZQ[1:0] <sub>R</sub>   | <b>VIM output impedance matching input.</b> <sup>[25]</sup> To use, connect a calibrating resistor between ZQ and ground. The resistor must be five times larger than the intended line impedance driven by the dual port. Assert HIGH or leave DNU to disable VIM.                                                                                               |
| $\overline{OE}_L$      | $\overline{OE}_R$      | <b>Output enable input.</b> This asynchronous signal must be asserted LOW to enable the DQ data pins during read operations.                                                                                                                                                                                                                                      |
| $\overline{INT}_L$     | $\overline{INT}_R$     | <b>Mailbox interrupt flag output.</b> The mailbox permits communications between ports. The upper two memory locations are used for message passing. $\overline{INT}_L$ is asserted LOW when the right port writes to the mailbox location of the left port, and vice versa. An interrupt to a port is deasserted HIGH when it reads the contents of its mailbox. |
| $\overline{LowSPD}_L$  | $\overline{LowSPD}_R$  | <b>Port low speed select input.</b> Assert this pin LOW to disable the DLL. In flow through mode, this pin needs to be asserted low.                                                                                                                                                                                                                              |

### Notes

20. For 18 Mbit x72 commercial configuration only, refer to [Electrical Characteristics on page 19](#) for complete information.

21. SDR mode with two pipelined stages.

22. The CYD36S18V18 device has 21 address bits. The CYD36S36V18 and CYD18S18V18 devices have 20 address bits. The CYD36S72V18, CYD18S36V18, and CYD09S18V18 devices have 19 address bits. The CYD18S72V18 and CYD09S36V18 devices have 18 address bits. The CYD09S72V18 device has 17 address bits. The CYD02S36V18 has 16 address bits.

23. The FullFlex72 family of devices has 72 data lines. The FullFlex36 family of devices has 36 data lines. The FullFlex18 family of devices has 18 data lines.

24. The FullFlex72 family of devices has eight byte enables. The FullFlex36 family of devices has four byte enables. The FullFlex18 family of devices has two byte enables.

25. The pin ZQ[1] is applicable only for 36 Mbit devices. This pin is DNU for 18 Mbit and lower density devices.

**Pin Definitions** *(continued)*

| Left Port                                 | Right Port                                | Description                                                                                                                                                                                                                                                                      |
|-------------------------------------------|-------------------------------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| PORTSTD[1:0] <sub>L</sub> <sup>[26]</sup> | PORTSTD[1:0] <sub>R</sub> <sup>[26]</sup> | <b>Port clock/Address/Control/Data/Echo clock/I/O standard select input.</b> Assert these pins LOW/LOW for LVTTL, LOW/HIGH for HSTL, HIGH/LOW for 2.5 V LVCMOS, and HIGH/HIGH for 1.8 V LVCMOS, respectively. These pins are driven by VTTL referenced levels.                   |
| R/W <sub>L</sub>                          | R/W <sub>R</sub>                          | <b>Read/Write enable input.</b> Assert this pin LOW to write to, or HIGH to read from the dual port memory array.                                                                                                                                                                |
| READY <sub>L</sub>                        | READY <sub>R</sub>                        | <b>Port DLL ready output.</b> This signal is asserted LOW when the DLL and variable impedance matching circuits complete calibration. This is a wired OR capable output.                                                                                                         |
| CNT/MSK <sub>L</sub>                      | CNT/MSK <sub>R</sub>                      | <b>Port counter/Mask select input.</b> Counter control input.                                                                                                                                                                                                                    |
| ADS <sub>L</sub>                          | ADS <sub>R</sub>                          | <b>Port counter address load strobe input.</b> Counter control input.                                                                                                                                                                                                            |
| CNTEN <sub>L</sub>                        | CNTEN <sub>R</sub>                        | <b>Port counter enable input.</b> Counter control input.                                                                                                                                                                                                                         |
| CNTRST <sub>L</sub>                       | CNTRST <sub>R</sub>                       | <b>Port counter reset input.</b> Counter control input.                                                                                                                                                                                                                          |
| CNTINT <sub>L</sub>                       | CNTINT <sub>R</sub>                       | <b>Port counter interrupt output.</b> This pin is asserted LOW one cycle before the unmasked portion of the counter is incremented to all "1s".                                                                                                                                  |
| WRP <sub>L</sub>                          | WRP <sub>R</sub>                          | <b>Port counter wrap input.</b> When the burst counter reaches the maximum count, on the next counter increment WRP is set LOW to load the unmasked counter bits to 0. It is set HIGH to load the counter with the value stored in the mirror register.                          |
| RET <sub>L</sub>                          | RET <sub>R</sub>                          | <b>Port counter retransmit input.</b> Assert this pin LOW to reload the initial address for repeated access to the same segment of memory.                                                                                                                                       |
| VREF <sub>L</sub>                         | VREF <sub>R</sub>                         | <b>Port external HSTL IO reference input.</b> This pin is left DNU when HSTL is not used.                                                                                                                                                                                        |
| VDDIO <sub>L</sub>                        | VDDIO <sub>R</sub>                        | <b>Port data IO power supply.</b>                                                                                                                                                                                                                                                |
| FTSEL <sub>L</sub>                        | FTSEL <sub>R</sub>                        | <b>Port flow through mode select input.</b> Assert this pin LOW to select flow through mode. Assert this pin HIGH to select Pipelined mode.                                                                                                                                      |
| MRST                                      |                                           | <b>Master reset input.</b> MRST is an asynchronous input signal and affects both ports. Asserting MRST LOW performs all of the reset functions as described in the text. A MRST operation is required at power up. This pin is driven by a VDDIO <sub>L</sub> referenced signal. |
| TMS                                       |                                           | <b>JTAG test mode select input.</b> It controls the advance of JTAG TAP state machine. State machine transitions occur on the rising edge of TCK. Operation for LVTTL or 2.5 V LVCMOS.                                                                                           |
| TDI                                       |                                           | <b>JTAG test data input.</b> Data on the TDI input is shifted serially into selected registers. Operation for LVTTL or 2.5 V LVCMOS.                                                                                                                                             |
| TRST                                      |                                           | <b>JTAG reset input.</b> Operation for LVTTL or 2.5 V LVCMOS.                                                                                                                                                                                                                    |
| TCK                                       |                                           | <b>JTAG test clock input.</b> Operation for LVTTL or 2.5 V LVCMOS.                                                                                                                                                                                                               |
| TDO                                       |                                           | <b>JTAG test data output.</b> TDO transitions occur on the falling edge of TCK. TDO is normally tri-stated except when captured data is shifted out of the JTAG TAP. Operation for LVTTL or 2.5 V LVCMOS.                                                                        |
| VSS                                       |                                           | <b>Ground inputs.</b>                                                                                                                                                                                                                                                            |
| VCORE                                     |                                           | <b>Device core power supply.</b>                                                                                                                                                                                                                                                 |
| VTTL                                      |                                           | <b>LVTTL power supply.</b>                                                                                                                                                                                                                                                       |

**Note**

26. PORTSTD[1:0]<sub>L</sub> and PORTSTD[1:0]<sub>R</sub> have internal pull-down resistors.

## Selectable IO Standard

The FullFlex device families offer the option to choose one of the four port standards for the device. Each port independently selects standards from single ended HSTL class I, single ended LVTTTL, 2.5 V LVCMOS, or 1.8 V LVCMOS. The selection of the standard is determined by the PORTSTD pins for each port. These pins must be connected to an LVTTTL power supply. This determines the input clock, address, control, data, and Echo clock standard for each port as shown in [Table 1](#).

**Table 1. Port Standard Selection**

| PORTSTD1 | PORTSTD0 | I/O Standard |
|----------|----------|--------------|
| VSS      | VSS      | LVTTTL       |
| VSS      | VTTTL    | HSTL         |
| VTTTL    | VSS      | 2.5 V LVCMOS |
| VTTTL    | VTTTL    | 1.8 V LVCMOS |

## Clocking

Separate clocks synchronize the operations on each port. Each port has one clock input C. In this mode, all the transactions on the address, control, and data are on the C rising edge. All transactions on the address, control, data input, output, and byte enables occur on the C rising edge.

**Table 2. Data Pin Assignment**

| BE Pin Name        | Data Pin Name |
|--------------------|---------------|
| $\overline{BE}[7]$ | DQ[71:63]     |
| $\overline{BE}[6]$ | DQ[62:54]     |
| $\overline{BE}[5]$ | DQ[53:45]     |
| $\overline{BE}[4]$ | DQ[44:36]     |
| $\overline{BE}[3]$ | DQ[35:27]     |
| $\overline{BE}[2]$ | DQ[26:18]     |
| $\overline{BE}[1]$ | DQ[17:9]      |
| $\overline{BE}[0]$ | DQ[8:0]       |

## Selectable Pipelined or Flow through Mode

To meet data rate and throughput requirements, the FullFlex families offer selectable pipelined or flow through mode. Echo clocks are not supported in flow through mode and the DLL must be disabled.

Flow through mode is selected by the  $\overline{FTSEL}$  pin. Strapping this pin HIGH selects pipelined mode. Strapping this pin LOW selects flow through mode.

## DLL

The FullFlex families of devices have an on-chip DLL. Enabling the DLL reduces the clock to data valid ( $t_{CD}$ ) time enabling more setup time for the receiving device. In flow through mode, the DLL must be disabled. This is selectable by strapping LowSPD low.

Whenever the operating frequency is altered beyond the Clock Input Cycle to Cycle Jitter specification, reset the DLL, followed by 1024 clocks before any valid operation.

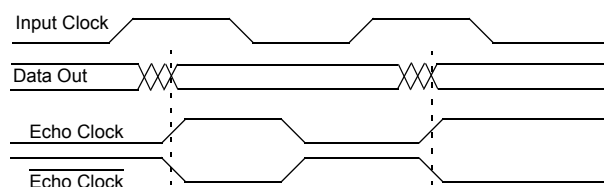
LowSPD pins are used to reset the DLLs for a single port independent of all other circuitry. MRST is used to reset all DLLs on the chip. For more information on DLL lock and reset time, see [Master Reset on page 18](#).

## Echo Clocking

As the speed of data increases, on-board delays caused by parasitics make it extremely difficult to provide accurate clock trees. To counter this problem, the FullFlex families incorporate Echo Clocks. Echo Clocks are enabled on a per port basis. The dual port receives input clocks that are used to clock in the address and control signals for a read operation. The dual port retransmits the input clocks relative to the data output. The buffered clocks are provided on the CQ1/CQ1 and CQ0/CQ0 outputs. Each port has a pair of Echo clocks. Each clock is associated with half the data bits. The output clock matches the corresponding ports IO configuration.

To enable echo clock outputs, tie CQEN HIGH. To disable echo clock outputs, tie CQEN LOW.

**Figure 6. SDR Echo Clock Delay**



## Deterministic Access Control

Deterministic Access Control is provided for ease of design. The circuitry detects when both ports access the same location and provides an external BUSY flag to the port on which data is corrupted. The collision detection logic saves the address in conflict (Busy Address) to a readable register. In the case of multiple collisions, the first busy address is written to the busy address register.

If both ports access the same location at the same time and only one port is doing a write, if  $t_{CCS}$  is met, then the data written to and read from the address is valid data. For example, if the right port is reading and the left port is writing and the left ports clock meets  $t_{CCS}$ , then the data read from the address by the right port is the old data. In the same case, if the right ports clock meets  $t_{CCS}$ , then the data read out of the address from the right port is the new data. In the above case, if  $t_{CCS}$  is violated by the either ports clock with respect to the other port and the right port gets the external BUSY flag, the data from the right port is corrupted. [Table 3 on page 12](#) shows the  $t_{CCS}$  timing that must be met to guarantee the data.

[Table 4 on page 12](#) shows that, in the case of the left port writing and the right port reading, when an external BUSY flag is asserted on the right port, the data read out of the device is not guaranteed.

The value in the busy address register is read back to the address lines. The required input control signals for this function are shown in [Table 7 on page 14](#). The value in the busy address register is read out to the address lines  $t_{CA}$  after the same amount of latency as a data read operation. After an initial address match, the BUSY flag is asserted and the address under contention is saved in the busy address register. All the following

address matches enable to generate the  $\overline{\text{BUSY}}$  flag. However, none of the addresses are saved into the busy address register. When a busy readback is performed, the address of the first

match that happens at least two clocks cycles after the busy readback is saved into the busy address register.

**Table 3.  $t_{\text{CCS}}$  Timing for All Operating Modes**

| Port A—Early Arriving Port |             | Port B—Late Arriving Port |             | $t_{\text{CCS}}$<br>C Rise to Opposite C Rise Setup Time for Non Corrupt Data | Unit |
|----------------------------|-------------|---------------------------|-------------|-------------------------------------------------------------------------------|------|
| Mode                       | Active Edge | Mode                      | Active Edge |                                                                               |      |
| SDR                        | C           | SDR                       | C           | $t_{\text{CYC}(\text{min})} - 0.5$                                            | ns   |

**Table 4. Deterministic Access Control Logic**

| Left Port | Right Port | Left Clock         | Right Clock                                 | $\text{BUSY}_L$ | $\text{BUSY}_R$ | Description                  |
|-----------|------------|--------------------|---------------------------------------------|-----------------|-----------------|------------------------------|
| Read      | Read       | X                  | X                                           | H               | H               | No collision                 |
| Write     | Read       | $> t_{\text{CCS}}$ | 0                                           | H               | H               | Read OLD data                |
|           |            | 0                  | $> t_{\text{CCS}}$                          | H               | H               | Read NEW data                |
|           |            | $< t_{\text{CCS}}$ | 0                                           | H               | H               | Read OLD data                |
|           |            |                    |                                             | H               | L               | Data not guaranteed          |
|           |            | 0                  | $< t_{\text{CCS}}$                          | H               | H               | Read NEW data                |
|           |            |                    |                                             | H               | L               | Data Not guaranteed          |
| Read      | Write      | $> t_{\text{CCS}}$ | 0                                           | H               | H               | Read NEW data                |
|           |            | 0                  | $> t_{\text{CCS}}$                          | H               | H               | Read OLD data                |
|           |            | $< t_{\text{CCS}}$ | 0                                           | H               | H               | Read NEW data                |
|           |            |                    |                                             | L               | H               | Data Not guaranteed          |
|           |            | 0                  | $< t_{\text{CCS}}$                          | H               | H               | Read OLD data                |
|           |            |                    |                                             | L               | H               | Data not guaranteed          |
| Write     | Write      | 0                  | $> -t_{\text{CCS}} \ \& \ < t_{\text{CCS}}$ | L               | L               | Array data corrupted         |
|           |            | 0                  | $> t_{\text{CCS}}$                          | L               | H               | Array stores right port data |
|           |            | $> t_{\text{CCS}}$ | 0                                           | H               | L               | Array stores left port data  |

## Variable Impedance Matching

Each port contains a variable impedance matching circuit to set the impedance of the IO driver to match the impedance of the on-board traces. The impedance is set for all outputs except JTAG and is done by port. To take advantage of the VIM feature, connect a calibrating resistor (RQ) that is five times the value of the intended line impedance from the  $\text{ZQ}_{[1:0]}$ <sup>[27]</sup> pin to  $V_{\text{SS}}$ . The output impedance is then adjusted to account for drifts in supply voltage and temperature every 1024 clock cycles. If a port's clock is suspended, the VIM circuit retains its last setting until the clock is restarted. On restart, it then resumes periodic adjustment. In the case of a significant change in device temperature or supply voltage, recalibration happens every 1024 clock cycles. A master reset initializes the VIM circuitry. Table 5 shows the VIM parameters and Table 6 describes the VIM operation modes.

To disable VIM, connect the ZQ pin to VDDIO of the relative supply for the IOs before a Master Reset.

**Table 5. Variable Impedance Matching Parameters**

| Parameter        | Min | Max  | Unit     | Tolerance  |
|------------------|-----|------|----------|------------|
| RQ value         | 100 | 275  | $\Omega$ | $\pm 2\%$  |
| Output impedance | 20  | 55   | $\Omega$ | $\pm 15\%$ |
| Reset time       | —   | 1024 | Cycles   | —          |
| Update time      | —   | 1024 | Cycles   | —          |

**Table 6. Variable Impedance Matching Operation**

| RQ Connection                                 | Output Configuration                                                                     |
|-----------------------------------------------|------------------------------------------------------------------------------------------|
| 100 $\Omega$ –275 $\Omega$ to $V_{\text{SS}}$ | Output driver impedance = $\text{RQ}/5 \pm 15\%$ at $V_{\text{out}} = V_{\text{DDIO}}/2$ |
| ZQ to VDDIO                                   | VIM disabled. $\text{Rout} \leq 20 \ \Omega$ at $V_{\text{out}} = V_{\text{DDIO}}/2$     |

### Note

27. The pin  $\text{ZQ}[1]$  is applicable only for 36 Mbit devices. This pin is DNU for 18 Mbit and lower density devices.

## Address Counter and Mask Register Operations <sup>[28]</sup>

Each port of the FullFlex family contains a programmable burst address counter. The burst counter contains four registers: a counter register, a mask register, a mirror register, and a busy address register.

The **counter register** contains the address used to access the RAM array. It is changed only by the master reset (MRST), counter reset, counter load, retransmit, and counter increment operations.

The **mask register** value affects the counter increment and counter reset operations by preventing the corresponding bits of the counter register from changing. It also affects the counter interrupt output (CNTINT). The **mask register** is only changed by mask reset, mask load, and MRST. The mask load operation loads the value of the address bus into the mask register. The mask register defines the counting range of the counter register. The mask register is divided into two or three consecutive regions. Zero or more 0s define the masked region and one or more 1s define the unmasked portion of the counter register. The counter register may be divided up to three regions. The region containing the least significant bits must be no more than two 0s. Bits one and zero may be 10 respectively, masking the least significant counter bit and causing the counter to increment by two instead of one. If bits one and zero are 00, the two least significant bits are masked and the counter increments by four instead of one. For example, in the case of a 256 K × 72 configuration, a mask register value of 003FC divides the mask register into three regions. With bit 0 being the least significant bit and bit 17 being the most significant bit, the two least significant bits are masked, the next eight bits are unmasked, and the remaining bits are masked.

The **mirror register** reloads a counter register on retransmit operations (see [Retransmit on page 15](#)) and wrap functions (see [Counter Interrupt on page 15](#) below). The last value loaded into the counter register is stored in the mirror register. The mirror register is only changed by master reset (MRST), counter reset, and counter load.

[Table 7 on page 14](#) summarizes the operations of these registers and the required input control signals. All signals except MRST are synchronized to the ports clock.

## Counter Load Operation <sup>[28]</sup>

For both non-burst and burst read or write accesses, the external address is loaded through counter load operation as shown in [Table 7 on page 14](#). The address counter and mirror registers are loaded with the address value presented on the address lines. This value ranges from 0 to 1FFFFFF.

## Mask Load Operation <sup>[28]</sup>

The mask register is loaded with the address value presented on the address bus. This value ranges from 0 to 1FFFFFF though not all values permit correct increment operations. Permitted values are in the form of  $2^n-1$ ,  $2^n-2$ , or  $2^n-4$ . The counter register is only segmented up to three regions. From the most significant bit to the least significant bit, permitted values have zero or more 0s, one or more 1s, and the least significant two bits are 11, 10, or 00. Thus 1FFFFFFE, 07FFFF, and 003FFC are permitted values but 02FFFF, 003FFA, and 07FFE4 are not.

## Counter Readback Operation

The internal value of the counter register is read out on the address lines. The address is valid  $t_{CA}$  after the selected number of latency cycles configured by FTSEL. The data bus (DQ) is tri-stated on the cycle that the address is presented on the address lines. [Figure 7 on page 16](#) shows a block diagram of this logic.

## Mask Readback Operation

The internal value of the mask register is read out on the address lines. The address is valid  $t_{CA}$  after the selected number of latency cycles configured by FTSEL. The data bus (DQ) is tri-stated on the cycle that the address is presented on the address lines. [Figure 7 on page 16](#) shows a block diagram of the operation.

## Counter Reset Operation

All unmasked bits of the counter and mirror registers are reset to '0'. All masked bits remain unchanged. A mask reset followed by a counter reset resets the counter and mirror registers to 00000.

## Mask Reset Operation

The mask register is reset to all 1s, that unmask every bit of the burst counter.

### Note

28. The CYD36S18V18 device has 21 address bits. The CYD36S36V18 and CYD18S18V18 devices have 20 address bits. The CYD36S72V18, CYD18S36V18, and CYD09S18V18 devices have 19 address bits. The CYD18S72V18 and CYD09S36V18 devices have 18 address bits. The CYD09S72V18 device has 17 address bits. The CYD02S36V18 has 16 address bits.

**Table 7. Burst Counter and Mask Register Control Operations**

The burst counter and mask register control operation for any port follows. [29, 30]

| C                                                                                   | MRST | CNTRST | CNT/MSK | CNTEN | ADS | RET | Operation                                                  | Description                                                                           |
|-------------------------------------------------------------------------------------|------|--------|---------|-------|-----|-----|------------------------------------------------------------|---------------------------------------------------------------------------------------|
| X                                                                                   | L    | X      | X       | X     | X   | X   | Master reset                                               | Reset address counter to all 0s, mask register to all 1s, and busy address to all 0s. |
|    | H    | L      | H       | X     | X   | X   | Counter reset                                              | Reset counter and mirror unmasked portion to all 0s.                                  |
|    | H    | L      | L       | X     | X   | X   | Mask reset                                                 | Reset mask register to all 1s.                                                        |
|    | H    | H      | H       | L     | L   | X   | Counter load for burst/external address load for non-burst | Load burst counter and mirror with external address value presented on address lines. |
|    | H    | H      | L       | L     | L   | X   | Mask load                                                  | Load mask register with value presented on the address lines.                         |
|    | H    | H      | H       | L     | H   | L   | Retransmit                                                 | Load counter with value in the mirror register.                                       |
|    | H    | H      | H       | L     | H   | H   | Counter increment                                          | Internally increment address counter value.                                           |
|    | H    | H      | H       | H     | H   | H   | Counter hold                                               | Constantly hold the address value for multiple clock cycles.                          |
|    | H    | H      | H       | H     | L   | H   | Counter readback                                           | Read out counter internal value on address lines.                                     |
|   | H    | H      | L       | H     | L   | H   | Mask readback                                              | Read out mask register value on address lines.                                        |
|  | H    | H      | L       | H     | H   | L   | Busy address readback                                      | Read out first busy address after last busy address readback.                         |
|  | H    | H      | L       | L     | H   | X   | Reserved                                                   |                                                                                       |
|  | H    | H      | L       | H     | L   | L   | Reserved                                                   |                                                                                       |
|  | H    | H      | L       | H     | H   | H   | Reserved                                                   |                                                                                       |
|  | H    | H      | H       | H     | L   | L   | Reserved                                                   |                                                                                       |
|  | H    | H      | H       | H     | H   | L   | Reserved                                                   |                                                                                       |

**Notes**

29. "X" = Don't Care, "H" = HIGH, "L" = LOW.

30. Counter operation and mask register operation is independent of chip enables.

## Increment Operation<sup>[31]</sup>

After the address counter is initially loaded with an external address, the counter can internally increment the address value and address the entire memory array. Only the unmasked bits of the counter register are incremented. For a counter bit to change, the corresponding bit in the mask register must be 1. If the two least significant bits of the mask register are 11, the burst counter increments by one. If the two least significant bits are 10, the burst counter increments by two, and if they are 00, the burst counter increments by four. If all unmasked counter bits are incremented to 1 and WRP is deasserted, the next increment wraps the counter back to the initially loaded value. The cycle before the increment that results in all unmasked counter bits to become 1s, a counter interrupt flag (CNTINT) is asserted if the counter is incremented again. This increment causes the counter to reach its maximum value and the next increment returns the counter register to its initial value that was stored in the mirror register if WRP is deasserted. If WRP is asserted, the unmasked portion of the counter is filled with 0 instead. The example shown in [Figure 8 on page 17](#) shows an example of the CYDD36S18V18 device with the mask register loaded with a mask value of 00007F unmasking the seven least significant bits. Setting the mask register to this value enables the counter to access the entire memory space. The address counter is then loaded with an initial value of 000005 assuming WRP is deasserted. The masked bits, the seventh address through the twenty-first address, do not increment in an increment operation. The counter address starts at address 000005 and increments its internal address value until it reaches the mask register value of 00007F. The counter wraps around the memory block to location 000005 at the next count. CNTINT is issued when the counter reaches the maximum -1 count.

## Hold Operation

The value of all three registers is constantly maintained unchanged for an unlimited number of clock cycles. This operation is useful in applications where wait states are needed or when address is available a few cycles ahead of data in a shared bus interface.

## Retransmit

Retransmit enables repeated access to the same block of memory without the need to reload the initial address. An internal

mirror register stores the address counter value last loaded. While RET is asserted low, the counter continues to wrap back to the value in the mirror register independent of the state of WRP.

## Counter Interrupt

The counter interrupt (CNTINT) is asserted LOW one clock cycle before an increment operation that results in the unmasked portion of the counter register being all 1s. It is deasserted by counter reset, counter load, counter increment, mask reset, mask load, and MRST.

## Counting by Two

When the two least significant bits of the mask register are 10, the counter increments by two.

## Counting by Four

When the two least significant bits of the mask register are 00, the counter increments by four.

## Mailbox Interrupts

Use the upper two memory locations for message passing and permit communications between ports. [Table 8 on page 17](#) shows the interrupt operation for both ports. The highest memory location is the mailbox for the right port and the maximum address - 1 is the mailbox for the left port.

When one port writes to the other port's mailbox, the  $\overline{\text{INT}}$  flag of the port that the mailbox belongs to is asserted LOW. The  $\overline{\text{INT}}$  flag remains asserted until the mailbox location is read by the other port. When a port reads its mailbox, the  $\overline{\text{INT}}$  flag is deasserted high after one cycle of latency with respect to the input clock of the port to which the mailbox belongs and is independent of OE.

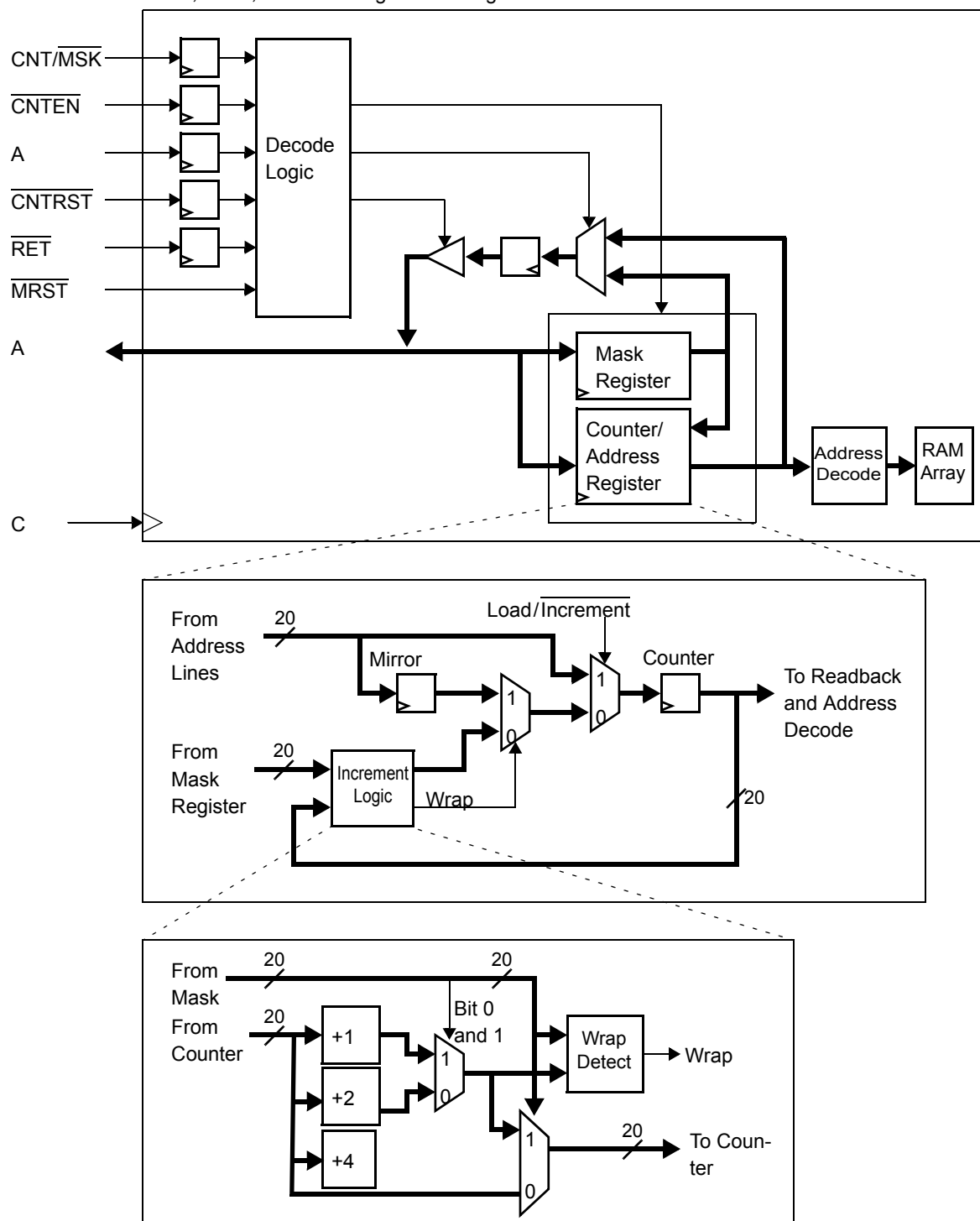
As shown in [Table 8 on page 17](#), to set the  $\overline{\text{INT}}_R$  flag, a write operation by the left port to address 1FFFFFF asserts  $\overline{\text{INT}}_R$  LOW. A valid read of the 1FFFFFF location by the right port resets  $\overline{\text{INT}}_R$  HIGH after one cycle of latency with respect to the right port's clock. You must activate at least one byte enable to set or reset the mailbox interrupt.

### Note

31. The CYD36S18V18 device has 21 address bits. The CYD36S36V18 and CYD18S18V18 devices have 20 address bits. The CYD36S72V18, CYD18S36V18, and CYD09S18V18 devices have 19 address bits. The CYD18S72V18 and CYD09S36V18 devices have 18 address bits. The CYD09S72V18 device has 17 address bits. The CYD02S36V18 has 16 address bits.

**Figure 7. Counter, Mask, and Mirror Logic Block Diagram**

Figure 7 shows the counter, mask, and mirror logic block diagram. [32]

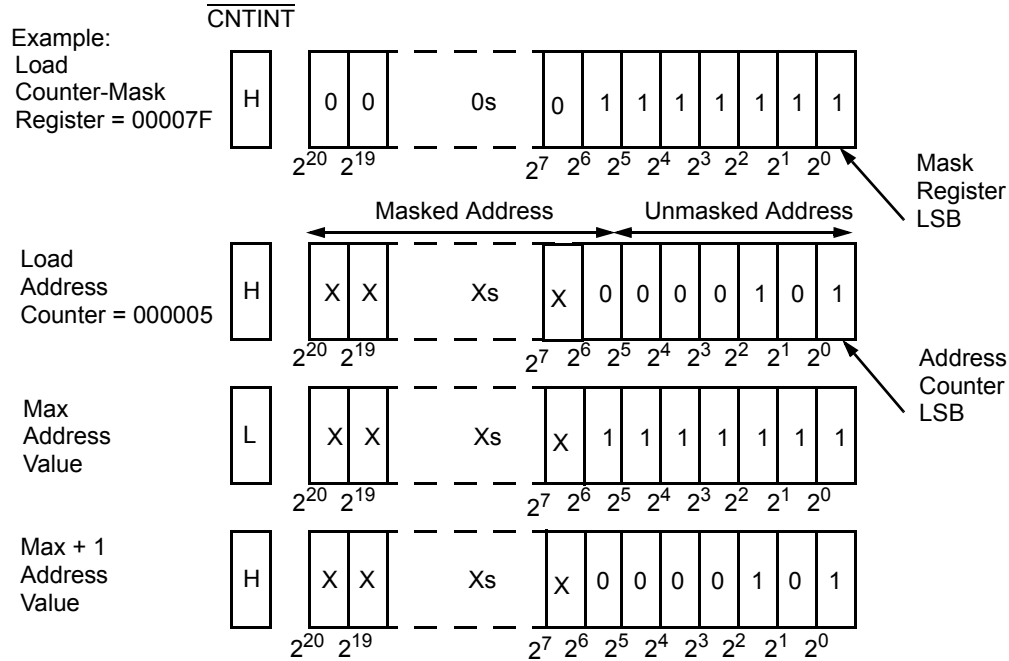


**Note**

32. The CYD36S18V18 device has 21 address bits. The CYD36S36V18 and CYD18S18V18 devices have 20 address bits. The CYD36S72V18, CYD18S36V18, and CYD09S18V18 devices have 19 address bits. The CYD18S72V18 and CYD09S36V18 devices have 18 address bits. The CYD09S72V18 device has 17 address bits. The CYD02S36V18 has 16 address bits.

**Figure 8. Programmable Counter-Mask Register Operation with  $\overline{WRP}$  deasserted**

Figure 8 shows the programmable counter-mask operation with  $\overline{WRP}$  deasserted. [36, 38]



**Table 8. Interrupt Operation Example**

Table 8 shows the interrupt operation example. [33, 34, 35, 37, 38]

| Function                            | Left Port          |                   |               |                    | Right Port         |                   |               |                    |
|-------------------------------------|--------------------|-------------------|---------------|--------------------|--------------------|-------------------|---------------|--------------------|
|                                     | $\overline{R/W}_L$ | $\overline{CE}_L$ | $A_{0L-20L}$  | $\overline{INT}_L$ | $\overline{R/W}_R$ | $\overline{CE}_R$ | $A_{0R-20R}$  | $\overline{INT}_R$ |
| Set Right $\overline{INT}_R$ Flag   | L                  | L                 | Max Address   | X                  | X                  | X                 | X             | L                  |
| Reset Right $\overline{INT}_R$ Flag | X                  | X                 | X             | X                  | H                  | L                 | Max Address   | H                  |
| Set Left $\overline{INT}_L$ Flag    | X                  | X                 | X             | L                  | L                  | L                 | Max Address-1 | X                  |
| Reset Left $\overline{INT}_L$ Flag  | H                  | L                 | Max Address-1 | H                  | X                  | X                 | X             | X                  |

#### Notes

33.  $\overline{CE}$  is internal signal.  $\overline{CE} = \text{LOW}$  if  $\overline{CE}_0 = \text{LOW}$  and  $\overline{CE}_1 = \text{HIGH}$ . For a single read operation,  $\overline{CE}$  only needs to be asserted once at the rising edge of the C and is deasserted after that. Data is out after the following C edge and is tri-stated after the next C edge.
34. OE is "Don't Care" for mailbox operation.
35. At least one of BE0, BE1, BE2, BE3, BE4, BE5, BE6, or BE7 must be LOW.
36. The "X" in this diagram represents the counter's upper bits.
37. "X" = Don't Care, "H" = HIGH, "L" = LOW.
38. The CYD36S18V18 device has 21 address bits. The CYD36S36V18 and CYD18S18V18 devices have 20 address bits. The CYD36S72V18, CYD18S36V18, and CYD09S18V18 devices have 19 address bits. The CYD18S72V18 and CYD09S36V18 devices have 18 address bits. The CYD09S72V18 device has 17 address bits. The CYD02S36V18 has 16 address bits.

## Master Reset

The FullFlex family of Dual Ports undergoes a complete reset when MRST is asserted. MRST must be driven by VDDIO<sub>L</sub> referenced levels. The MRST is asserted asynchronously to the clocks and must remain asserted for at least  $t_{RS}$ . When asserted MRST deasserts READY, initializes the internal burst counters, internal mirror registers, and internal busy addresses to zero. It also initializes the internal mask register to all 1s. All mailbox interrupts (INT), busy address outputs (BUSY), and burst counter interrupts (CNTINT) are deasserted upon master reset. Additionally, do not release MRST until all power supplies including VREF are fully ramped and all port clocks and mode select inputs (LOWSPD, ZQ, CQEN, FTSEL, and PORTSTD) are valid and stable. This begins calibration of the DLL and VIM circuits. READY is asserted within 1024 clock cycles. READY is a wired OR capable output with a strong pull up and weak pull down. Up to four outputs may be connected together. For faster pull down of the signal, connect a 250 Ohm resistor to VSS. If the DLL and VIM circuits are disabled for a port, the port is operational within five clock cycles. However, the READY is asserted within 160 clock cycles.

## IEEE 1149.1 Serial Boundary Scan (JTAG)

The FullFlex families incorporate an IEEE 1149.1 serial boundary scan test access port (TAP). The TAP operates using JEDEC-standard 3.3 V or 2.5 V IO logic levels depending on the VTTL power supply. It is composed of four input connections and

one output connection required by the test logic defined by the standard.

**Table 9. JTAG IDCODE Register Definitions**

| Part Number | Configuration | Value          |
|-------------|---------------|----------------|
| CYD36S72V18 | 512 K × 72    | 0C026069h (×2) |
| CYD36S36V18 | 1024 K × 36   | 0C023069h      |
| CYD36S18V18 | 2048 K × 18   | 0C024069h      |
| CYD18S72V18 | 256 K × 72    | 0C025069h      |
| CYD18S36V18 | 512 K × 36    | 0C026069h      |
| CYD18S18V18 | 1024 K × 18   | 0C027069h      |
| CYD09S72V18 | 128 K × 72    | 0C028069h      |
| CYD09S36V18 | 256 K × 36    | 0C029069h      |
| CYD09S18V18 | 512 K × 18    | 0C02A069h      |
| CYD02S36V18 | 64 K × 36     | 0C030069h      |

**Table 10. Scan Registers Sizes**

| Register Name  | Bit Size   |
|----------------|------------|
| Instruction    | 4          |
| Bypass         | 1          |
| Identification | 32         |
| Boundary Scan  | $n^{[39]}$ |

**Table 11. Instruction Identification Codes**

| Instruction    | Code            | Description                                                                                            |
|----------------|-----------------|--------------------------------------------------------------------------------------------------------|
| EXTEST         | 0000            | Captures the input and output ring contents. Places the BSR between the TDI and TDO.                   |
| BYPASS         | 1111            | Places the BYR between TDI and TDO.                                                                    |
| IDCODE         | 1011            | Loads the IDR with the vendor ID code and places the register between TDI and TDO.                     |
| HIGHZ          | 0111            | Places BYR between TDI and TDO. Forces all FullFlex72 and FullFlex36 output drivers to a High Z state. |
| CLAMP          | 0100            | Controls boundary to 1 or 0. Places BYR between TDI and TDO.                                           |
| SAMPLE/PRELOAD | 1000            | Captures the input and output ring contents. Places BSR between TDI and TDO.                           |
| RESERVED       | All other codes | Other combinations are reserved. Do not use other than the mentioned combinations.                     |

### Note

39. Details of the boundary scan length is found in the BSD file for the device.

## Maximum Ratings

Exceeding maximum ratings may impair the useful life of the device. User guidelines are not tested.

Storage temperature ..... –65 °C to + 150 °C

Ambient temperature with power applied ..... –55 °C to + 125 °C

Supply voltage to ground potential ..... –0.5 V to + 4.1 V

DC voltage applied to outputs in high Z State ..... –0.5 V to  $V_{DDIO} + 0.5 V$

DC input voltage ..... –0.5 V to  $V_{DDIO} + 0.5 V$

Output current into outputs (LOW) ..... 20 mA

Static discharge voltage ..... > 2200 V (JEDEC JESD8-6, JESD8-B)

Latch-up current ..... > 200 mA

## Operating Range

| Range      | Ambient Temperature | V <sub>CORE</sub>               |
|------------|---------------------|---------------------------------|
| Commercial | 0 °C to +70 °C      | 1.8 V ± 100 mV<br>1.5 V ± 80 mV |
| Industrial | –40 °C to +85 °C    | 1.8 V ± 100 mV<br>1.5 V ± 80 mV |

## Power Supply Requirements

|                                | Min    | Typ    | Max    |
|--------------------------------|--------|--------|--------|
| LVTTL V <sub>DDIO</sub>        | 3.0 V  | 3.3 V  | 3.6 V  |
| 2.5 V LVCMOS V <sub>DDIO</sub> | 2.3 V  | 2.5 V  | 2.7 V  |
| HSTL V <sub>DDIO</sub>         | 1.4 V  | 1.5 V  | 1.9 V  |
| 1.8 V LVCMOS V <sub>DDIO</sub> | 1.7 V  | 1.8 V  | 1.9 V  |
| 3.3 V VTTL                     | 3.0 V  | 3.3 V  | 3.6 V  |
| 2.5 V VTTL                     | 2.3 V  | 2.5 V  | 2.7 V  |
| HSTL V <sub>REF</sub>          | 0.68 V | 0.75 V | 0.95 V |

## Electrical Characteristics

Over the Operating Range

| Parameter       | Description                                                            | Configuration             | All Speed Bins                           |     |                          | Unit |
|-----------------|------------------------------------------------------------------------|---------------------------|------------------------------------------|-----|--------------------------|------|
|                 |                                                                        |                           | Min                                      | Typ | Max                      |      |
| V <sub>OH</sub> | Output HIGH voltage (V <sub>DDIO</sub> = Min, I <sub>OH</sub> = –8 mA) | LVTTL                     | 2.4 <sup>[40]</sup>                      | –   | –                        | V    |
|                 | (V <sub>DDIO</sub> = Min, I <sub>OH</sub> = –4 mA)                     | HSTL (DC) <sup>[41]</sup> | V <sub>DDIO</sub> – 0.4 <sup>[40]</sup>  | –   | –                        | V    |
|                 | (V <sub>DDIO</sub> = Min, I <sub>OH</sub> = –4 mA)                     | HSTL (AC) <sup>[41]</sup> | V <sub>DDIO</sub> – 0.5 <sup>[40]</sup>  | –   | –                        | V    |
|                 | (V <sub>DDIO</sub> = Min, I <sub>OH</sub> = –6 mA)                     | 2.5 V LVCMOS              | 1.7 <sup>[40]</sup>                      | –   | –                        | V    |
|                 | (V <sub>DDIO</sub> = Min, I <sub>OH</sub> = –4 mA)                     | 1.8 V LVCMOS              | V <sub>DDIO</sub> – 0.45 <sup>[40]</sup> | –   | –                        | V    |
| V <sub>OL</sub> | Output HIGH voltage (V <sub>DDIO</sub> = Min, I <sub>OL</sub> = 8 mA)  | LVTTL                     | –                                        | –   | 0.4 <sup>[40]</sup>      | V    |
|                 | (V <sub>DDIO</sub> = Min, I <sub>OL</sub> = 4 mA)                      | HSTL(DC) <sup>[41]</sup>  | –                                        | –   | 0.4 <sup>[40]</sup>      | V    |
|                 | (V <sub>DDIO</sub> = Min, I <sub>OL</sub> = 4 mA)                      | HSTL (AC) <sup>[41]</sup> | –                                        | –   | 0.5 <sup>[40]</sup>      | V    |
|                 | (V <sub>DDIO</sub> = Min, I <sub>OL</sub> = 6 mA)                      | 2.5 V LVCMOS              | –                                        | –   | 0.7 <sup>[40]</sup>      | V    |
|                 | (V <sub>DDIO</sub> = Min, I <sub>OL</sub> = 4 mA)                      | 1.8 V LVCMOS              | –                                        | –   | 0.45 <sup>[40]</sup>     | V    |
| V <sub>IH</sub> | Input HIGH voltage                                                     | LVTTL                     | 2                                        | –   | V <sub>DDIO</sub> + 0.3  | V    |
|                 |                                                                        | HSTL(DC) <sup>[41]</sup>  | V <sub>REF</sub> + 0.1                   | –   | V <sub>DDIO</sub> + 0.3  | V    |
|                 |                                                                        | 2.5 V LVCMOS              | 1.7                                      | –   |                          | V    |
|                 |                                                                        | 1.8 V LVCMOS              | 0.65 × V <sub>DDIO</sub>                 | –   |                          | V    |
| V <sub>IL</sub> | Input LOW voltage                                                      | LVTTL                     | –0.3                                     | –   | 0.8                      | V    |
|                 |                                                                        | HSTL(DC) <sup>[41]</sup>  | –0.3                                     | –   | V <sub>REF</sub> – 0.1   | V    |
|                 |                                                                        | 2.5 V LVCMOS              | –                                        | –   | 0.7                      | V    |
|                 |                                                                        | 1.8 V LVCMOS              | –                                        | –   | 0.35 × V <sub>DDIO</sub> | V    |

### Notes

40. These parameters are met with VIM disabled.

41. The DC specifications are measured under steady state conditions. The AC specifications are measured while switching at speed. AC V<sub>IH</sub>/V<sub>IL</sub> in HSTL mode are measured with 1 V/ns input edge rates.

## Electrical Characteristics *(continued)*

Over the Operating Range

| Parameter                             | Description                                                                    | Configuration             | All Speed Bins                    |     |                      | Unit          |
|---------------------------------------|--------------------------------------------------------------------------------|---------------------------|-----------------------------------|-----|----------------------|---------------|
|                                       |                                                                                |                           | Min                               | Typ | Max                  |               |
| $\overline{\text{READY}}$<br>$V_{OH}$ | Output HIGH voltage<br>( $V_{DDIO} = \text{Min}$ , $I_{OH} = -24 \text{ mA}$ ) | LVTTL                     | 2.7 <sup>[42]</sup>               | –   | –                    | V             |
|                                       | ( $V_{DDIO} = \text{Min}$ , $I_{OH} = -12 \text{ mA}$ )                        | HSTL(DC) <sup>[43]</sup>  | $V_{DDIO} - 0.4$ <sup>[42]</sup>  | –   | –                    | V             |
|                                       | ( $V_{DDIO} = \text{Min}$ , $I_{OH} = -12 \text{ mA}$ )                        | HSTL (AC) <sup>[43]</sup> | $V_{DDIO} - 0.5$ <sup>[42]</sup>  | –   | –                    | V             |
|                                       | ( $V_{DDIO} = \text{Min}$ , $I_{OH} = -15 \text{ mA}$ )                        | 2.5 V LVCMOS              | 2.0 <sup>[42]</sup>               | –   | –                    | V             |
|                                       | ( $V_{DDIO} = \text{Min}$ , $I_{OH} = -12 \text{ mA}$ )                        | 1.8 V LVCMOS              | $V_{DDIO} - 0.45$ <sup>[42]</sup> | –   | –                    | V             |
| $\overline{\text{READY}}$<br>$V_{OL}$ | Output HIGH voltage<br>( $V_{DDIO} = \text{Min}$ , $I_O = 0.12 \text{ mA}$ )   | LVTTL                     | –                                 | –   | 0.4 <sup>[42]</sup>  | V             |
|                                       | ( $V_{DDIO} = \text{Min}$ , $I_{OL} = 0.12 \text{ mA}$ )                       | HSTL(DC) <sup>[43]</sup>  | –                                 | –   | 0.4 <sup>[42]</sup>  | V             |
|                                       | ( $V_{DDIO} = \text{Min}$ , $I_{OL} = 0.12 \text{ mA}$ )                       | HSTL (AC) <sup>[43]</sup> | –                                 | –   | 0.5 <sup>[42]</sup>  | V             |
|                                       | ( $V_{DDIO} = \text{Min}$ , $I_{OL} = 0.15 \text{ mA}$ )                       | 2.5 V LVCMOS              | –                                 | –   | 0.7 <sup>[42]</sup>  | V             |
|                                       | ( $V_{DDIO} = \text{Min}$ , $I_{OL} = 0.08 \text{ mA}$ )                       | 1.8 V LVCMOS              | –                                 | –   | 0.45 <sup>[42]</sup> | V             |
| $I_{OZ}$                              | Output leakage current                                                         |                           | –10                               | –   | 10                   | $\mu\text{A}$ |
| $I_{IX1}$                             | Input leakage current except<br>TDI, TMS, MRST, PORTSTD                        |                           | –10                               | –   | 10                   | $\mu\text{A}$ |
| $I_{IX2}$                             | Input leakage current TDI,<br>TMS, MRST                                        |                           | –300                              | –   | 10                   | $\mu\text{A}$ |
| $I_{IX3}$                             | Input leakage current<br>PORTSTD                                               |                           | –10                               | –   | 300                  | $\mu\text{A}$ |

### Notes

42. These parameters are met with VIM disabled.

43. The DC specifications are measured under steady state conditions. The AC specifications are measured while switching at speed. AC VIH/VIL in HSTL mode are measured with 1 V/ns input edge rates.

## Electrical Characteristics

Over the Operating Range

| Parameter       | Description                                                                                 | Configuration |            | -200 |      | -167 |      | Unit |
|-----------------|---------------------------------------------------------------------------------------------|---------------|------------|------|------|------|------|------|
|                 |                                                                                             |               |            | Typ  | Max  | Typ  | Max  |      |
| I <sub>CC</sub> | Operating current<br>(V <sub>CORE</sub> = Max, I <sub>OUT</sub> = 0 mA)<br>outputs disabled | 512 K × 72    | Commercial | 1440 | 1800 | 1280 | 1620 | mA   |
|                 |                                                                                             |               | Industrial | –    | –    | 1330 | 1730 | mA   |
|                 |                                                                                             | 1024 K × 36   | Commercial | 1180 | 1500 | 1050 | 1350 | mA   |
|                 |                                                                                             |               | Industrial | –    | –    | 1110 | 1470 | mA   |
|                 |                                                                                             | 2048 K × 18   | Commercial | 1130 | 1430 | 1000 | 1290 | mA   |
|                 |                                                                                             |               | Industrial | –    | –    | 1060 | 1410 | mA   |
|                 |                                                                                             | 256 K × 72    | Commercial | 800  | 980  | 700  | 880  | mA   |
|                 |                                                                                             |               | Industrial | 820  | 1030 | 730  | 930  | mA   |
|                 |                                                                                             | 512 K × 36    | Commercial | 640  | 800  | 570  | 720  | mA   |
|                 |                                                                                             |               | Industrial | 670  | 860  | 590  | 780  | mA   |
|                 |                                                                                             | 1024 K × 18   | Commercial | 610  | 770  | 540  | 690  | mA   |
|                 |                                                                                             |               | Industrial | 640  | 830  | 570  | 750  | mA   |
|                 |                                                                                             | 128 K × 72    | Commercial | 640  | 790  | 560  | 700  | mA   |
|                 |                                                                                             |               | Industrial | 660  | 830  | 580  | 740  | mA   |
|                 |                                                                                             | 256 K × 36    | Commercial | 540  | 640  | 470  | 570  | mA   |
|                 |                                                                                             |               | Industrial | 550  | 670  | 490  | 600  | mA   |
|                 |                                                                                             | 512 K × 18    | Commercial | 550  | 660  | 480  | 580  | mA   |
|                 |                                                                                             |               | Industrial | 570  | 690  | 500  | 610  | mA   |
|                 |                                                                                             | 64 K × 36     | Commercial | –    | –    | –    | –    | mA   |
|                 |                                                                                             |               | Industrial | –    | –    | –    | –    | mA   |

## Electrical Characteristics *(continued)*

Over the Operating Range

| Parameter        | Description                                                                                                               | Configuration |            | -200 |      | -167 |      | Unit |
|------------------|---------------------------------------------------------------------------------------------------------------------------|---------------|------------|------|------|------|------|------|
|                  |                                                                                                                           |               |            | Typ  | Max  | Typ  | Max  |      |
| I <sub>SB1</sub> | Standby current<br>(both ports TTL Level)<br>CE <sub>L</sub> and CE <sub>R</sub> ≥ V <sub>IH</sub> , f = f <sub>MAX</sub> | 512 K × 72    | Commercial | 1000 | 1250 | 920  | 1160 | mA   |
|                  |                                                                                                                           |               | Industrial | –    | –    | 970  | 1260 | mA   |
|                  |                                                                                                                           | 1024 K × 36   | Commercial | 910  | 1140 | 820  | 1050 | mA   |
|                  |                                                                                                                           |               | Industrial | –    | –    | 880  | 1160 | mA   |
|                  |                                                                                                                           | 2048 K × 18   | Commercial | 890  | 1110 | 810  | 1030 | mA   |
|                  |                                                                                                                           |               | Industrial | –    | –    | 860  | 1140 | mA   |
|                  |                                                                                                                           | 256 K × 72    | Commercial | 500  | 630  | 460  | 580  | mA   |
|                  |                                                                                                                           |               | Industrial | 530  | 680  | 490  | 630  | mA   |
|                  |                                                                                                                           | 512 K × 36    | Commercial | 460  | 570  | 410  | 530  | mA   |
|                  |                                                                                                                           |               | Industrial | 480  | 630  | 440  | 580  | mA   |
|                  |                                                                                                                           | 1024 K × 18   | Commercial | 450  | 560  | 410  | 520  | mA   |
|                  |                                                                                                                           |               | Industrial | 470  | 610  | 430  | 570  | mA   |
|                  |                                                                                                                           | 128 K × 72    | Commercial | 400  | 490  | 360  | 450  | mA   |
|                  |                                                                                                                           |               | Industrial | 420  | 540  | 380  | 490  | mA   |
|                  |                                                                                                                           | 256 K × 36    | Commercial | 380  | 440  | 340  | 400  | mA   |
|                  |                                                                                                                           |               | Industrial | 390  | 470  | 360  | 430  | mA   |
|                  |                                                                                                                           | 512 K × 18    | Commercial | 390  | 460  | 350  | 410  | mA   |
|                  |                                                                                                                           |               | Industrial | 410  | 480  | 370  | 440  | mA   |
|                  |                                                                                                                           | 64 K × 36     | Commercial | –    | –    | –    | –    | mA   |
|                  |                                                                                                                           |               | Industrial | –    | –    | –    | –    | mA   |

## Electrical Characteristics *(continued)*

Over the Operating Range

| Parameter        | Description                                                                                  | Configuration |            | -200 |      | -167 |      | Unit |
|------------------|----------------------------------------------------------------------------------------------|---------------|------------|------|------|------|------|------|
|                  |                                                                                              |               |            | Typ  | Max  | Typ  | Max  |      |
| I <sub>SB2</sub> | Standby current<br>(one port TTL or CMOS level)<br>$CE_L \mid CE_R \geq V_{IH}, f = f_{MAX}$ | 512 K × 72    | Commercial | 1300 | 1570 | 1160 | 1410 | mA   |
|                  |                                                                                              |               | Industrial | –    | –    | 1210 | 1520 | mA   |
|                  |                                                                                              | 1024 K × 36   | Commercial | 1090 | 1330 | 980  | 1210 | mA   |
|                  |                                                                                              |               | Industrial | –    | –    | 1030 | 1330 | mA   |
|                  |                                                                                              | 2048 K × 18   | Commercial | 1040 | 1270 | 930  | 1160 | mA   |
|                  |                                                                                              |               | Industrial | –    | –    | 980  | 1270 | mA   |
|                  |                                                                                              | 256 K × 72    | Commercial | 650  | 790  | 580  | 710  | mA   |
|                  |                                                                                              |               | Industrial | 680  | 840  | 610  | 760  | mA   |
|                  |                                                                                              | 512 K × 36    | Commercial | 550  | 670  | 490  | 610  | mA   |
|                  |                                                                                              |               | Industrial | 570  | 730  | 520  | 670  | mA   |
|                  |                                                                                              | 1024 K × 18   | Commercial | 520  | 640  | 470  | 580  | mA   |
|                  |                                                                                              |               | Industrial | 550  | 690  | 490  | 640  | mA   |
|                  |                                                                                              | 128 K × 72    | Commercial | 520  | 630  | 460  | 560  | mA   |
|                  |                                                                                              |               | Industrial | 550  | 670  | 480  | 610  | mA   |
|                  |                                                                                              | 256 K × 36    | Commercial | 460  | 530  | 400  | 470  | mA   |
|                  |                                                                                              |               | Industrial | 480  | 560  | 430  | 500  | mA   |
|                  |                                                                                              | 512 K × 18    | Commercial | 460  | 530  | 410  | 480  | mA   |
|                  |                                                                                              |               | Industrial | 480  | 560  | 430  | 510  | mA   |
|                  |                                                                                              | 64 K × 36     | Commercial | –    | –    | –    | –    | mA   |
|                  |                                                                                              |               | Industrial | –    | –    | –    | –    | mA   |

## Electrical Characteristics

Over the Operating Range

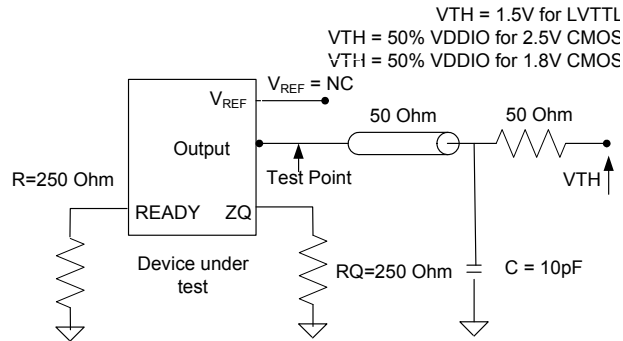
| Parameter | Description                                                                                    | Configuration |            | All Speed Bins |     | Unit |
|-----------|------------------------------------------------------------------------------------------------|---------------|------------|----------------|-----|------|
|           |                                                                                                |               |            | Typ            | Max |      |
| $I_{SB3}$ | Standby current<br>(both ports CMOS level)<br>$CE_L$ and $CE_R \geq V_{CORE} - 0.2$ V, $f = 0$ | 512 K × 72    | Commercial | 410            | 590 | mA   |
|           |                                                                                                |               | Industrial | 460            | 700 | mA   |
|           |                                                                                                | 1024 K × 36   | Commercial | 410            | 590 | mA   |
|           |                                                                                                |               | Industrial | 460            | 700 | mA   |
|           |                                                                                                | 2048 K × 18   | Commercial | 410            | 590 | mA   |
|           |                                                                                                |               | Industrial | 460            | 700 | mA   |
|           |                                                                                                | 256 K × 72    | Commercial | 210            | 300 | mA   |
|           |                                                                                                |               | Industrial | 230            | 350 | mA   |
|           |                                                                                                | 512 K × 36    | Commercial | 210            | 300 | mA   |
|           |                                                                                                |               | Industrial | 230            | 350 | mA   |
|           |                                                                                                | 1024 K × 18   | Commercial | 210            | 300 | mA   |
|           |                                                                                                |               | Industrial | 230            | 350 | mA   |
|           |                                                                                                | 128 K × 72    | Commercial | 150            | 200 | mA   |
|           |                                                                                                |               | Industrial | 170            | 220 | mA   |
|           |                                                                                                | 256 K × 36    | Commercial | 150            | 200 | mA   |
|           |                                                                                                |               | Industrial | 170            | 220 | mA   |
|           |                                                                                                | 512 K × 18    | Commercial | 150            | 200 | mA   |
|           |                                                                                                |               | Industrial | 170            | 220 | mA   |

**Table 12. Capacitance**

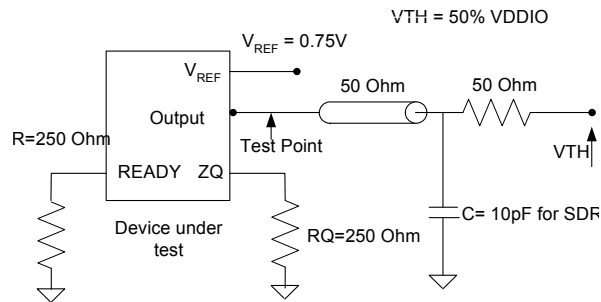
| Signals           | Packages                                                                |                            |                            |             |
|-------------------|-------------------------------------------------------------------------|----------------------------|----------------------------|-------------|
|                   | CYD18S72V18<br>CYD09S72V18<br>CYD18S36V18<br>CYD09S36V18<br>CYD02S36V18 | CYD18S18V18<br>CYD09S18V18 | CYD36S72V18<br>CYD36S36V18 | CYD36S18V18 |
| OE                | 12 pF                                                                   | 12 pF                      | 20 pF                      | 20 pF       |
| BE, DQ            | 10 pF                                                                   | 18 pF                      | 16 pF                      | 30 pF       |
| All other signals | 10 pF                                                                   | 10 pF                      | 16 pF                      | 16 pF       |

## AC Test Load and Waveforms

**Figure 9. Output Test Load for LVTTTL/CMOS**

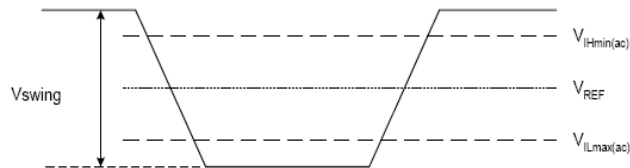


**Figure 10. Output Test Load for HSTL**



**Figure 11. HSTL Input Waveform**

### AC Input Test Signal Waveform



$$V_{swing} = 1.0V$$

$$V_{REF} = 0.75V$$

$$V_{IH} = 1.25V$$

$$V_{IL} = 0.25V$$

$$\text{Slew} = 2.0V/ns$$

All input parameters are referenced to  $V_{REF}$

## Switching Characteristics

Over the Operating Range

**Table 13. SDR Mode, Signals Affected by DLL**

| Parameter                              | Description                                  | DLL ON (LOWSPD=1) <sup>[46]</sup> |                          |      |                          | DLL OFF (LOWSPD=0) <sup>[46]</sup> |                          | Unit |
|----------------------------------------|----------------------------------------------|-----------------------------------|--------------------------|------|--------------------------|------------------------------------|--------------------------|------|
|                                        |                                              | -200                              |                          | -167 |                          |                                    |                          |      |
|                                        |                                              | Min                               | Max                      | Min  | Max                      | Min                                | Max                      |      |
| t <sub>CD2</sub> <sup>[49]</sup>       | C rise to DQ valid for pipelined mode        | –                                 | 3.30 <sup>[45, 48]</sup> | –    | 4.00 <sup>[45, 48]</sup> | –                                  | 6.00 <sup>[45, 48]</sup> | ns   |
| t <sub>CCQ</sub> <sup>[49]</sup>       | C rise to CQ rise                            | 1.00                              | 3.30 <sup>[48]</sup>     | 1.00 | 4.00 <sup>[48]</sup>     | 1.00                               | 6.00 <sup>[48]</sup>     | ns   |
| t <sub>CKHZ2</sub> <sup>[44, 49]</sup> | C rise to DQ output high Z in pipelined mode | 1.00                              | 3.30 <sup>[45, 48]</sup> | 1.00 | 4.00 <sup>[45, 48]</sup> | 1.00                               | 6.00 <sup>[45, 48]</sup> | ns   |
| t <sub>CKLZ2</sub> <sup>[44, 49]</sup> | C rise to DQ output low Z in pipelined mode  | 1.00                              | –                        | 1.00 | –                        | 1.00                               | –                        | ns   |

**Table 14. SDR Mode**

| Parameter                        | Description                                       |                    | -200                         |                          | -167                         |                          | Unit |
|----------------------------------|---------------------------------------------------|--------------------|------------------------------|--------------------------|------------------------------|--------------------------|------|
|                                  |                                                   |                    | Min                          | Max                      | Min                          | Max                      |      |
| f <sub>MAX</sub> (PIPELINED)     | Maximum operating frequency for pipelined mode    |                    | 100                          | 200                      | 100                          | 167                      | MHz  |
| f <sub>MAX</sub> (FLOW THROUGH)  | Maximum operating frequency for flow through mode |                    | –                            | 77                       | –                            | 66.7                     | MHz  |
| t <sub>CYC</sub> (PIPELINED)     | C clock cycle time for pipelined mode             |                    | 5.00 <sup>[48]</sup>         | 10.00                    | 6.00 <sup>[48]</sup>         | 10.00                    | ns   |
| t <sub>CYC</sub> (FLOW THROUGH)  | C clock cycle time for flow through mode          |                    | 13.00 <sup>[48]</sup>        | –                        | 15.00 <sup>[48]</sup>        | –                        | ns   |
| t <sub>CKD</sub>                 | C clock duty time                                 |                    | 45                           | 55                       | 45                           | 55                       | %    |
| t <sub>SD</sub>                  | Data input setup time to C rise                   | HSTL 1.8 V LVCMOS  | 1.50 <sup>[45, 48]</sup>     | –                        | 1.70 <sup>[45, 48]</sup>     | –                        | ns   |
|                                  |                                                   | 2.5 V LVCMOS       | 1.75 <sup>[45, 48]</sup>     | –                        | 1.95 <sup>[45, 48]</sup>     |                          | ns   |
|                                  |                                                   | 3.3 V LVTTTL       |                              |                          |                              |                          |      |
| t <sub>HD</sub> <sup>[47]</sup>  | Data input hold time after C rise                 |                    | 0.5                          | –                        | 0.5                          | –                        | ns   |
| t <sub>SAC</sub>                 | Address and control input setup time to C rise    | HSTL 1.8 V L VCMOS | 1.50 <sup>[45, 47, 48]</sup> | –                        | 1.70 <sup>[45, 47, 48]</sup> | –                        | ns   |
|                                  |                                                   | 2.5 V LVCMOS       | 1.75 <sup>[45, 47, 48]</sup> | –                        | 1.95 <sup>[45, 47, 48]</sup> | –                        | ns   |
|                                  |                                                   | 3.3 V LVTTTL       |                              |                          |                              |                          |      |
| t <sub>HAC</sub> <sup>[47]</sup> | Address and control input hold time after C rise  |                    | 0.50                         | –                        | 0.60                         | –                        | ns   |
| t <sub>OE</sub>                  | Output enable to data valid                       |                    | –                            | 4.40 <sup>[45, 48]</sup> | –                            | 5.00 <sup>[45, 48]</sup> | ns   |
| t <sub>OLZ</sub> <sup>[44]</sup> | OE to low Z                                       |                    | 1.00                         | –                        | 1.00                         | –                        | ns   |

### Notes

44. Parameters specified with the load capacitance in [Figure 9 on page 25](#) and [Figure 10 on page 25](#).

45. For the x18 devices, add 200 ps to this parameter in [Table 14](#).

46. Test conditions assume a signal transition time of 2 V/ns.

47. Add 300 ps to this timing for 36M devices.

48. Add 15% to this parameter if a V<sub>CORE</sub> of 1.5 V is used.

49. This parameter assumes input clock cycle to cycle jitter of ± 0ps.

**Table 14. SDR Mode** *(continued)*

| Parameter           | Description                                            | -200              |                          | -167  |                           | Unit |
|---------------------|--------------------------------------------------------|-------------------|--------------------------|-------|---------------------------|------|
|                     |                                                        | Min               | Max                      | Min   | Max                       |      |
| $t_{OHZ}^{[50]}$    | OE to high Z                                           | 1.00              | 4.40 <sup>[51, 52]</sup> | 1.00  | 5.00 <sup>[51, 52]</sup>  | ns   |
| $t_{CD1}$           | C rise to DQ valid for flow through mode (LowSPD = 0)  | –                 | 9.00 <sup>[51, 52]</sup> | –     | 11.00 <sup>[51, 52]</sup> | ns   |
| $t_{CA1}$           | C rise to address readback valid for flow through mode | –                 | 9.00 <sup>[52]</sup>     | –     | 11.00 <sup>[52]</sup>     | ns   |
| $t_{CA2}$           | C rise to address readback valid for pipelined mode    | –                 | 5.00 <sup>[52]</sup>     | –     | 6.00 <sup>[52]</sup>      | ns   |
| $t_{DC}^{[53]}$     | DQ output hold after C rise                            | 1.00              | –                        | 1.00  | –                         | ns   |
| $t_{JIT}$           | Clock input cycle to cycle jitter                      | –                 | +/- 200                  | –     | +/- 200                   | ps   |
| $t_{CQHCV}^{[53]}$  | Echo clock (CQ) high to output valid                   | HSTL 1.8 V LVCMOS |                          | –     | 0.70 <sup>[51]</sup>      | ns   |
|                     |                                                        | 2.5 V LVCMOS      |                          | –     | 0.80 <sup>[51]</sup>      | ns   |
|                     |                                                        | 3.3 V LVTTTL      |                          | –     | 0.90 <sup>[51]</sup>      | ns   |
| $t_{CQHCV}^{[53]}$  | Echo clock (CQ) high to output hold                    | HSTL 1.8 V LVCMOS |                          | –0.70 | –                         | ns   |
|                     |                                                        | 2.5 V LVCMOS      |                          | –0.85 | –                         | ns   |
|                     |                                                        | 3.3 V LVTTTL      |                          | –0.95 | –                         | ns   |
| $t_{CKHZ1}^{[50]}$  | C rise to DQ output high Z in flow through mode        | 1.00              | 9.00 <sup>[51, 52]</sup> | 1.00  | 11.00 <sup>[51, 52]</sup> | ns   |
| $t_{CKLZ1}^{[50]}$  | C rise to DQ output low Z in flow through mode         | 1.00              | –                        | 1.00  | –                         | ns   |
| $t_{AC}$            | Address output hold after C rise                       | 1.00              | –                        | 1.00  | –                         | ns   |
| $t_{CKHZA1}^{[50]}$ | C rise to address output high Z for flow through mode  | 1.00              | 9.00 <sup>[52]</sup>     | 1.00  | 11.00 <sup>[52]</sup>     | ns   |
| $t_{CKHZA2}^{[50]}$ | C rise to address output high Z for pipelined mode     | 1.00              | 5.00 <sup>[52]</sup>     | 1.00  | 6.00 <sup>[52]</sup>      | ns   |
| $t_{CKLZA}^{[50]}$  | C rise to address output low Z                         | 1.00              | –                        | 1.00  | –                         | ns   |
| $t_{SCINT}$         | C rise to $\overline{CNTINT}$ low                      | 1.00              | 3.30 <sup>[52]</sup>     | 1.00  | 4.00 <sup>[52]</sup>      | ns   |
| $t_{RCINT}$         | C rise to $\overline{CNTINT}$ high                     | 1.00              | 3.30 <sup>[52]</sup>     | 1.00  | 4.00 <sup>[52]</sup>      | ns   |
| $t_{SINT}$          | C rise to $\overline{INT}$ low                         | 0.50              | 7.00 <sup>[52]</sup>     | 0.50  | 8.00 <sup>[52]</sup>      | ns   |
| $t_{RINT}$          | C rise to $\overline{INT}$ high                        | 0.50              | 7.00 <sup>[52]</sup>     | 0.50  | 8.00 <sup>[52]</sup>      | ns   |
| $t_{BSY}$           | C rise to $\overline{BUSY}$ valid                      | 1.00              | 3.30 <sup>[52]</sup>     | 1.00  | 4.00 <sup>[52]</sup>      | ns   |

**Notes**

50. Parameters specified with the load capacitance in Figure 9 on page 25 and Figure 10 on page 25.

51. For the x18 devices, add 200 ps to this parameter in Table 14.

52. Add 15% to this parameter if a V<sub>CORE</sub> of 1.5 V is used.

53. This parameter assumes input clock cycle to cycle jitter of ± 0ps.

**Table 15. Master Reset Timing**

| Parameter          | Description                           | -200 |                     | -167 |                    | Unit   |
|--------------------|---------------------------------------|------|---------------------|------|--------------------|--------|
|                    |                                       | Min  | Max                 | Min  | Max                |        |
| $t_{PUP}$          | Power-up time                         | 1    | –                   | 1    | –                  | ms     |
| $t_{RS}$           | Master reset pulse width              | 5    | –                   | 5    | –                  | cycles |
| $t_{RSR}$          | Master reset recovery time            | 5    | –                   | 5    | –                  | cycles |
| $t_{RSF}$          | Master reset to outputs inactive/Hi Z | –    | 15                  | –    | 18                 | ns     |
| $t_{RDY}^{[54]}$   | Master reset release to port ready    | –    | 1024                | –    | 1024               | cycles |
| $t_{CORDY}^{[55]}$ | C rise to port ready                  | –    | 9.5 <sup>[56]</sup> | –    | 11 <sup>[56]</sup> | ns     |

**Table 16. JTAG Timing**

| Parameter  | Description                   | -200 |     | -167 |     | Unit |
|------------|-------------------------------|------|-----|------|-----|------|
|            |                               | Min  | Max | Min  | Max |      |
| $f_{JTAG}$ | JTAG TAP controller frequency | –    | 20  | –    | 20  | MHz  |
| $t_{TCYC}$ | TCK cycle time                | 50   | –   | 50   | –   | ns   |
| $t_{TH}$   | TCK high time                 | 20   | –   | 20   | –   | ns   |
| $t_{TL}$   | TCK low time                  | 20   | –   | 20   | –   | ns   |
| $t_{TMSS}$ | TMS setup to TCK rise         | 10   | –   | 10   | –   | ns   |
| $t_{TMSH}$ | TMS hold to TCK rise          | 10   | –   | 10   | –   | ns   |
| $t_{TDIS}$ | TDI setup to TCK rise         | 10   | –   | 10   | –   | ns   |
| $t_{TDIH}$ | TDI hold to TCK rise          | 10   | –   | 10   | –   | ns   |
| $t_{TDOV}$ | TCK low to TDO valid          | –    | 10  | –    | 10  | ns   |
| $t_{TDOX}$ | TCK low to TDO invalid        | 0    | –   | 0    | –   | ns   |
| $t_{JXZ}$  | TCK low to TDO high Z         | –    | 15  | –    | 15  | ns   |
| $t_{JZX}$  | TCK low to TDO active         | –    | 15  | –    | 15  | ns   |
| $t_{JZX}$  | TCK low to TDO active         | –    | 15  | –    | 15  | ns   |

**Notes**

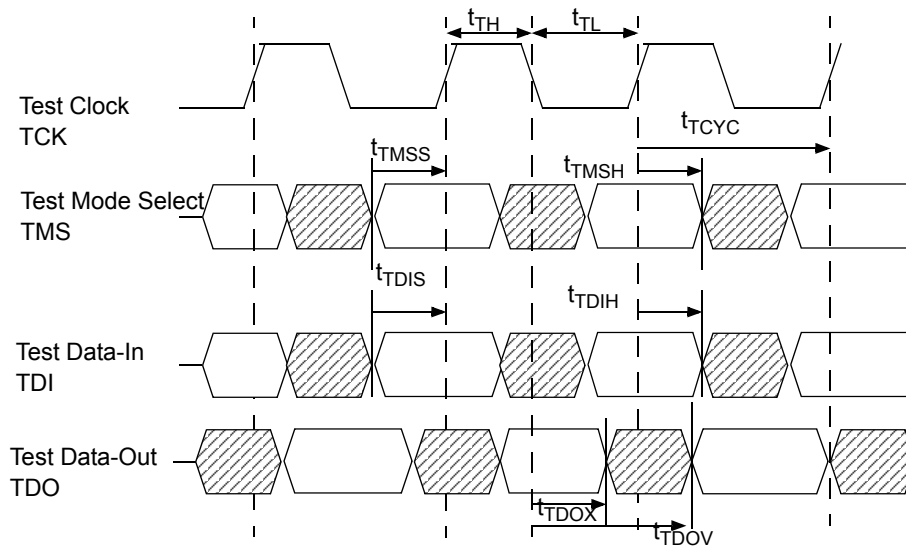
54. READY is a wired OR capable output with a weak pull-down. For a decreased falling delay, connect a 250-Ω resistor to VSS.

55. Add this propagation delay after  $t_{RDY}$  for all Master Reset Operations.

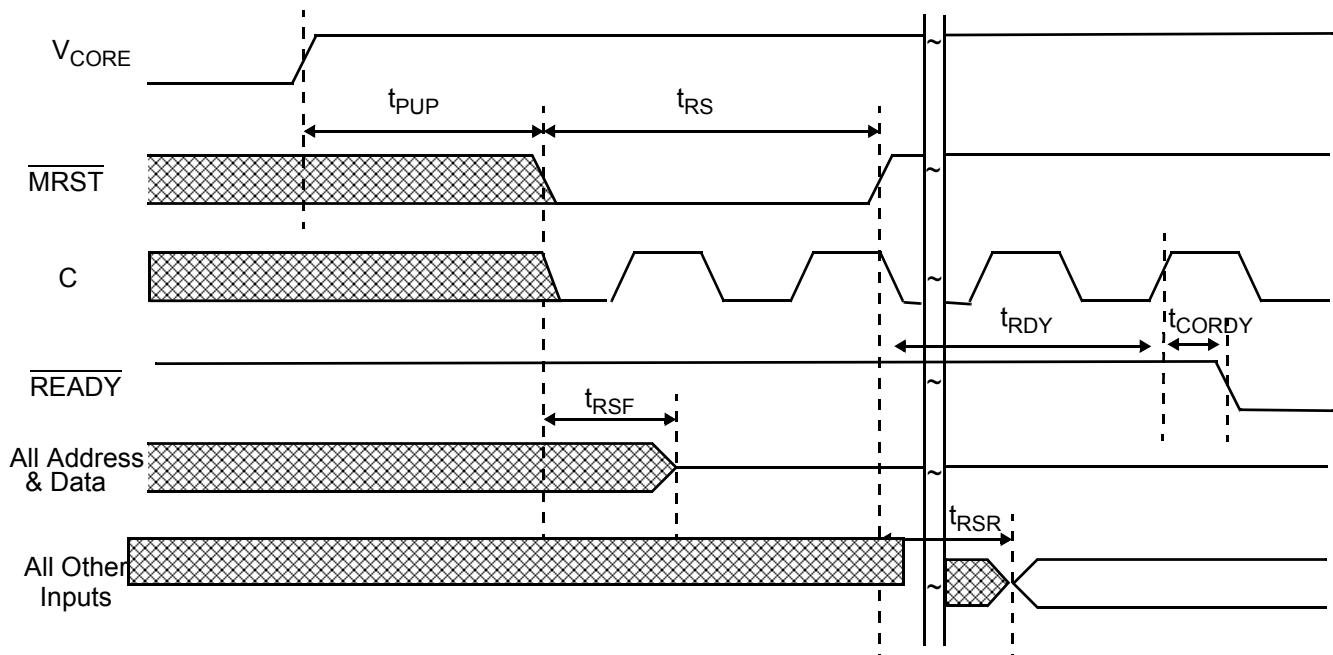
56. Add 15% to this parameter if a VCORE of 1.5 V is used.

## Switching Waveforms

**Figure 12. JTAG Timing**



**Figure 13. Master Reset <sup>[57]</sup>**



**Note**

57.  $\overline{READY}$  is a wired OR capable output with a weak pull-down. For a decreased falling delay, connect a 250- $\Omega$  resistor to VSS.

## Switching Waveforms (continued)

Figure 14. READ Cycle for Pipelined Mode

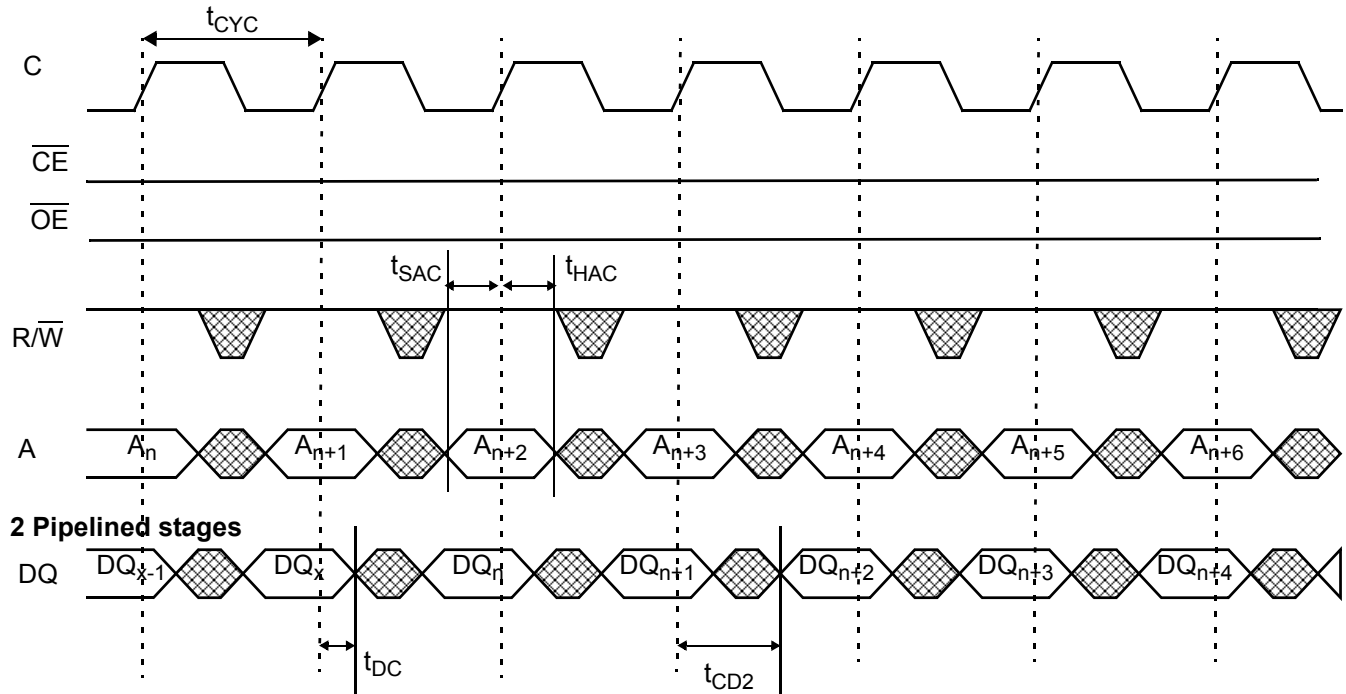
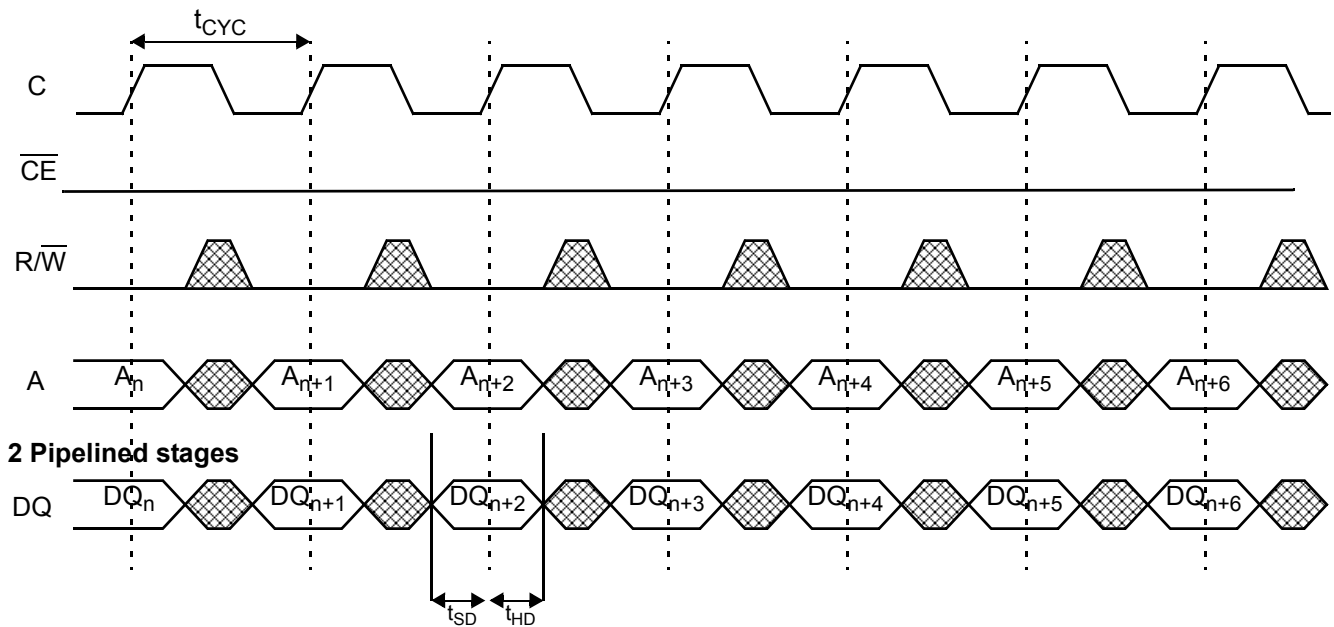
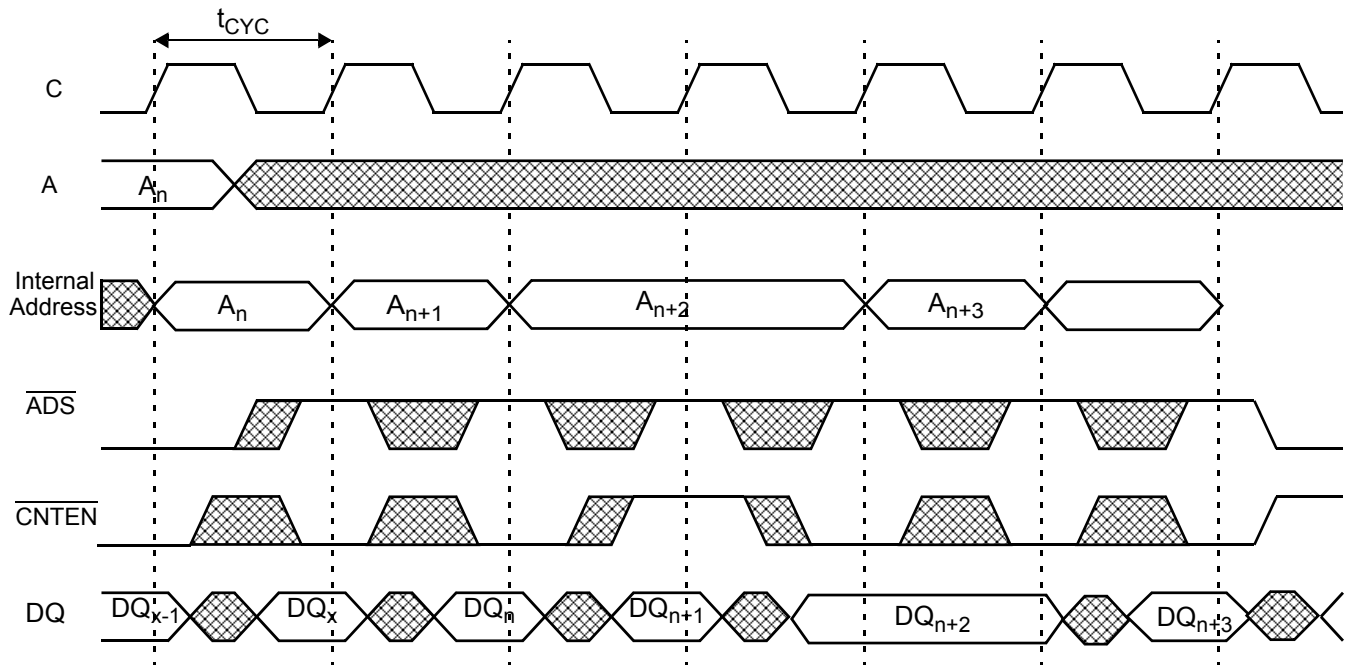


Figure 15. WRITE Cycle for Pipelined and Flow through Modes

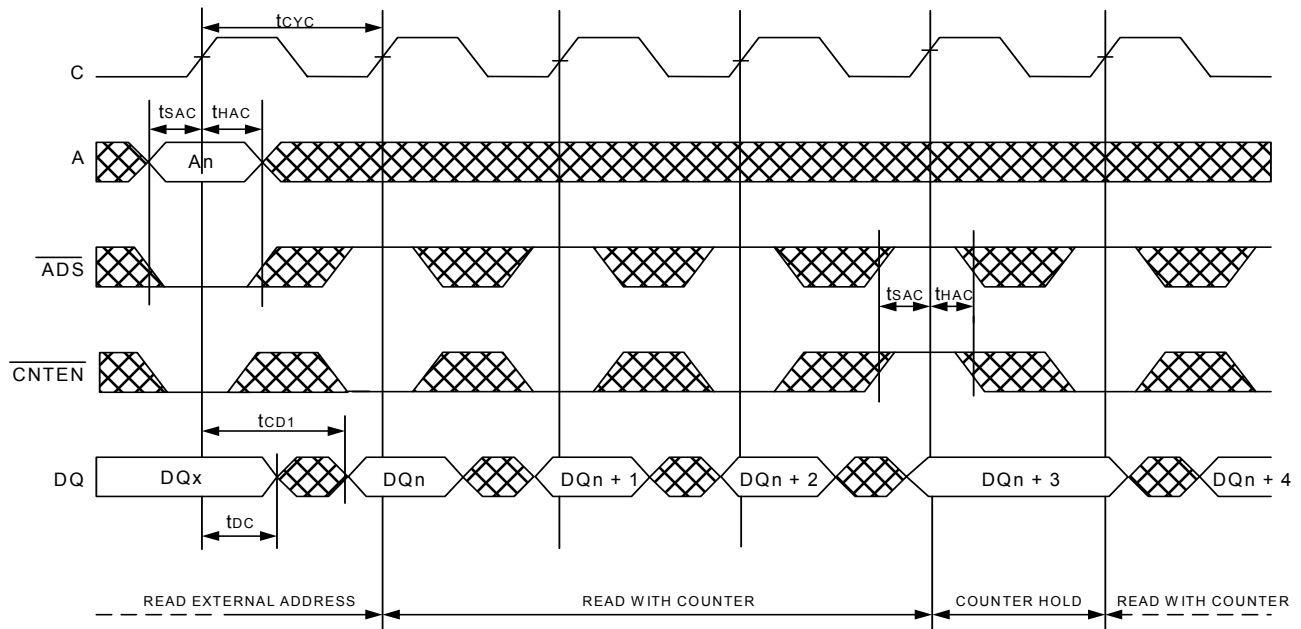


## Switching Waveforms (continued)

**Figure 16. READ with Address Counter Advance for Pipelined Mode**



**Figure 17. READ with Address Counter Advance for Flow through Mode**



## Switching Waveforms (continued)

Figure 18. Port-to-Port WRITE-READ for Pipelined Mode

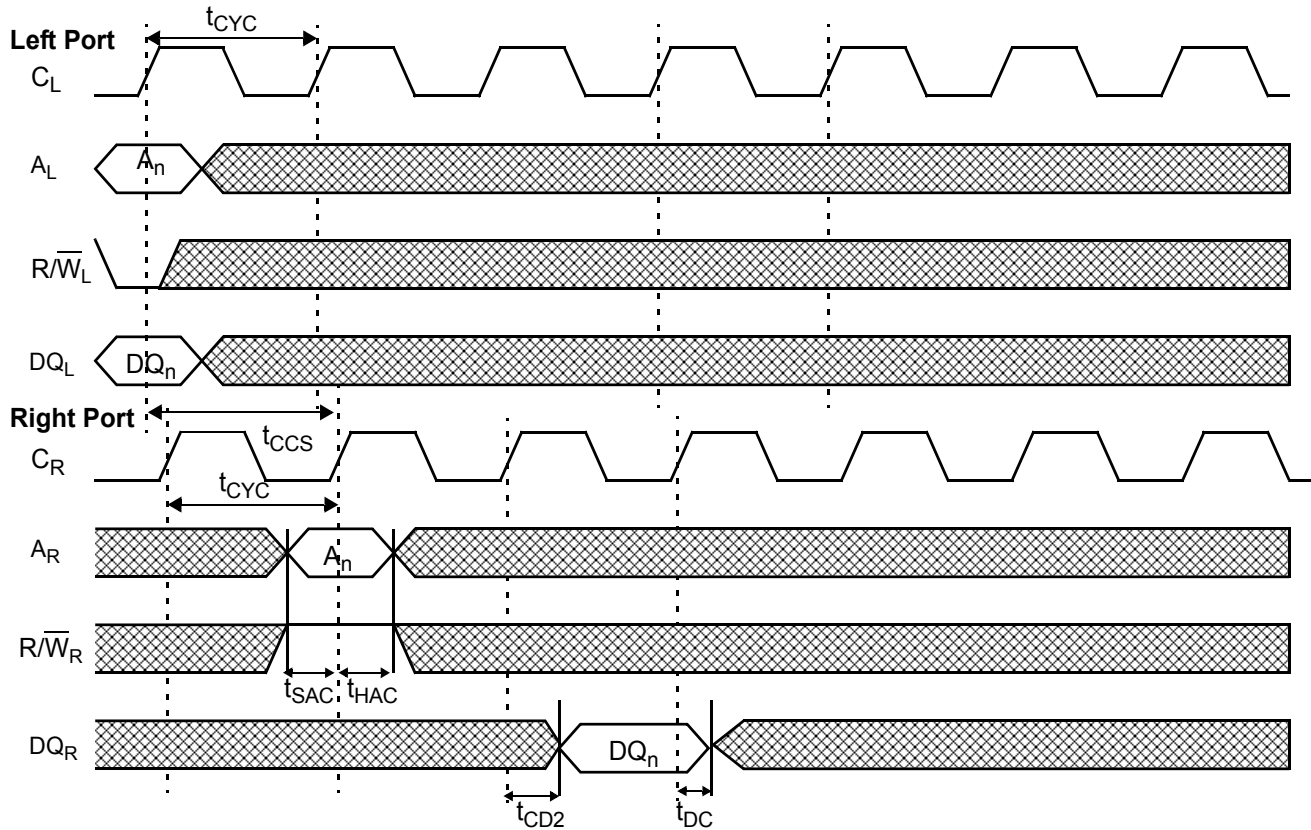
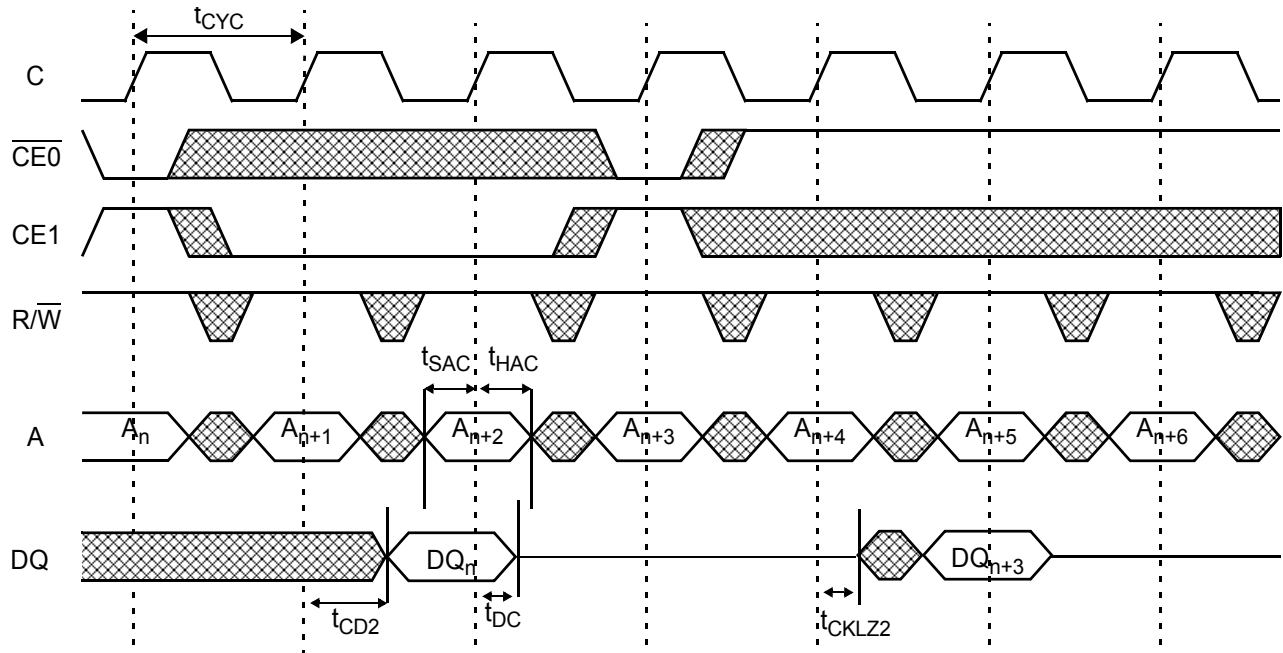


Figure 19. Chip Enable READ for Pipelined Mode



## Switching Waveforms (continued)

Figure 20. OE Controlled WRITE for Pipelined Mode

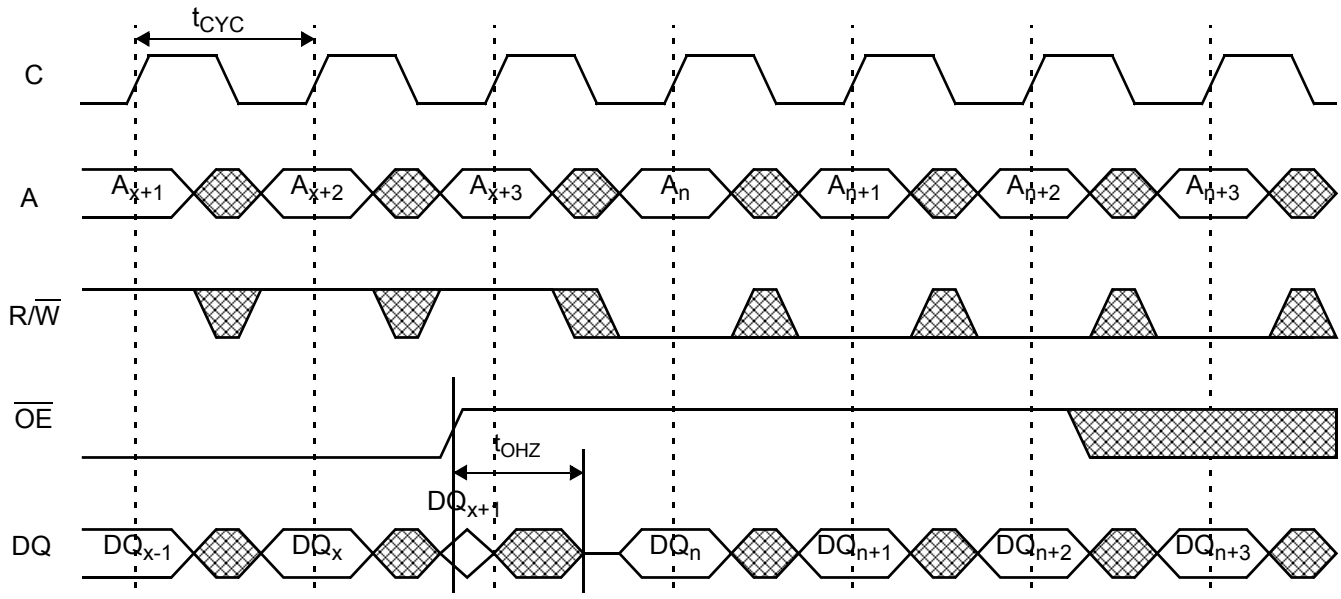
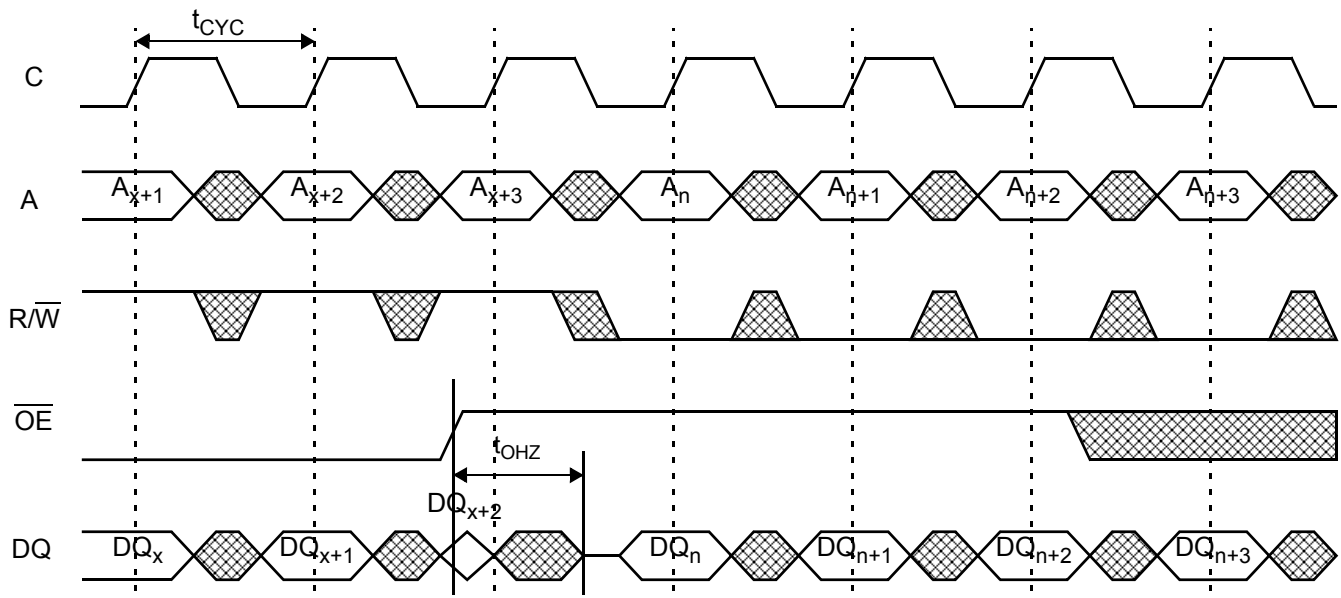
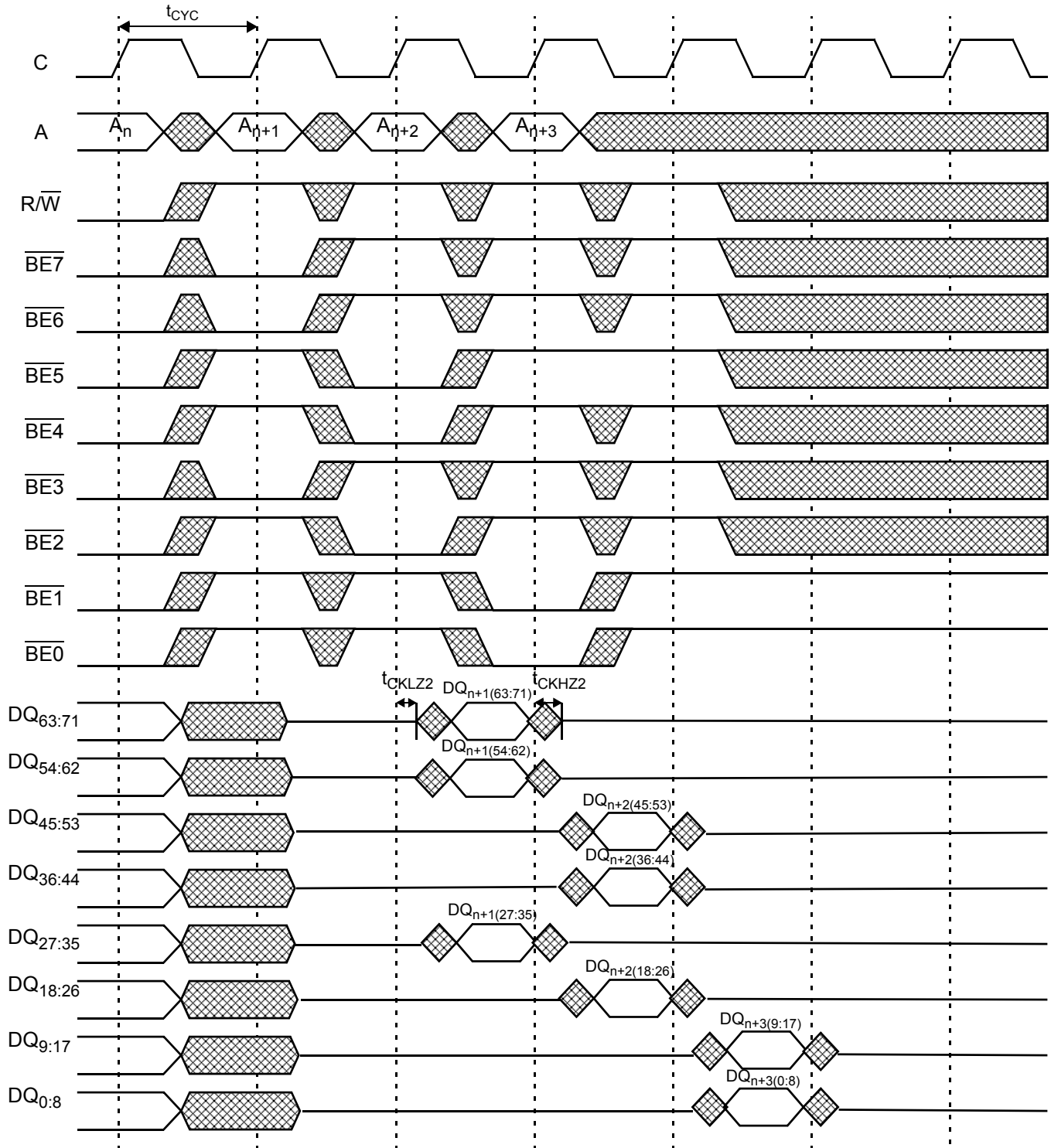


Figure 21. OE Controlled WRITE for Flow through Mode



## Switching Waveforms (continued)

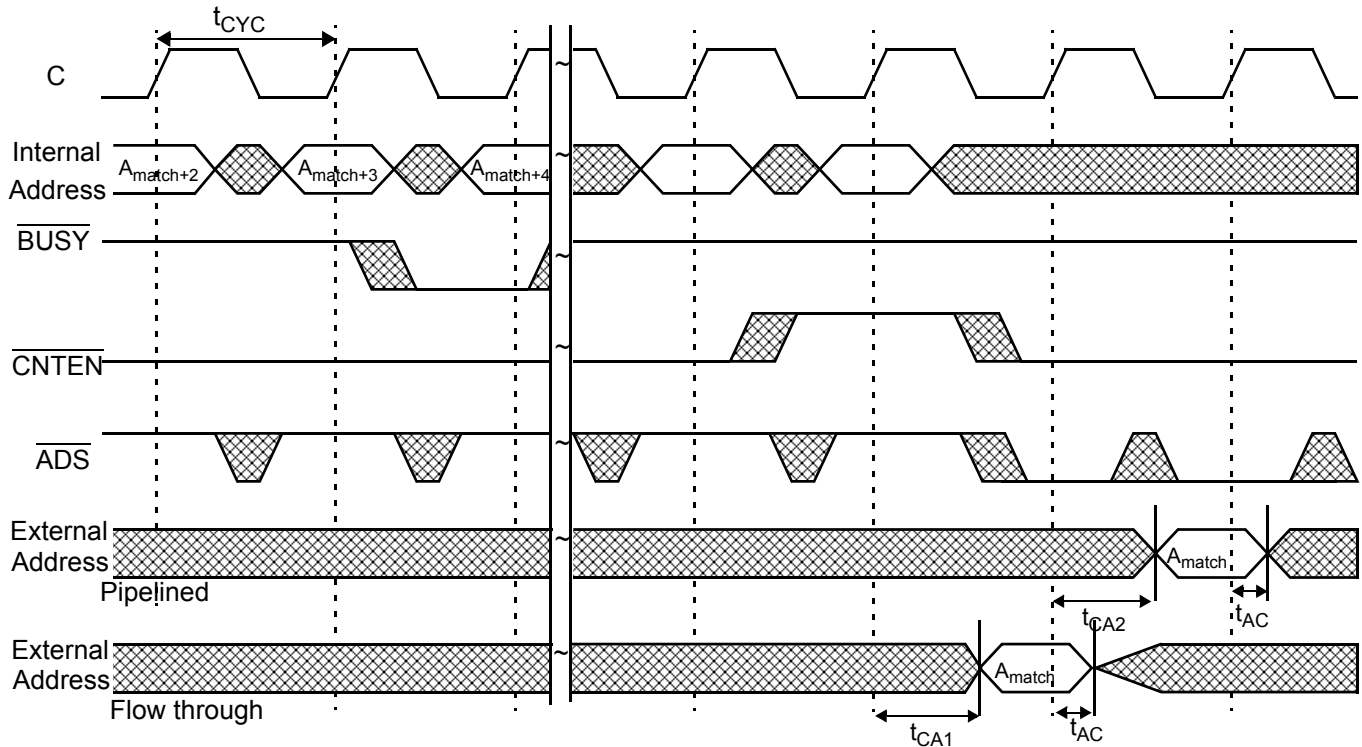
**Figure 22. Byte-Enable READ for Pipelined Mode**



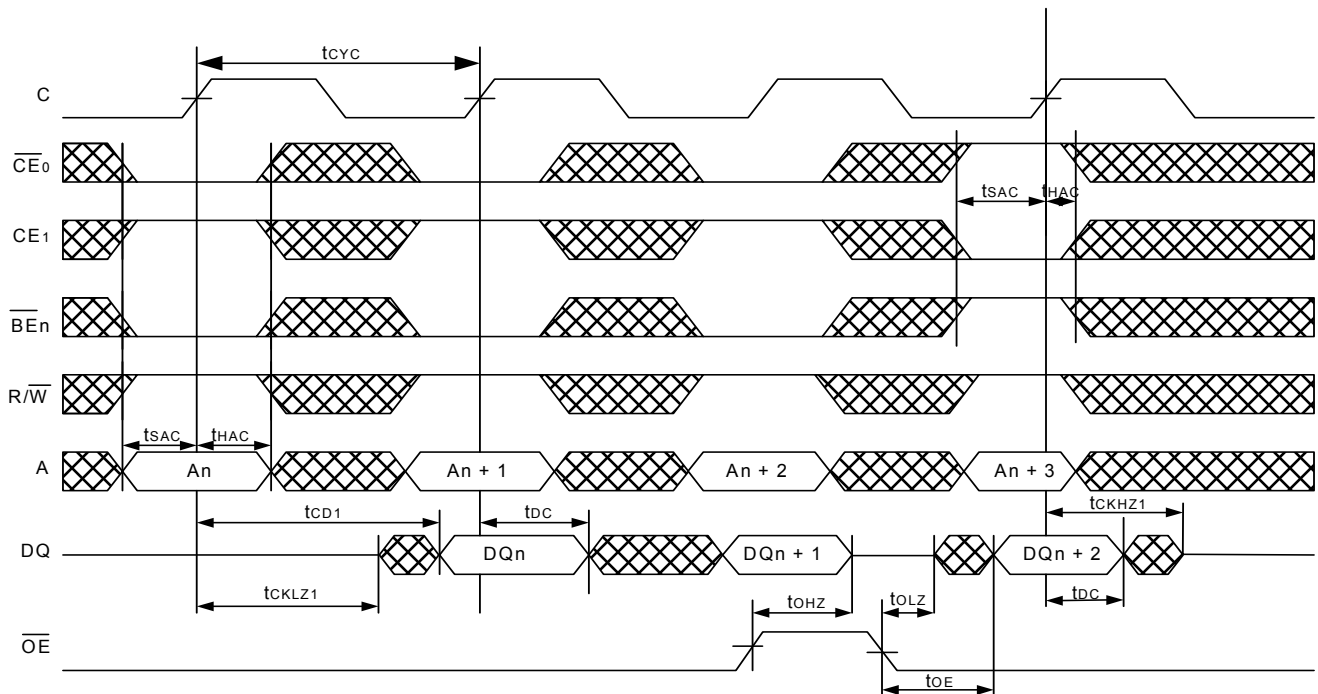


## Switching Waveforms (continued)

**Figure 24. Busy Address Readback for Pipelined and Flow through Modes,  $\overline{\text{CNT}}/\overline{\text{MSK}} = \overline{\text{RET}} = \text{LOW}$ <sup>[58]</sup>**



**Figure 25. Read Cycle for Flow through Mode**

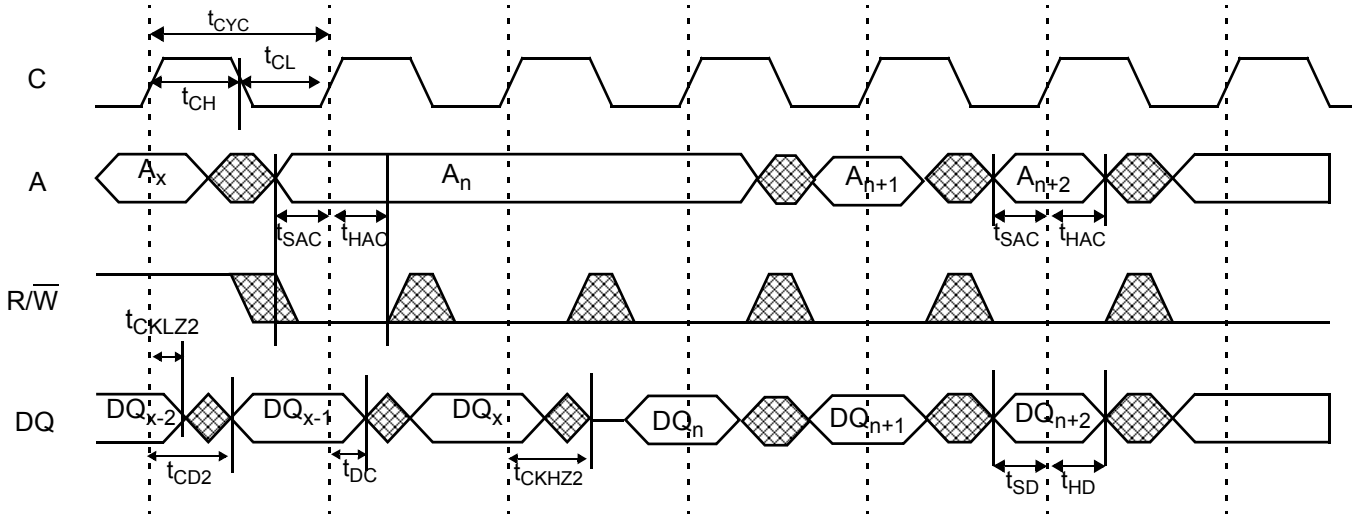


**Note**

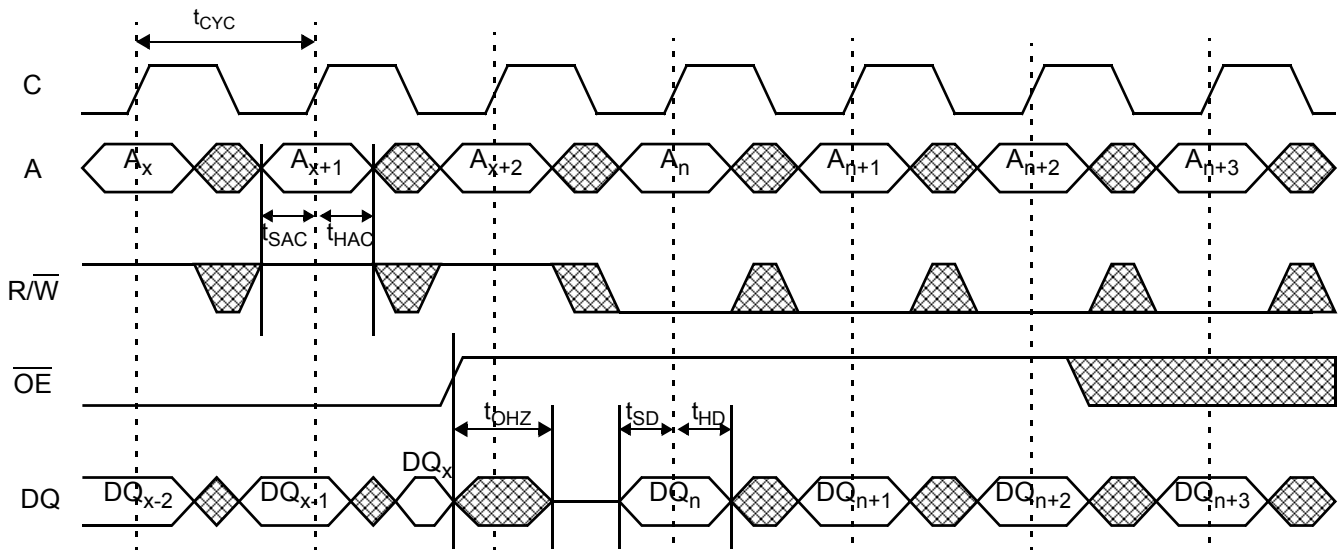
58.  $A_{\text{match}}$  is the matching address that is reported on the address bus of the losing port. The counter operation selected for reporting the address is "Busy Address Readback."

## Switching Waveforms (continued)

**Figure 26. READ-to-WRITE for Pipelined Mode ( $\overline{OE} = V_{IL}$ )**<sup>[59, 60, 61]</sup>



**Figure 27. READ-to-WRITE for Pipelined Mode ( $\overline{OE}$  Controlled)**<sup>[62, 63]</sup>

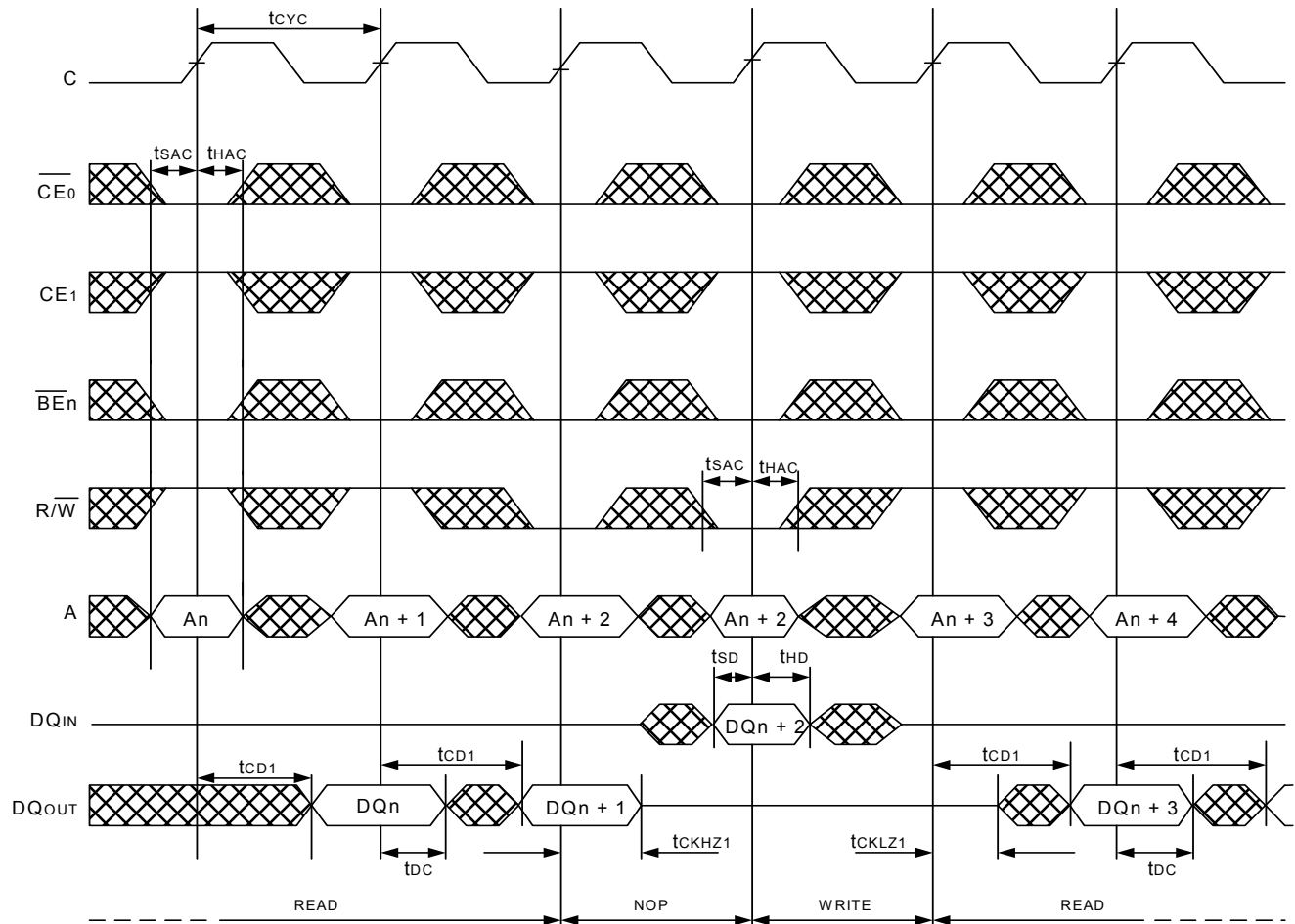


### Notes

- 59. When  $\overline{OE} = V_{IL}$ , the last read operation is enabled to complete before the DQ bus is tri-stated and the user is enabled to drive write data.
- 60. Two dummy writes are issued to accomplish bus turnaround. The third instruction is the first valid write.
- 61. Chip enable or all byte enables are held inactive during the two dummy writes to avoid data corruption.
- 62.  $\overline{OE}$  is deasserted and  $t_{OHZ}$  enabled to elapse before the first write operation is issued.
- 63. Any write scheduled to complete after  $\overline{OE}$  is deasserted is pre-empted.

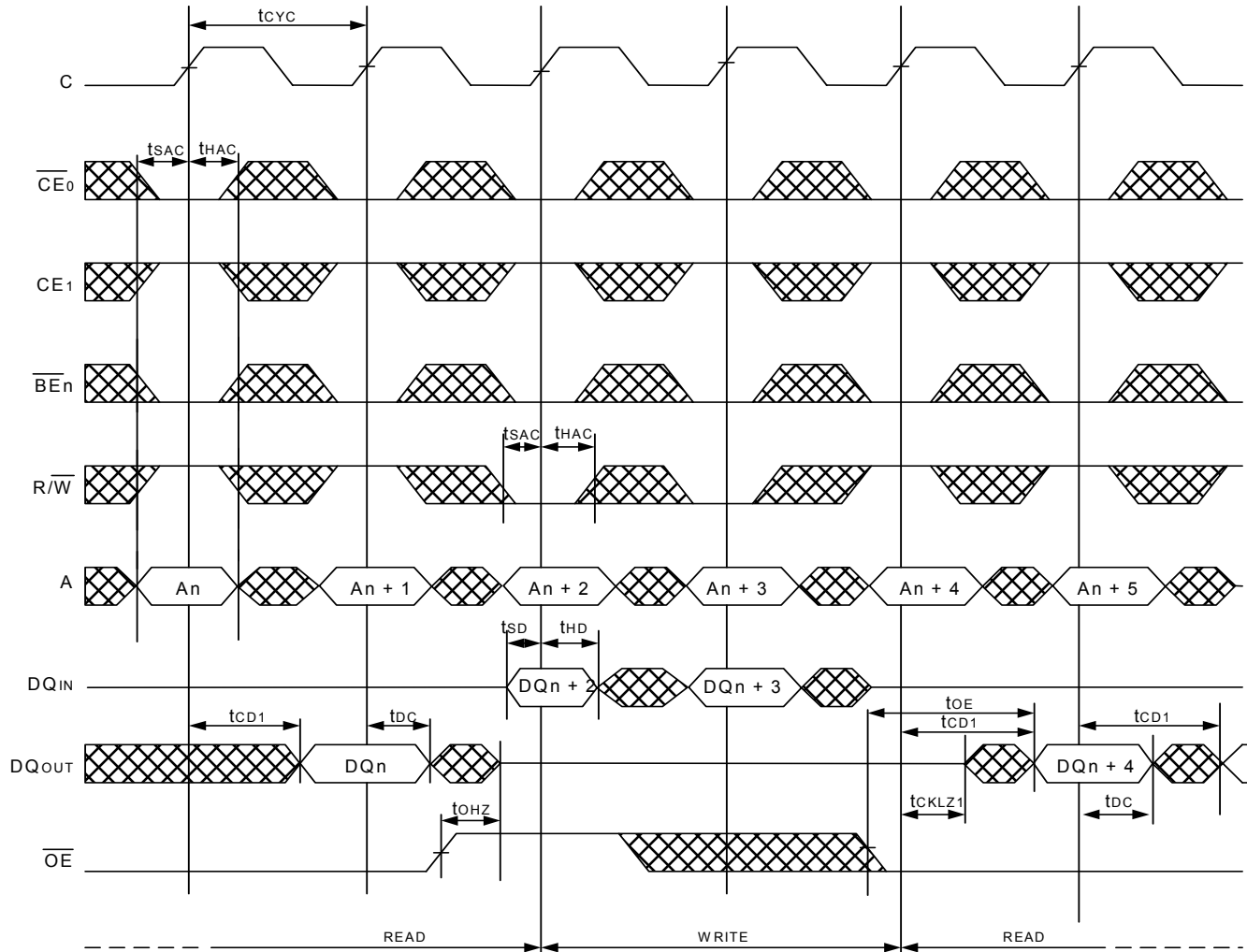
## Switching Waveforms (continued)

Figure 28. Read-to-Write-to-Read for Flow through Mode ( $\overline{OE} = \text{LOW}$ )



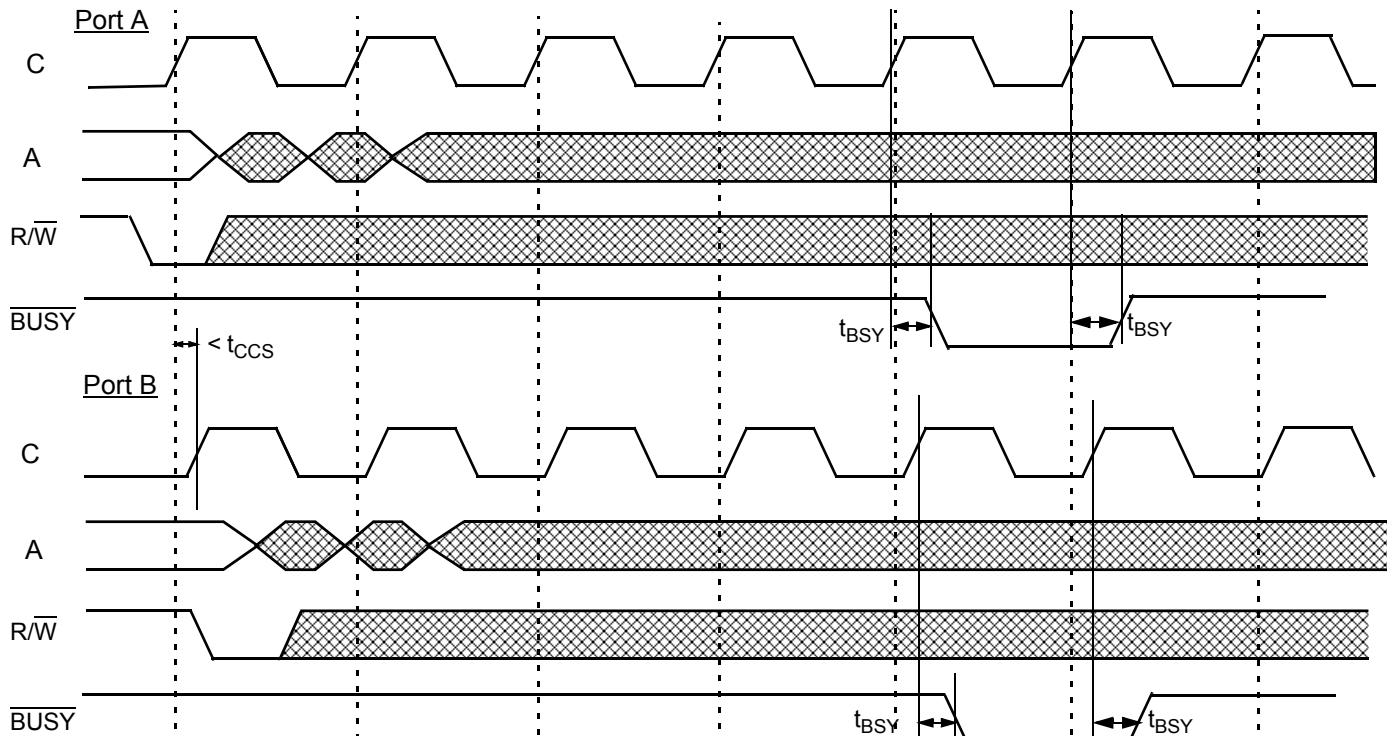
## Switching Waveforms (continued)

Figure 29. Read-to-Write-to-Read for Flow through Mode ( $\overline{\text{OE}}$  Controlled)

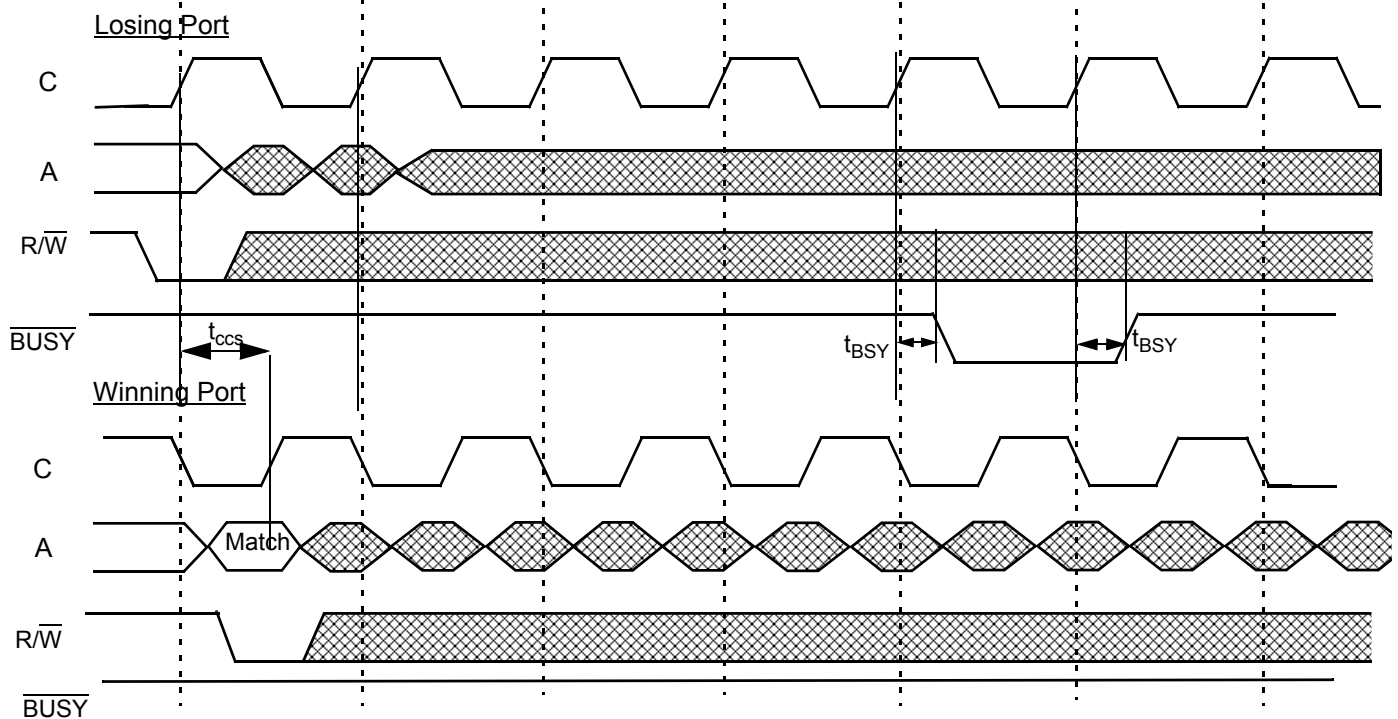


## Switching Waveforms (continued)

**Figure 30.  $\overline{\text{BUSY}}$  Timing, WRITE-WRITE Collision for Pipelined and Flow through Modes, Clock Timing Violates  $t_{\text{CCS}}$ . (Flag Both Ports)**

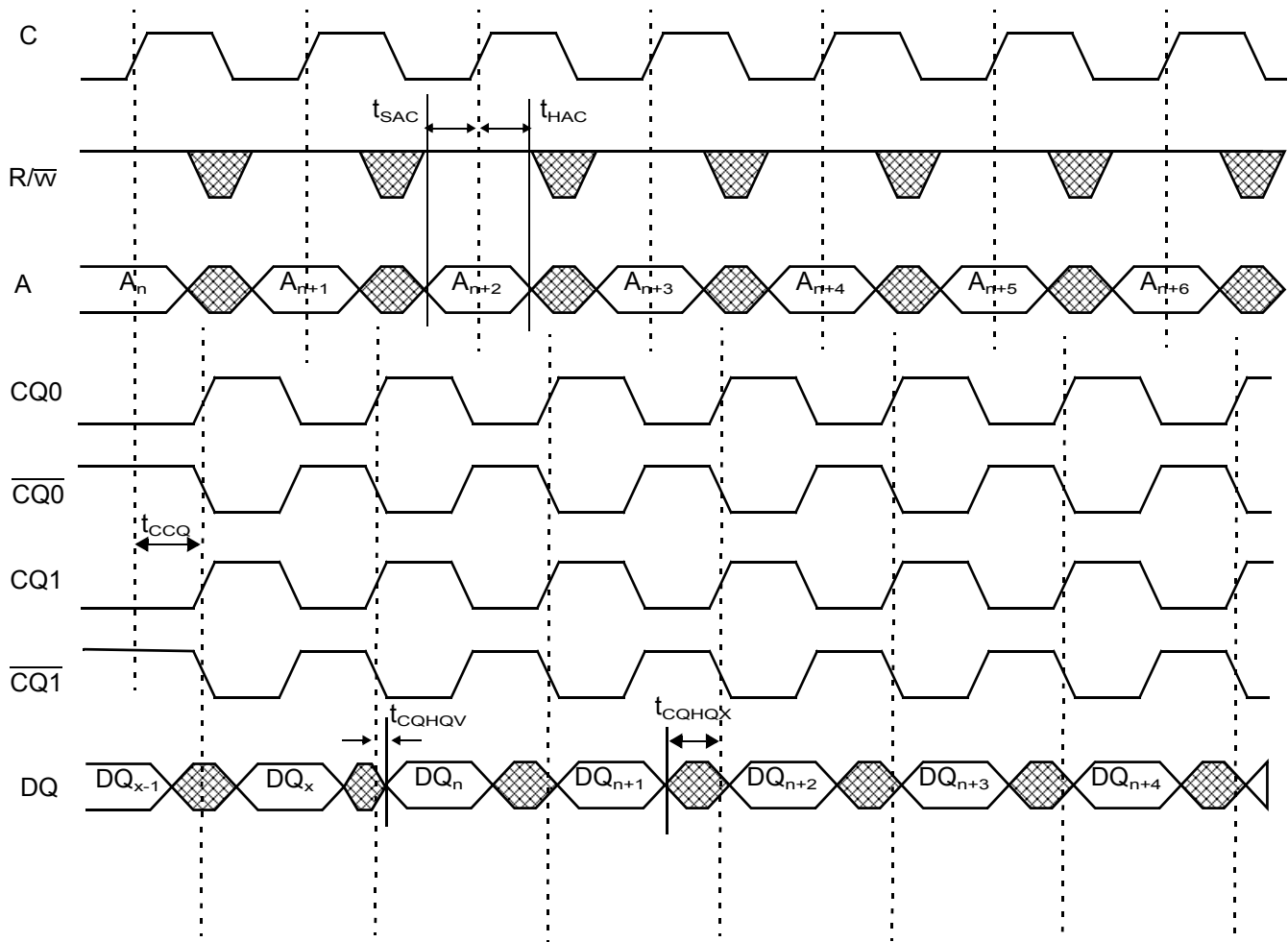


**Figure 31.  $\overline{\text{BUSY}}$  Timing, WRITE-WRITE Collision for Pipelined and Flow through Modes, Clock Timing Meets  $t_{\text{CCS}}$ . (Flag Losing Port)**



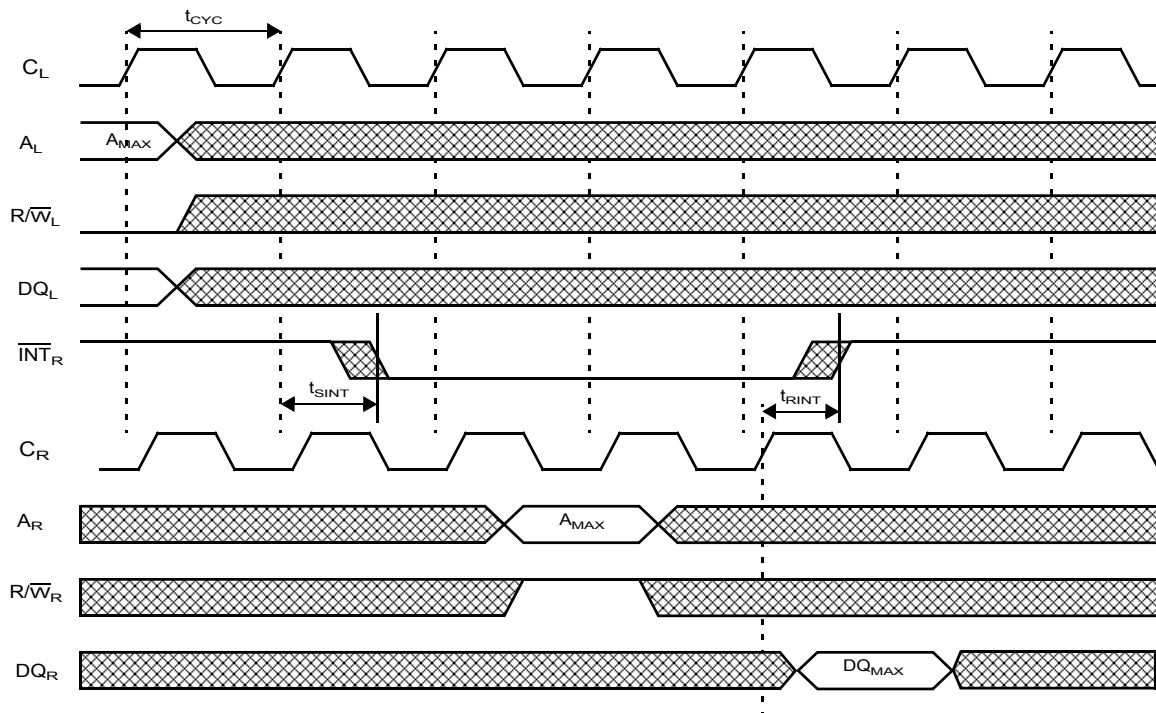
## Switching Waveforms *(continued)*

**Figure 32. Read with Echo Clock for Pipelined Mode (CQEN = HIGH)**



## Switching Waveforms *(continued)*

**Figure 33. Mailbox Interrupt Output**



## Ordering Information

### 512 K × 72 (36-Mbit) 1.8 V/1.5 V Synchronous CYD36S72V18 Dual Port SRAM

| Speed (MHz) | Ordering Code       | Package Diagram | Package Type                                                       | Operating Range |
|-------------|---------------------|-----------------|--------------------------------------------------------------------|-----------------|
| 200         | CYD36S72V18-200BGXC | 001-07825       | 484-ball Ball Grid Array 27 mm × 27 mm with 1.0 mm pitch (Pb-free) | Commercial      |
| 167         | CYD36S72V18-167BGXI | 001-07825       | 484-ball Ball Grid Array 27 mm × 27 mm with 1.0 mm pitch (Pb-free) | Industrial      |

### 256 K × 72 (18-Mbit) 1.8 V/1.5 V Synchronous CYD18S72V18 Dual Port SRAM

| Speed (MHz) | Ordering Code       | Package Diagram | Package Type                                                       | Operating Range |
|-------------|---------------------|-----------------|--------------------------------------------------------------------|-----------------|
| 200         | CYD18S72V18-200BGXI | 51-85218        | 484-ball Ball Grid Array 23 mm × 23 mm with 1.0 mm pitch (Pb-free) | Industrial      |
| 200         | CYD18S72V18-200BGI  | 51-85218        | 484-ball Ball Grid Array 23 mm × 23 mm with 1.0 mm pitch           | Industrial      |
| 167         | CYD18S72V18-167BGXC | 51-85218        | 484-ball Ball Grid Array 23 mm × 23 mm with 1.0 mm pitch (Pb-free) | Commercial      |
| 167         | CYD18S72V18-167BGC  | 51-85218        | 484-ball Ball Grid Array 23 mm × 23 mm with 1.0 mm pitch           | Commercial      |
| 167         | CYD18S72V18-167BGI  | 51-85218        | 484-ball Ball Grid Array 23 mm × 23 mm with 1.0 mm pitch           | Industrial      |

### 128 K × 72 (9-Mbit) 1.8 V/1.5 V Synchronous CYD09S72V18 Dual Port SRAM

| Speed (MHz) | Ordering Code       | Package Diagram | Package Type                                                       | Operating Range |
|-------------|---------------------|-----------------|--------------------------------------------------------------------|-----------------|
| 200         | CYD09S72V18-200BGXI | 51-85218        | 484-ball Ball Grid Array 23 mm × 23 mm with 1.0 mm pitch (Pb-free) | Industrial      |
| 167         | CYD09S72V18-167BBXC | 51-85218        | 484-ball Ball Grid Array 23 mm × 23 mm with 1.0 mm pitch (Pb-free) | Commercial      |

### 1024 K × 36 (36-Mbit) 1.8 V/1.5 V Synchronous CYD36S36V18 Dual Port SRAM

| Speed (MHz) | Ordering Code       | Package Diagram | Package Type                                                       | Operating Range |
|-------------|---------------------|-----------------|--------------------------------------------------------------------|-----------------|
| 200         | CYD36S36V18-200BGXC | 001-07825       | 484-ball Ball Grid Array 27 mm × 27 mm with 1.0 mm pitch (Pb-free) | Commercial      |
| 167         | CYD36S36V18-167BGXC | 001-07825       | 484-ball Ball Grid Array 27 mm × 27 mm with 1.0 mm pitch (Pb-free) | Commercial      |
| 167         | CYD36S36V18-167BGXI | 001-07825       | 484-ball Ball Grid Array 27 mm × 27 mm with 1.0 mm pitch (Pb-free) | Industrial      |

### 512 K × 36 (18-Mbit) 1.8 V/1.5 V Synchronous CYD18S36V18 Dual Port SRAM

| Speed (MHz) | Ordering Code        | Package Diagram | Package Type                                                       | Operating Range |
|-------------|----------------------|-----------------|--------------------------------------------------------------------|-----------------|
| 200         | CYD18S36V18-200BBAXI | 51-85108        | 256-ball Ball Grid Array 17 mm × 17 mm with 1.0 mm pitch (Pb-free) | Industrial      |
| 167         | CYD18S36V18-167BBAI  | 51-85108        | 256-ball Ball Grid Array 17 mm × 17 mm with 1.0 mm pitch           | Industrial      |

**Ordering Information** *(continued)*
**256 K × 36 (9-Mbit) 1.8 V/1.5 V Synchronous CYD09S36V18 Dual Port SRAM**

| Speed (MHz) | Ordering Code       | Package Diagram | Package Type                                                       | Operating Range |
|-------------|---------------------|-----------------|--------------------------------------------------------------------|-----------------|
| 200         | CYD09S36V18-200BBXC | 51-85108        | 256-ball Ball Grid Array 17 mm × 17 mm with 1.0 mm pitch (Pb-free) | Commercial      |
| 200         | CYD09S36V18-200BBXI | 51-85108        | 256-ball Ball Grid Array 17 mm × 17 mm with 1.0 mm pitch (Pb-free) | Industrial      |
| 167         | CYD09S36V18-167BBXC | 51-85108        | 256-ball Ball Grid Array 17 mm × 17 mm with 1.0 mm pitch (Pb-free) | Commercial      |

**64 K × 36 (2-Mbit) 1.8 V or 1.5 V Synchronous CYD02S36V18 Dual Port SRAM**

| Speed (MHz) | Ordering Code      | Package Diagram | Package Type                                             | Operating Range |
|-------------|--------------------|-----------------|----------------------------------------------------------|-----------------|
| 200         | CYD02S36V18-200BBC | 51-85108        | 256-ball Ball Grid Array 17 mm × 17 mm with 1.0 mm pitch | Commercial      |

## Ordering Information *(continued)*

### 2048 K × 18 (36-Mbit) 1.8 V/1.5 V Synchronous CYD36S18V18 Dual Port SRAM

| Speed (MHz) | Ordering Code       | Package Diagram | Package Type                                                       | Operating Range |
|-------------|---------------------|-----------------|--------------------------------------------------------------------|-----------------|
| 200         | CYD36S18V18-200BGXC | 001-07825       | 484-ball Ball Grid Array 27 mm × 27 mm with 1.0 mm pitch (Pb-free) | Commercial      |
| 167         | CYD36S18V18-167BGXC | 001-07825       | 484-ball Ball Grid Array 27 mm × 27 mm with 1.0 mm pitch (Pb-free) | Commercial      |
| 167         | CYD36S18V18-167BGXI | 001-07825       | 484-ball Ball Grid Array 27 mm × 27 mm with 1.0 mm pitch (Pb-free) | Industrial      |

### 1024 K × 18 (18-Mbit) 1.8 V/1.5 V Synchronous CYD18S18V18 Dual Port SRAM

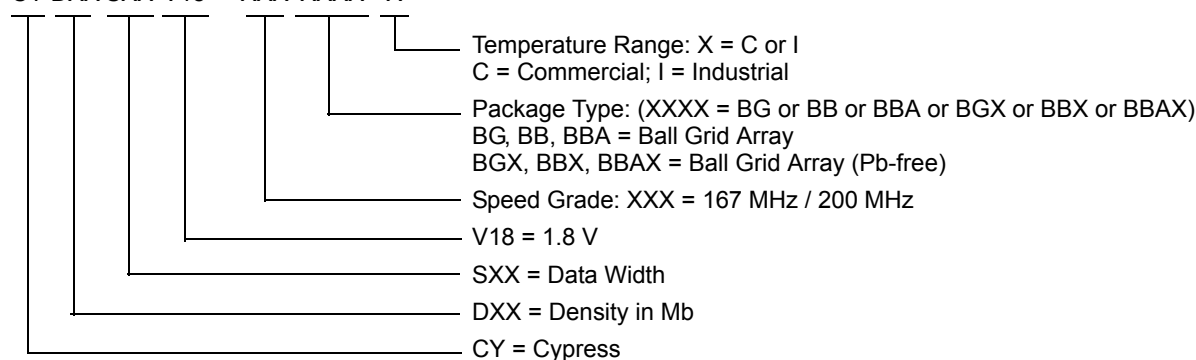
| Speed (MHz) | Ordering Code        | Package Diagram | Package Type                                                       | Operating Range |
|-------------|----------------------|-----------------|--------------------------------------------------------------------|-----------------|
| 200         | CYD18S18V18-200BBAXI | 51-85108        | 256-ball Ball Grid Array 17 mm × 17 mm with 1.0 mm pitch (Pb-free) | Industrial      |
| 200         | CYD18S18V18-200BBAXC | 51-85108        | 256-ball Ball Grid Array 17 mm × 17 mm with 1.0 mm pitch (Pb-free) | Commercial      |
| 167         | CYD18S18V18-167BBAXI | 51-85108        | 256-ball Ball Grid Array 17 mm × 17 mm with 1.0 mm pitch (Pb-free) | Industrial      |

### 512 K × 18 (9-Mbit) 1.8 V/1.5 V Synchronous CYD09S18V18 Dual Port SRAM

| Speed (MHz) | Ordering Code       | Package Diagram | Package Type                                                       | Operating Range |
|-------------|---------------------|-----------------|--------------------------------------------------------------------|-----------------|
| 200         | CYD09S18V18-200BBXC | 51-85108        | 256-ball Ball Grid Array 17 mm × 17 mm with 1.0 mm pitch (Pb-free) | Commercial      |
| 200         | CYD09S18V18-200BBXI | 51-85108        | 256-ball Ball Grid Array 17 mm × 17 mm with 1.0 mm pitch (Pb-free) | Industrial      |
| 167         | CYD09S18V18-167BBXI | 51-85108        | 256-ball Ball Grid Array 17 mm × 17 mm with 1.0 mm pitch (Pb-free) | Industrial      |

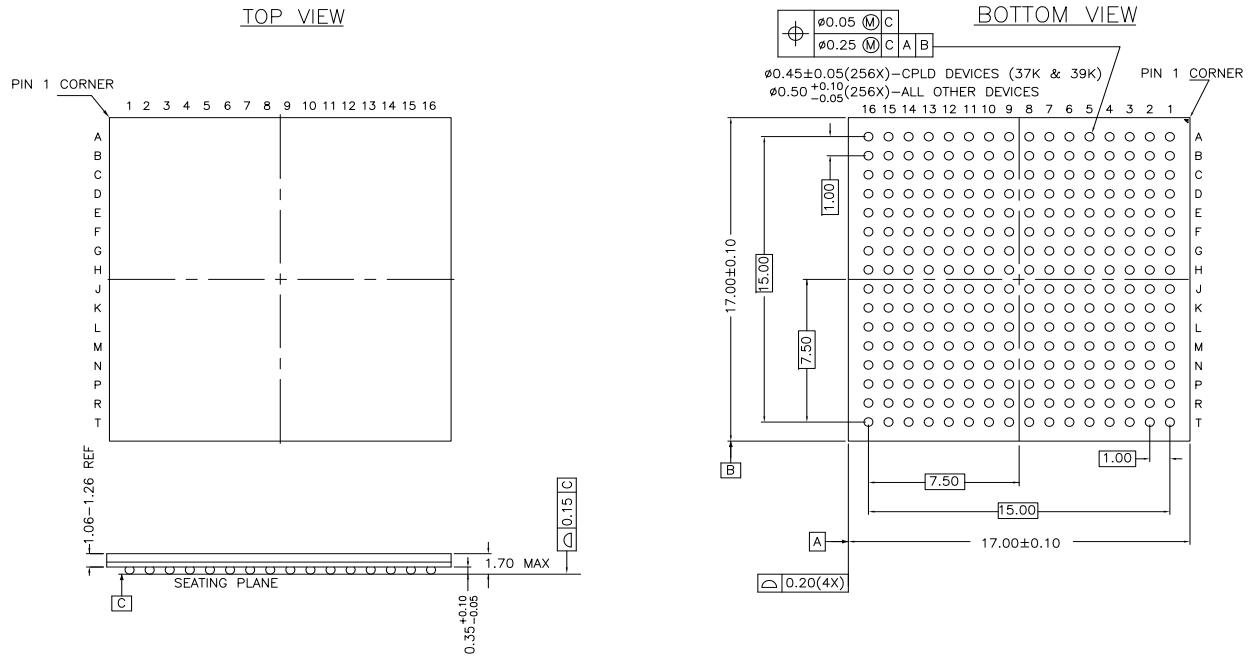
## Ordering Code Definitions

CY DXX SXX V18 - XXX XXXX X



## Package Diagrams

Figure 34. 256-ball FPBGA (17 × 17 mm), 51-85108



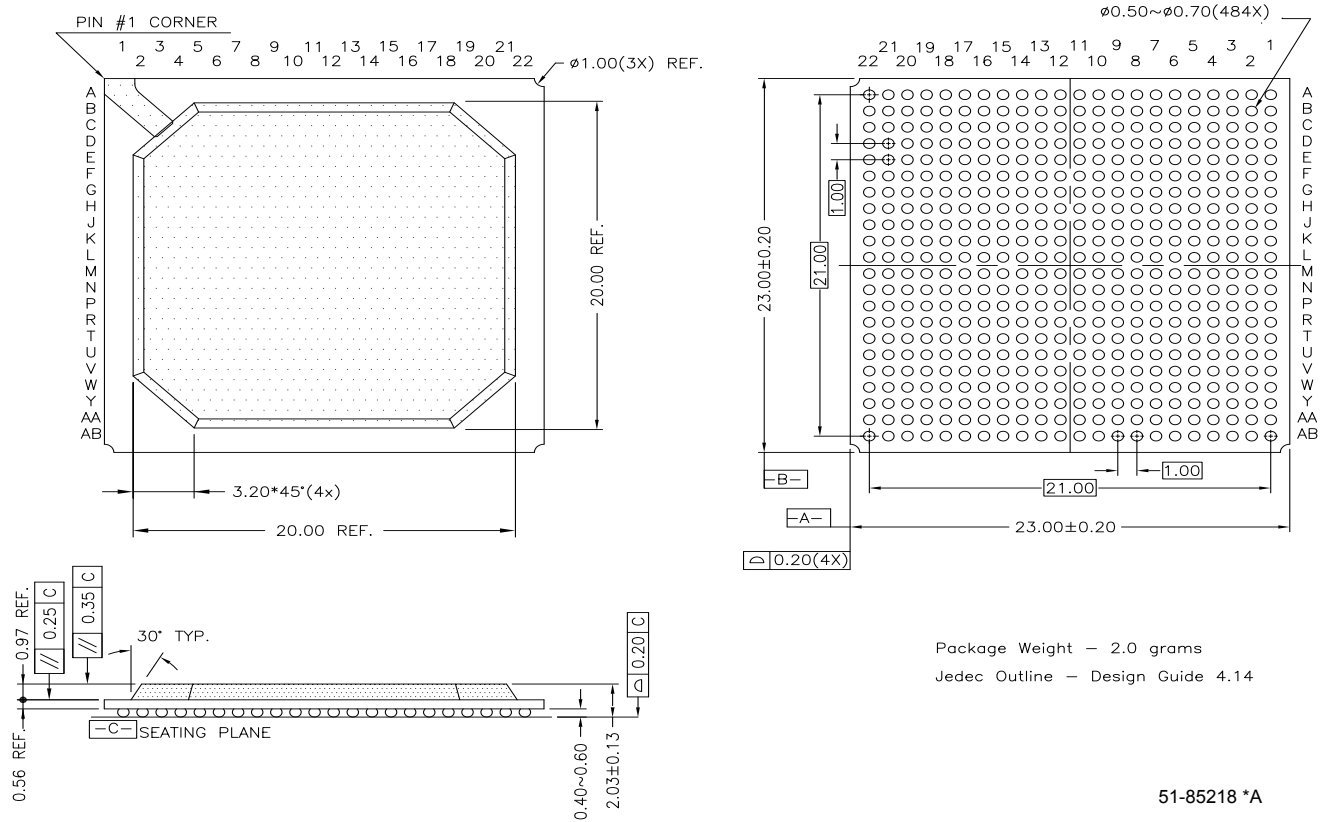
51-85108 \*H

REFERENCE JEDEC MO-192

PACKAGE WEIGHT — 0.95gr

## Package Diagrams

Figure 35. 484-ball PBGA (23 mm × 23 mm × 2.03 mm), 51-85218





## Document History Page

| Document Title: FullFlex™ Synchronous SDR Dual Port SRAM<br>Document Number: 38-06082 |         |                 |                 |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |
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| REV.                                                                                  | ECN NO. | Submission Date | Orig. of Change | Description of Change                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |
| **                                                                                    | 302411  | See ECN         | YDT             | New data sheet                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |
| *A                                                                                    | 334036  | See ECN         | YDT             | Corrected typo on page 1<br>Reproduced PDF file to fix formatting errors                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |
| *B                                                                                    | 395800  | See ECN         | SPN             | <p>Added statement about no echo clocks for flow through mode</p> <p>Updated electrical characteristics</p> <p>Added note 16 and 17 (1.5 V timing)</p> <p>Added note 33 (timing for x18 devices)</p> <p>Updated input edge rate (note 34)</p> <p>Updated table 5 on deterministic access control logic</p> <p>Added description of busy readback in deterministic access control section</p> <p>Changed dummy write descriptions</p> <p>Updated ZQ pins connection details</p> <p>Updated note 24, B0 to BE0</p> <p>Added power supply requirements to <math>\overline{\text{MRST}}</math> and VC_SEL</p> <p>Added note 4 (VIM disable)</p> <p>Updated supply voltage to ground potential to 4.1 V</p> <p>Updated parameters on table 15</p> <p>Updated and added parameters to table 16</p> <p>Updated x72 pinout to SDR only pinout</p> <p>Updated 484 PBGA pin diagram</p> <p>Updated the pin definition of <math>\overline{\text{MRST}}</math></p> <p>Updated the pin definition of VC_SEL</p> <p>Updated READY description to include Wired OR note</p> <p>Updated master reset to include wired OR note for <math>\overline{\text{READY}}</math></p> <p>Updated minimum <math>V_{\text{OH}}</math> value for the 1.8 V LVCMOS configuration</p> <p>Updated electrical characteristics to include <math>I_{\text{OH}}</math> and <math>I_{\text{OL}}</math> values</p> <p>Updated electrical characteristics to include <math>\overline{\text{READY}}</math></p> <p>Added <math>I_{\text{X3}}</math></p> <p>Updated maximum input capacitance</p> <p>Added Notes 33 and 34<br/>Removed Notes 15 and 17</p> <p>Updated Pin Definitions for CQ0, CQ0, CQ1, and CQ1</p> <p>Removed -100 Speed bin from Table.1 Selection Guide</p> <p>Changed voltage name from <math>V_{\text{DDQ}}</math> to <math>V_{\text{DDIO}}</math></p> <p>Changed voltage name from <math>V_{\text{DD}}</math> to <math>V_{\text{CORE}}</math></p> <p>Moved the Mailbox Interrupt Timing Diagram to be the final timing diagram</p> <p>Updated the Package Type for the CYD36S18V18 parts</p> <p>Updated the Package Type for the CYD36S18V18 parts</p> <p>Updated the Package Type for the CYD18S18V18 parts</p> <p>Updated the Package Type for the CYD18S36V18 parts</p> <p>Included the Package Diagram for the 256-Ball FBGA (19 x 19 mm) BW256</p> <p>Included an OE Controlled Write for Flow through Mode Switching Waveform</p> <p>Included a Read with Echo Clock Switching Waveform</p> <p>Updated Figure 5 and Figure 6</p> <p>Updated Electrical Characteristics for <math>\overline{\text{READY}}</math> <math>V_{\text{OH}}</math> and <math>\overline{\text{READY}}</math> V</p> <p>Updated Electrical Characteristics for <math>V_{\text{OH}}</math> and <math>V_{\text{OL}}</math> for the -167 and -133 speeds</p> <p>Included a Unit column for Table 5</p> <p>Removed Switching Characteristic <math>t_{\text{CA}}</math> from chart</p> <p>Included <math>t_{\text{OHZ}}</math> in Switching Waveform OE Controlled Write for Pipelined Mode</p> <p>Included <math>t_{\text{CKLZ2}}</math> in Waveform Read-to-Write-to-Read for Flow through Mode</p> |

**Document History Page** *(continued)*

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| REV.                                                                                  | ECN NO. | Submission Date | Orig. of Change | Description of Change                                                                                                                                                                                                                                                                                                                                                                                                              |
| *C                                                                                    | 402238  | SEE ECN         | KGH             | Updated AC Test Load and Waveforms<br>Included FullFlex36 SDR 484-Ball BGA Pinout (Top View)<br>Included FullFlex18 SDR 484-Ball BGA Pinout (Top View)<br>Included Timing Parameter $t_{CORDY}$                                                                                                                                                                                                                                    |
| *D                                                                                    | 458131  | SEE ECN         | YDT             | Changed ordering information with Pb-free part numbers<br>Removed VC_SEL<br>Added IO and core voltage adders<br>Removed references to bin drop for LVTTL/2.5 V LVCMOS and 1.5 V core modes<br>Updated Cin and Cout<br>Updated ICC, ISB1, ISB2 and ISB3 tables<br>Updated busy address read back timing diagram<br>Added HTSL input waveform<br>Removed HSTL (AC) from DC tables<br>Added 484-ball 27 mmx27 mmx2.33 mm PBGA package |
| *E                                                                                    | 470031  | SEE ECN         | YDT             | Changed VOL of 1.8 V LVCMOS to 0.45 V<br>Updated tRSF<br>VREF is DNU when HSTL is not used<br>Formatted pin description table<br>Changed VDDIO pins for 36M x 36 and 36M x 18 pinouts<br>Changed 36Mx72 JTAG IDCODE                                                                                                                                                                                                                |
| *F                                                                                    | 500001  | SEE ECN         | YDT             | DLL Change, added Clock Input Cycle to Cycle Jitter<br>Modified DLL description<br>Changed Input Capacitance Table<br>Changed tCCS number<br>Added note 31                                                                                                                                                                                                                                                                         |
| *G                                                                                    | 627539  | SEE ECN         | QSL             | change all NC to DNU<br>corrected switching waveform for (CQEN = High) from both Pipeline and Flow through mode to only pipeline mode<br>Modified master reset description<br>Modified switching characteristics tables, extracted signals effected by the DLL into one table and combine all other signals into one table<br>updated package name<br>Added footnote for tHD, tHAC and tSAC<br>changed note 26 description         |

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| REV.                                                                                  | ECN NO. | Submission Date | Orig. of Change | Description of Change                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |
| *H                                                                                    | 2505003 | See ECN         | VKN/<br>AESA    | Modified footnote #1<br>Removed 250 MHz speed bin<br>Added 2-Mbit part and it's related information<br>Changed ball name ZQ1 to DNU for 18M and lesser density devices<br>Added 256-Ball (17 x 17 mm) BGA package for 18M<br>Made PORTSTD[1:0] left and right pins driven only by LVTTTL reference level<br>For 1.8V LVCMOS level, Changed $V_{IH(min)}$ from 1.26V to 0.65 times $V_{DDIO}$ and<br>Changed $V_{IL(max)}$ from 0.36V to 0.35 times $V_{DDIO}$<br>Changed tHD, tHAC specs for 36M from 0.6 ns/0.7 ns to 0.8 ns (See footnote# 32)<br>Updated Ordering Information table |
| *I                                                                                    | 2898491 | 07/01/2010      | RAME            | Modified "Counter Load Operation" section on page 12 and in Table7. on page 13.<br>Corrected typo in Table 14. by making LowSPD = 0 for $t_{CD1}$ spec in the description.<br>Modified figure 16. on page 30.<br>Removed inactive parts from Ordering Information.<br>Updated Packaging Information.<br>Corrected "Counter Interrupt operation" Section in Page 14 of the datasheet<br>Updated ordering information with the parts, CYD02S36V18-200BBC and CYD36S72V18-167BGI.                                                                                                         |
| *J                                                                                    | 2995098 | 07/28/2010      | RAME            | Updated <a href="#">Ordering Information</a> and added <a href="#">Ordering Code Definitions</a> .<br>Added <a href="#">Acronyms</a> and <a href="#">Units of Measure</a> .<br>Minor edits.                                                                                                                                                                                                                                                                                                                                                                                            |
| *K                                                                                    | 3267210 | 05/26/2011      | ADMU            | Updated <a href="#">Electrical Characteristics on page 21</a> (Removed 133 MHz speed bin).<br>Updated <a href="#">Switching Characteristics on page 26</a> (Removed 133 MHz speed bin).<br>Removed information for 4Mb devices.<br>Updated <a href="#">Ordering Information</a> .                                                                                                                                                                                                                                                                                                      |

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