

**4-Mb (512K x 8) MoBL<sup>®</sup> Static RAM****Features**

- Very high speed: 55 ns
  - Wide voltage range: 2.20V – 3.60V
- Pin-compatible with CY62148CV25, CY62148CV30 and CY62148CV33
- Ultra low active power
  - Typical active current: 1.5 mA @ f = 1 MHz
  - Typical active current: 8 mA @ f = f<sub>max</sub> (55-ns speed)
- Ultra low standby power
- Easy memory expansion with  $\overline{\text{CE}}$ , and  $\overline{\text{OE}}$  features
- Automatic power-down when deselected
- CMOS for optimum speed/power
- Packages offered: 36-ball BGA, 32-pin TSOPII and 32-pin SOIC

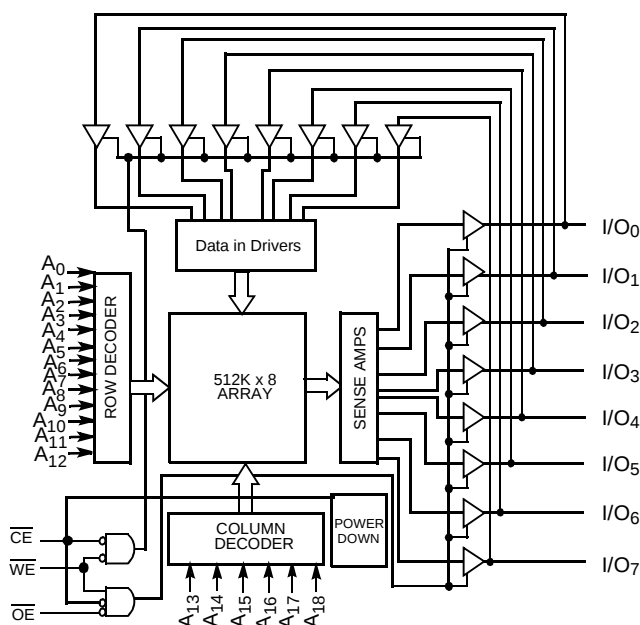
**Functional Description<sup>[1]</sup>**

The CY62148DV30 is a high-performance CMOS static RAMs organized as 512K words by 8 bits. This device features advanced circuit design to provide ultra-low active current. This is ideal for providing More Battery Life<sup>™</sup> (MoBL<sup>®</sup>) in portable applications such as cellular telephones. The device also has an automatic power-down feature that significantly reduces power consumption. The device can be put into standby mode reducing power consumption when deselected ( $\overline{\text{CE}}$  HIGH).

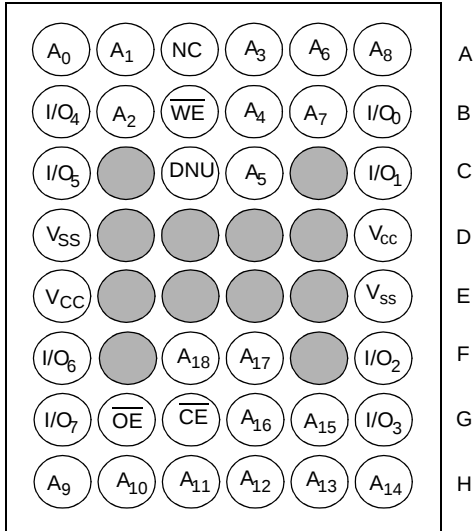
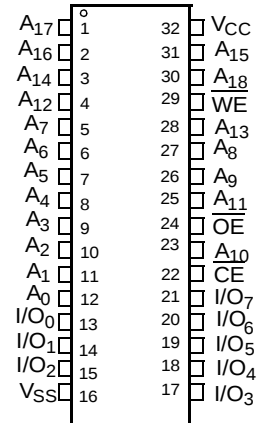
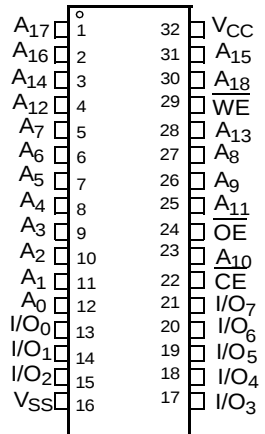
Writing to the device is accomplished by taking Chip Enable ( $\overline{\text{CE}}$ ) and Write Enable ( $\overline{\text{WE}}$ ) inputs LOW. Data on the eight I/O pins (I/O<sub>0</sub> through I/O<sub>7</sub>) is then written into the location specified on the address pins (A<sub>0</sub> through A<sub>18</sub>).

Reading from the device is accomplished by taking Chip Enable ( $\overline{\text{CE}}$ ) and Output Enable ( $\overline{\text{OE}}$ ) LOW while forcing Write Enable ( $\overline{\text{WE}}$ ) HIGH. Under these conditions, the contents of the memory location specified by the address pins will appear on the I/O pins.

The eight input/output pins (I/O<sub>0</sub> through I/O<sub>7</sub>) are placed in a high-impedance state when the device is deselected ( $\overline{\text{CE}}$  HIGH), the outputs are disabled ( $\overline{\text{OE}}$  HIGH), or during a write operation ( $\overline{\text{CE}}$  LOW and  $\overline{\text{WE}}$  LOW).

**Logic Block Diagram****Note:**

1. For best practice recommendations, please refer to the Cypress application note "System Design Guidelines" on <http://www.cypress.com>.

**Pin Configuration<sup>[2,3]</sup>**
**FBGA  
Top View**

**32 TSOPII  
Top View**

**32 SOIC  
Top View**

**Notes:**

- NC pins are not connected on the die.
- DNU pins have to be left floating or tied to V<sub>SS</sub> to ensure proper application.

## Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... -65°C to +150°C

Ambient Temperature with  
Power Applied ..... 55°C to +125°C

Supply Voltage to Ground  
Potential ..... -0.3V to  $V_{CC(MAX)}$  + 0.3V

DC Voltage Applied to Outputs  
in High-Z State<sup>[4,5]</sup> ..... -0.3V to  $V_{CC(MAX)}$  + 0.3V

DC Input Voltage<sup>[4,5]</sup> ..... -0.3V to  $V_{CC(MAX)}$  + 0.3V

Output Current into Outputs (LOW) ..... 20 mA

Static Discharge Voltage ..... > 2001V  
(per MIL-STD-883, Method 3015)

Latch-up Current ..... > 200 mA

## Operating Range

| Product       | Range      | Ambient Temperature | $V_{CC}$ <sup>[6]</sup> |
|---------------|------------|---------------------|-------------------------|
| CY62148DV30L  | Industrial | -40°C to +85°C      | 2.2V to 3.6V            |
| CY62148DV30LL |            |                     |                         |

## Product Portfolio

| Product       | V <sub>CC</sub> Range (V) |                     |                      | Speed (ns) | Power Dissipation              |      |                     |      |                               |      |
|---------------|---------------------------|---------------------|----------------------|------------|--------------------------------|------|---------------------|------|-------------------------------|------|
|               |                           |                     |                      |            | Operating I <sub>CC</sub> (mA) |      |                     |      | Standby I <sub>SB2</sub> (uA) |      |
|               | f = 1 MHz                 |                     | f = f <sub>max</sub> |            |                                |      |                     |      |                               |      |
|               | Min.                      | Typ. <sup>[7]</sup> | Max.                 |            | Typ. <sup>[7]</sup>            | Max. | Typ. <sup>[7]</sup> | Max. | Typ. <sup>[7]</sup>           | Max. |
| CY62148DV30L  | 2.2                       | 3.0                 | 3.6                  | 55         | 1.5                            | 3    | 8                   | 15   | 2                             | 12   |
| CY62148DV30LL | 2.2                       | 3.0                 | 3.6                  | 55         |                                | 3    |                     | 10   |                               | 8    |
| CY62148DV30L  | 2.2                       | 3.0                 | 3.6                  | 70         | 1.5                            | 3    | 8                   | 15   | 2                             | 12   |
| CY62148DV30LL | 2.2                       | 3.0                 | 3.6                  | 70         |                                | 3    |                     | 10   |                               | 8    |

## Electrical Characteristics Over the Operating Range

| Parameter        | Description                                   | Test Conditions                                                                                                                                                                                |                                                                                | CY62148DV30-55 |                     |                        | CY62148DV30-70 |                     |                        | Unit |
|------------------|-----------------------------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------------------------------------------------------------------------------|----------------|---------------------|------------------------|----------------|---------------------|------------------------|------|
|                  |                                               |                                                                                                                                                                                                |                                                                                | Min.           | Typ. <sup>[7]</sup> | Max.                   | Min.           | Typ. <sup>[7]</sup> | Max.                   |      |
| V <sub>OH</sub>  | Output HIGH Voltage                           | I <sub>OH</sub> = −0.1 mA                                                                                                                                                                      | V <sub>CC</sub> = 2.20V                                                        | 2.0            |                     |                        | 2.0            |                     |                        | V    |
|                  |                                               | I <sub>OH</sub> = −1.0 mA                                                                                                                                                                      | V <sub>CC</sub> = 2.70V                                                        | 2.4            |                     |                        | 2.4            |                     |                        | V    |
| V <sub>OL</sub>  | Output LOW Voltage                            | I <sub>OL</sub> = 0.1 mA                                                                                                                                                                       | V <sub>CC</sub> = 2.20V                                                        |                |                     | 0.4                    |                |                     | 0.4                    | V    |
|                  |                                               | I <sub>OL</sub> = 2.1 mA                                                                                                                                                                       | V <sub>CC</sub> = 2.70V                                                        |                |                     | 0.4                    |                |                     | 0.4                    | V    |
| V <sub>IH</sub>  | Input HIGH Voltage                            | V <sub>CC</sub> = 2.2V to 2.7V                                                                                                                                                                 |                                                                                | 1.8            |                     | V <sub>CC</sub> + 0.3V | 1.8            |                     | V <sub>CC</sub> + 0.3V | V    |
|                  |                                               | V <sub>CC</sub> = 2.7V to 3.6V                                                                                                                                                                 |                                                                                | 2.2            |                     | V <sub>CC</sub> + 0.3V | 2.2            |                     | V <sub>CC</sub> + 0.3V | V    |
| V <sub>IL</sub>  | Input LOW Voltage                             | V <sub>CC</sub> = 2.2V to 2.7V                                                                                                                                                                 |                                                                                | −0.3           |                     | 0.6                    | −0.3           |                     | 0.6                    | V    |
|                  |                                               | V <sub>CC</sub> = 2.7V to 3.6V                                                                                                                                                                 |                                                                                | −0.3           |                     | 0.8                    | −0.3           |                     | 0.8                    | V    |
| I <sub>IX</sub>  | Input Leakage Current                         | GND ≤ V <sub>I</sub> ≤ V <sub>CC</sub>                                                                                                                                                         |                                                                                | −1             |                     | +1                     | −1             |                     | +1                     | μA   |
| I <sub>OZ</sub>  | Output Leakage Current                        | GND ≤ V <sub>O</sub> ≤ V <sub>CC</sub> , Output Disabled                                                                                                                                       |                                                                                | −1             |                     | +1                     | −1             |                     | +1                     | μA   |
| I <sub>CC</sub>  | V <sub>CC</sub> Operating Supply Current      | f = f <sub>MAX</sub> = 1/t <sub>RC</sub>                                                                                                                                                       | V <sub>CC</sub> = V <sub>CCmax</sub><br>I <sub>OUT</sub> = 0 mA<br>CMOS levels | L              | 8                   | 15                     |                | 8                   | 15                     | mA   |
|                  |                                               |                                                                                                                                                                                                |                                                                                | LL             |                     | 10                     |                |                     | 10                     | mA   |
|                  |                                               | f = 1 MHz                                                                                                                                                                                      |                                                                                | L              | 1.5                 | 3                      |                | 1.5                 | 3                      | mA   |
|                  |                                               |                                                                                                                                                                                                |                                                                                | LL             |                     |                        |                |                     |                        | mA   |
| I <sub>SB1</sub> | Automatic CE Power-down Current — CMOS Inputs | CE ≥ V <sub>CC</sub> − 0.2V, V <sub>IN</sub> ≥ V <sub>CC</sub> − 0.2V, V <sub>IN</sub> ≤ 0.2V)<br>f = f <sub>MAX</sub> (Address and Data Only),<br>f = 0 (OE, and WE), V <sub>CC</sub> = 3.60V |                                                                                | L              | 2                   | 12                     |                | 2                   | 12                     | μA   |
|                  |                                               |                                                                                                                                                                                                |                                                                                | LL             |                     | 8                      |                |                     | 8                      |      |
| I <sub>SB2</sub> | Automatic CE Power-down Current — CMOS Inputs | CE ≥ V <sub>CC</sub> − 0.2V, V <sub>IN</sub> ≥ V <sub>CC</sub> − 0.2V or V <sub>IN</sub> ≤ 0.2V, f = 0, V <sub>CC</sub> = 3.60V                                                                |                                                                                | L              | 2                   | 12                     |                | 2                   | 12                     | μA   |
|                  |                                               |                                                                                                                                                                                                |                                                                                | LL             |                     | 8                      |                |                     | 8                      |      |

### Notes:

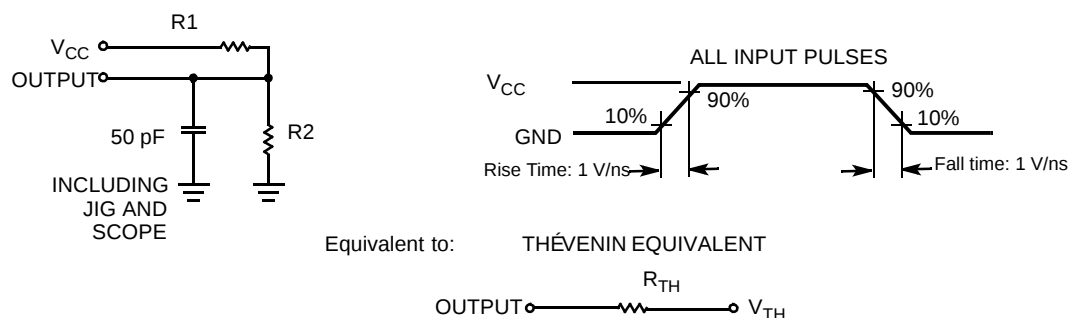
- $V_{IL(min.)} = -2.0$  V for pulse durations less than 20 ns.
- $V_{IH(max.)} = V_{CC} + 0.75$  V for pulse durations less than 20 ns.
- Full device AC operation assumes a 100 μs ramp time from 0 to  $V_{CC(min)}$  and 200 μs wait time after  $V_{CC}$  stabilization.
- Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at  $V_{CC} = V_{CC(typ.)}$ ,  $T_A = 25^\circ\text{C}$ .

**Capacitance** for all packages<sup>[8]</sup>

| Parameter | Description        | Test Conditions                                                                   | Max. | Unit |
|-----------|--------------------|-----------------------------------------------------------------------------------|------|------|
| $C_{IN}$  | Input Capacitance  | $T_A = 25^\circ\text{C}$ , $f = 1\text{ MHz}$ ,<br>$V_{CC} = V_{CC}(\text{typ.})$ | 10   | pF   |
| $C_{OUT}$ | Output Capacitance |                                                                                   | 10   | pF   |

**Thermal Resistance**

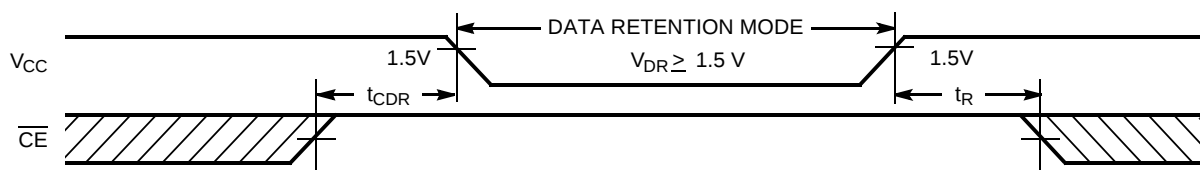
| Parameter     | Description                              | Test Conditions                                                         | BGA  | TSOP II | SOIC | STSOP | Unit               |
|---------------|------------------------------------------|-------------------------------------------------------------------------|------|---------|------|-------|--------------------|
| $\Theta_{JA}$ | Thermal Resistance (Junction to Ambient) | Still Air, soldered on a 3 x 4.5 inch, four-layer printed circuit board | 72   | 75.13   | 55   | 105   | $^\circ\text{C/W}$ |
| $\Theta_{JC}$ | Thermal Resistance (Junction to Case)    |                                                                         | 8.86 | 8.95    | 22   | 13    | $^\circ\text{C/W}$ |

**AC Test Loads and Waveforms**


| Parameters      | 2.50V | 3.0V | Unit     |
|-----------------|-------|------|----------|
| R1              | 16667 | 1103 | $\Omega$ |
| R2              | 15385 | 1554 | $\Omega$ |
| R <sub>TH</sub> | 8000  | 645  | $\Omega$ |
| V <sub>TH</sub> | 1.20  | 1.75 | V        |

**Data Retention Characteristics** (Over the Operating Range)

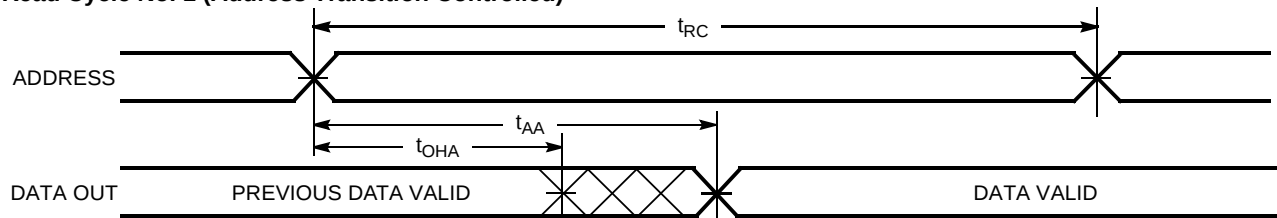
| Parameter                       | Description                          | Conditions                                                                                                                                     | Min.            | Typ. <sup>[7]</sup> | Max. | Unit          |
|---------------------------------|--------------------------------------|------------------------------------------------------------------------------------------------------------------------------------------------|-----------------|---------------------|------|---------------|
| V <sub>DR</sub>                 | V <sub>CC</sub> for Data Retention   |                                                                                                                                                | 1.5             |                     |      | V             |
| I <sub>CCDR</sub>               | Data Retention Current               | $V_{CC} = 1.5\text{V}$ , $\overline{\text{CE}} \geq V_{CC} - 0.2\text{V}$ ,<br>$V_{IN} \geq V_{CC} - 0.2\text{V}$ or $V_{IN} \leq 0.2\text{V}$ | L               |                     | 9    | $\mu\text{A}$ |
|                                 |                                      |                                                                                                                                                | LL              |                     | 6    | $\mu\text{A}$ |
| t <sub>CDR</sub> <sup>[8]</sup> | Chip Deselect to Data Retention Time |                                                                                                                                                | 0               |                     |      | ns            |
| t <sub>R</sub> <sup>[9]</sup>   | Operation Recovery Time              |                                                                                                                                                | t <sub>RC</sub> |                     |      | ns            |

**Data Retention Waveform**

**Notes:**

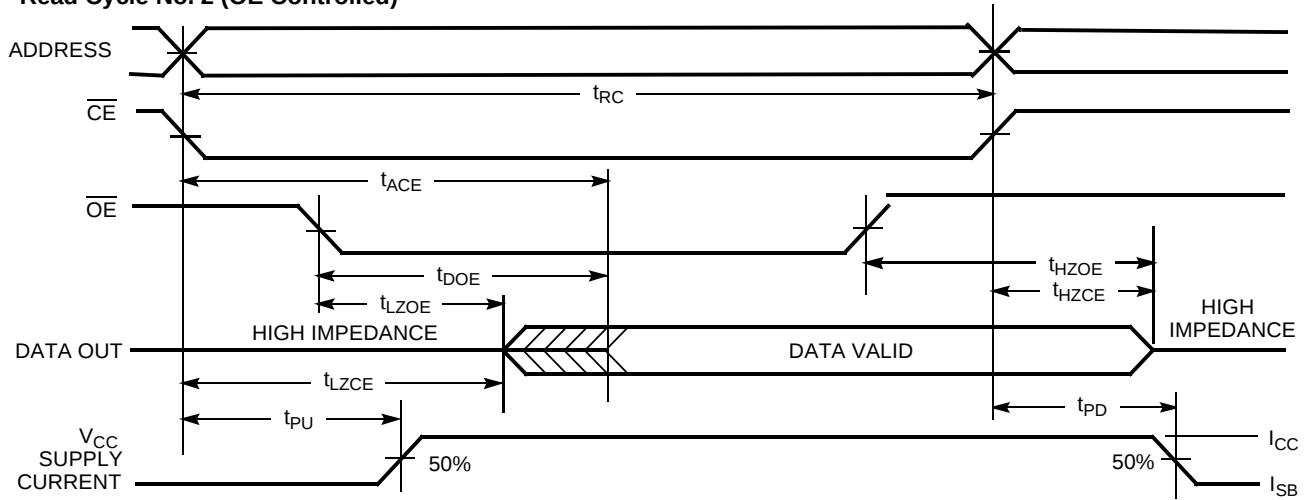
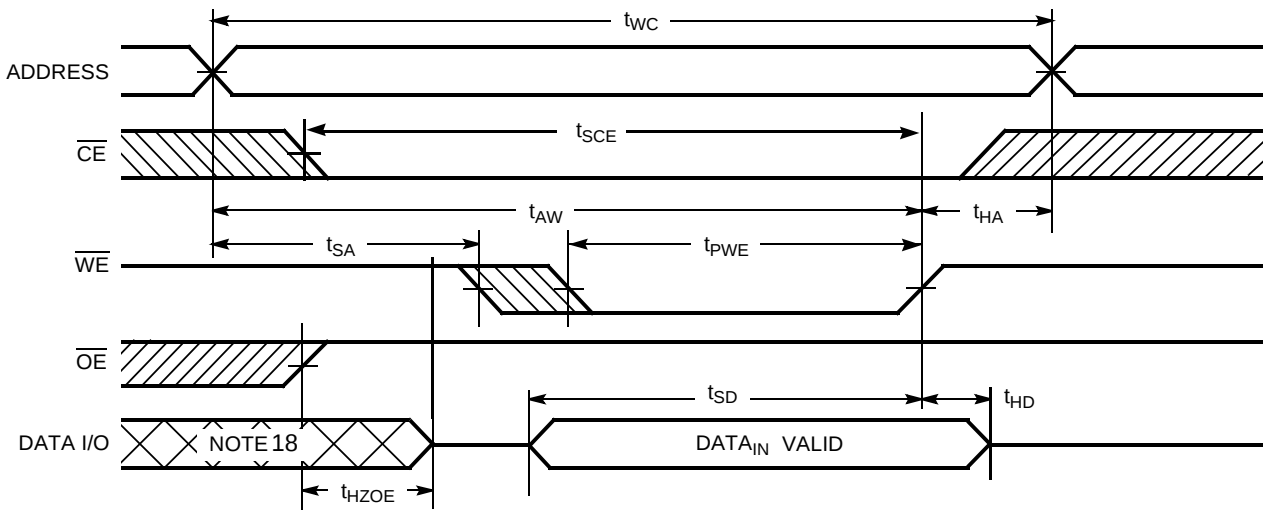
8. Tested initially and after any design or process changes that may affect these parameters.
9. Full Device AC operation requires linear V<sub>CC</sub> ramp from V<sub>DR</sub> to V<sub>CC(min.)</sub> ≥ 100  $\mu\text{s}$  or stable at V<sub>CC(min.)</sub> ≥ 100  $\mu\text{s}$ .

**Switching Characteristics** (Over the Operating Range)<sup>[10]</sup>

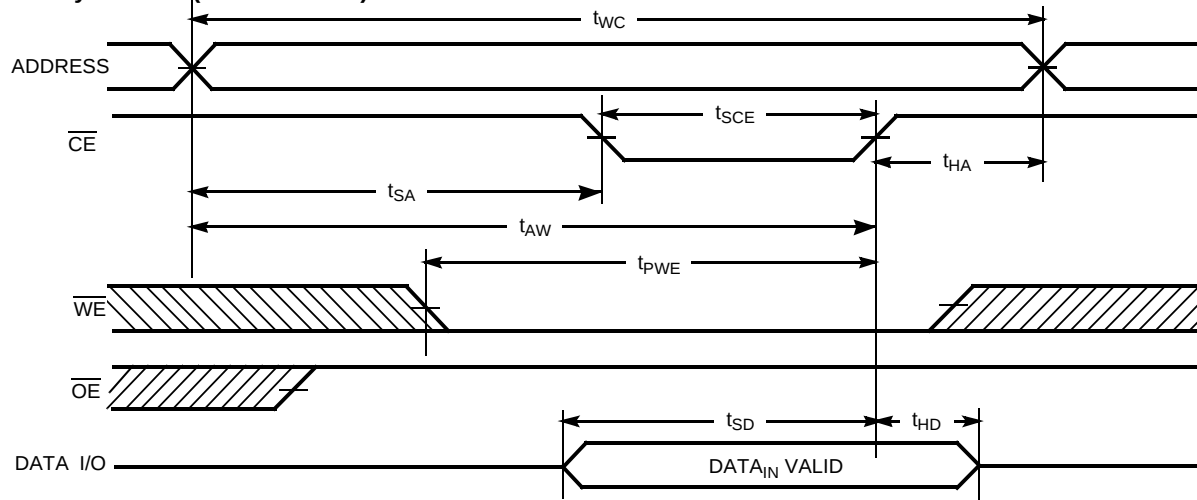
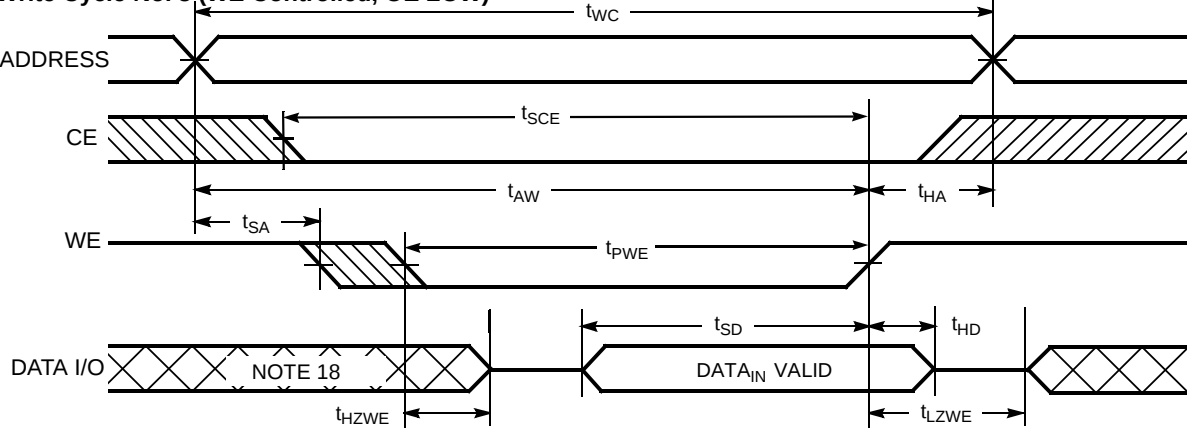
| Parameter                   | Description                           | 55 ns |      | 70 ns |      | Unit |
|-----------------------------|---------------------------------------|-------|------|-------|------|------|
|                             |                                       | Min.  | Max. | Min.  | Max. |      |
| Read Cycle                  |                                       |       |      |       |      |      |
| t <sub>RC</sub>             | Read Cycle Time                       | 55    |      | 70    |      | ns   |
| t <sub>AA</sub>             | Address to Data Valid                 |       | 55   |       | 70   | ns   |
| t <sub>OHA</sub>            | Data Hold from Address Change         | 10    |      | 10    |      | ns   |
| t <sub>ACE</sub>            | CE LOW to Data Valid                  |       | 55   |       | 70   | ns   |
| t <sub>DOE</sub>            | OE LOW to Data Valid                  |       | 25   |       | 35   | ns   |
| t <sub>LZOE</sub>           | OE LOW to Low Z <sup>[11]</sup>       | 5     |      | 5     |      | ns   |
| t <sub>HZOE</sub>           | OE HIGH to High Z <sup>[11,12]</sup>  |       | 20   |       | 25   | ns   |
| t <sub>LZCE</sub>           | CE LOW to Low Z <sup>[11]</sup>       | 10    |      | 10    |      | ns   |
| t <sub>HZCE</sub>           | CE HIGH to High Z <sup>[11, 12]</sup> |       | 20   |       | 25   | ns   |
| t <sub>PU</sub>             | CE LOW to Power-up                    | 0     |      | 0     |      | ns   |
| t <sub>PD</sub>             | CE HIGH to Power-up                   |       | 55   |       | 70   | ns   |
| Write Cycle <sup>[13]</sup> |                                       |       |      |       |      |      |
| t <sub>WC</sub>             | Write Cycle Time                      | 55    |      | 70    |      | ns   |
| t <sub>SCE</sub>            | CE LOW to Write End                   | 40    |      | 45    |      | ns   |
| t <sub>AW</sub>             | Address Set-up to Write End           | 40    |      | 45    |      | ns   |
| t <sub>HA</sub>             | Address Hold from Write End           | 0     |      | 0     |      | ns   |
| t <sub>SA</sub>             | Address Set-up to Write Start         | 0     |      | 0     |      | ns   |
| t <sub>PWE</sub>            | WE Pulse Width                        | 40    |      | 45    |      | ns   |
| t <sub>SD</sub>             | Data Set-up to Write End              | 25    |      | 30    |      | ns   |
| t <sub>HD</sub>             | Data Hold from Write End              | 0     |      | 0     |      | ns   |
| t <sub>HZWE</sub>           | WE LOW to High Z <sup>[11, 12]</sup>  |       | 20   |       | 25   | ns   |
| t <sub>LZWE</sub>           | WE HIGH to Low Z <sup>[11]</sup>      | 10    |      | 10    |      | ns   |

**Switching Waveforms**
**Read Cycle No. 1 (Address Transition Controlled)<sup>[14, 15]</sup>**

**Notes:**

- Test Conditions for all parameters other than three-state parameters assume signal transition time of 3 ns or less (1 V/ns), timing reference levels of  $V_{CC(typ)}/2$ , input pulse levels of 0 to  $V_{CC(typ)}$ , and output loading of the specified  $I_{OL}/I_{OH}$  as shown in the "AC Test Loads and Waveforms" section.
- At any given temperature and voltage condition,  $t_{HZCE}$  is less than  $t_{LZCE}$ ,  $t_{HZOE}$  is less than  $t_{LZOE}$ , and  $t_{HZWE}$  is less than  $t_{LZWE}$  for any given device.
- $t_{HZOE}$ ,  $t_{HZCE}$ , and  $t_{HZWE}$  transitions are measured when the output enters a high impedance state.
- The internal write time of the memory is defined by the overlap of  $\overline{WE}$ ,  $\overline{CE} = V_{IL}$ . All signals must be ACTIVE to initiate a write and any of these signals can terminate a write by going INACTIVE. The data input set-up and hold timing should be referenced to the edge of the signal that terminates the write.
- Device is continuously selected.  $\overline{OE}$ ,  $\overline{CE} = V_{IL}$ .
- $\overline{WE}$  is HIGH for read cycle.

**Switching Waveforms (continued)**
**Read Cycle No. 2 ( $\overline{OE}$  Controlled)** [15, 16]

**Write Cycle No. 1 ( $\overline{WE}$  Controlled)** [17, 19]

**Notes:**

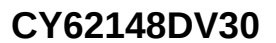
16. Address valid prior to or coincident with  $\overline{CE}$  transition LOW.
17. Data I/O is high impedance if  $OE = V_{IH}$ .
18. During this period, the I/Os are in output state and input signals should not be applied.
19. If CE goes HIGH simultaneously with WE HIGH, the output remains in high-impedance state.

**Switching Waveforms (continued)**
**Write Cycle No. 2 ( $\overline{\text{CE}}$  Controlled)<sup>[17, 19]</sup>**

**Write Cycle No. 3 ( $\overline{\text{WE}}$  Controlled,  $\overline{\text{OE}}$  LOW)<sup>[19]</sup>**

**Truth Table**

| $\overline{\text{CE}}$ | $\overline{\text{WE}}$ | $\overline{\text{OE}}$ | Inputs/Outputs                 | Mode                | Power                       |
|------------------------|------------------------|------------------------|--------------------------------|---------------------|-----------------------------|
| H                      | X                      | X                      | High Z                         | Deselect/Power-down | Standby ( $I_{\text{SB}}$ ) |
| L                      | H                      | L                      | Data Out ( $I/O_0$ - $I/O_7$ ) | Read                | Active ( $I_{\text{CC}}$ )  |
| L                      | H                      | H                      | High Z                         | Output Disabled     | Active ( $I_{\text{CC}}$ )  |
| L                      | L                      | X                      | Data in ( $I/O_0$ - $I/O_7$ )  | Write               | Active ( $I_{\text{CC}}$ )  |

**Ordering Information**

| Speed (ns) | Ordering Code        | Package Name | Package Type                                             | Operating Range |
|------------|----------------------|--------------|----------------------------------------------------------|-----------------|
| 55         | CY62148DV30L-55BVI   | BV36A        | 36-ball Very Fine Pitch BGA (6 mm × 8 mm × 1 mm)         | Industrial      |
|            | CY62148DV30LL-55BVI  |              |                                                          |                 |
| 55         | CY62148DV30L-55BVXI  | BV36A        | 36-ball Very Fine Pitch BGA (6 mm × 8 mm × 1 mm) Pb-free | Industrial      |
|            | CY62148DV30LL-55BVXI |              |                                                          |                 |
| 55         | CY62148DV30L-55ZSXI  | ZS-32        | 32-pin TSOP II Pb-free                                   | Industrial      |
|            | CY62148DV30LL-55ZSXI |              |                                                          |                 |
| 55         | CY62148DV30L-55SXI   | S-32         | 32-pin SOIC Pb-free                                      | Industrial      |
|            | CY62148DV30LL-55SXI  |              |                                                          |                 |



| Speed (ns) | Ordering Code        | Package Name | Package Type                                             | Operating Range |
|------------|----------------------|--------------|----------------------------------------------------------|-----------------|
| 70         | CY62148DV30L-70BVI   | BV36A        | 36-ball Very Fine Pitch BGA (6 mm × 8 mm × 1 mm)         | Industrial      |
|            | CY62148DV30LL-70BVI  |              |                                                          |                 |
| 70         | CY62148DV30L-70BVXI  | BV36A        | 36-ball Very Fine Pitch BGA (6 mm × 8 mm × 1 mm) Pb-free | Industrial      |
|            | CY62148DV30LL-70BVXI |              |                                                          |                 |
| 70         | CY62148DV30L-70ZSXI  | ZS-32        | 32-pin TSOP II Pb-free                                   | Industrial      |
|            | CY62148DV30LL-70ZSXI |              |                                                          |                 |
| 70         | CY62148DV30L-70SXI   | S-32         | 32-pin SOIC Pb-free                                      | Industrial      |
|            | CY62148DV30LL-70SXI  |              |                                                          |                 |

**TOP VIEW**

A1 CORNER

1 2 3 4 5 6

A B C D E F G H

8.00±0.10

6.00±0.10

**BOTTOM VIEW**

A1 CORNER

6 5 4 3 2 1

A B C D E F G H

8.00±0.10

6.00±0.10

0.05 (M) C

0.25 (M) C A B

0.30±0.05(36X)

6.25

0.75

2.625

1.875

0.75

3.75

0.15(4X)

**SIDE VIEW**

0.26 MAX.

0.55 MAX.

0.21±0.05

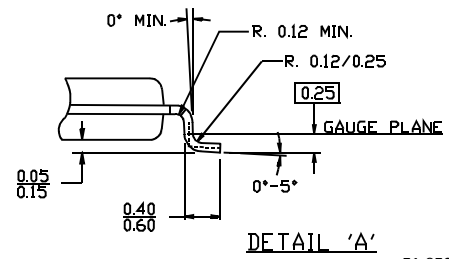
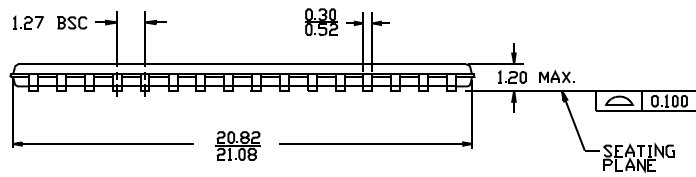
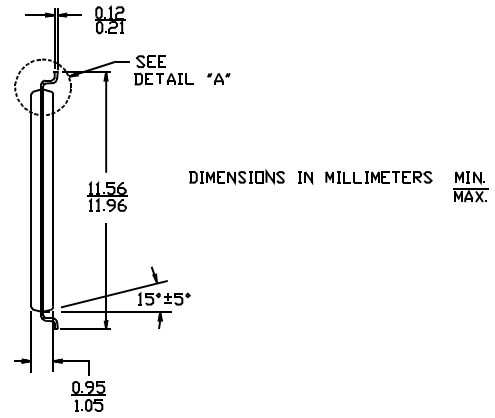
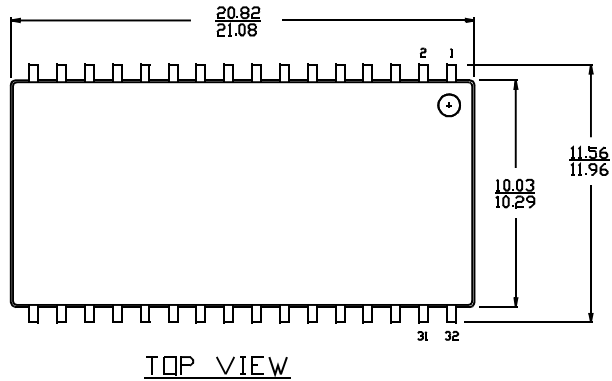
1.00 MAX.

SEATING PLANE

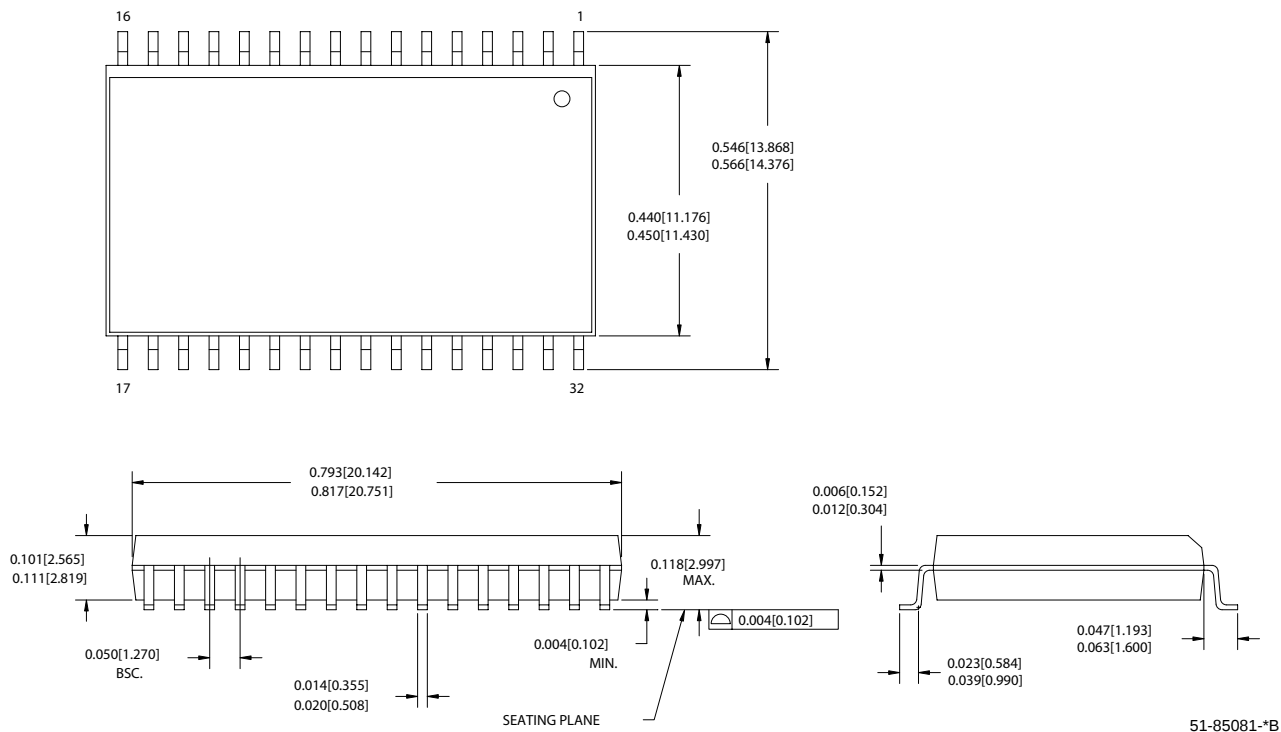
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Package Diagrams (continued)

32-Lead TSOP II ZS32



51-85095-\*\*

**Package Diagrams (continued)**
**32-Lead (450 MIL) Molded SOIC S34**


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**Document History Page**

| Document Title: CY62148DV30 4-Mb (512K x 8) MoBL <sup>®</sup> Static RAM<br>Document Number: 38-05341 |         |            |                 |                                                                                                                                                                                                                                                                                             |
|-------------------------------------------------------------------------------------------------------|---------|------------|-----------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| REV.                                                                                                  | ECN NO. | Issue Date | Orig. of Change | Description of Change                                                                                                                                                                                                                                                                       |
| **                                                                                                    | 127480  | 06/17/03   | HRT             | Created new data sheet                                                                                                                                                                                                                                                                      |
| *A                                                                                                    | 131041  | 01/23/04   | CBD             | Change from Advance to Preliminary                                                                                                                                                                                                                                                          |
| *B                                                                                                    | 222180  | See ECN    | AJU             | Change from Preliminary to Final<br>Added 70 ns speed bin<br>Modified footnote #6 and #12<br>Removed MAX value for $V_{DR}$ on "Data Retention Characteristics" table<br>Modified input and output capacitance values<br>Added Pb-free ordering information<br>Removed 32-pin STSOP package |