CY7C455
CY7C456
CY7C457

512 x 18, 1K x 18, and 2K x 18 Cascadable Clocked FIFOs with Programmable Flags

Features

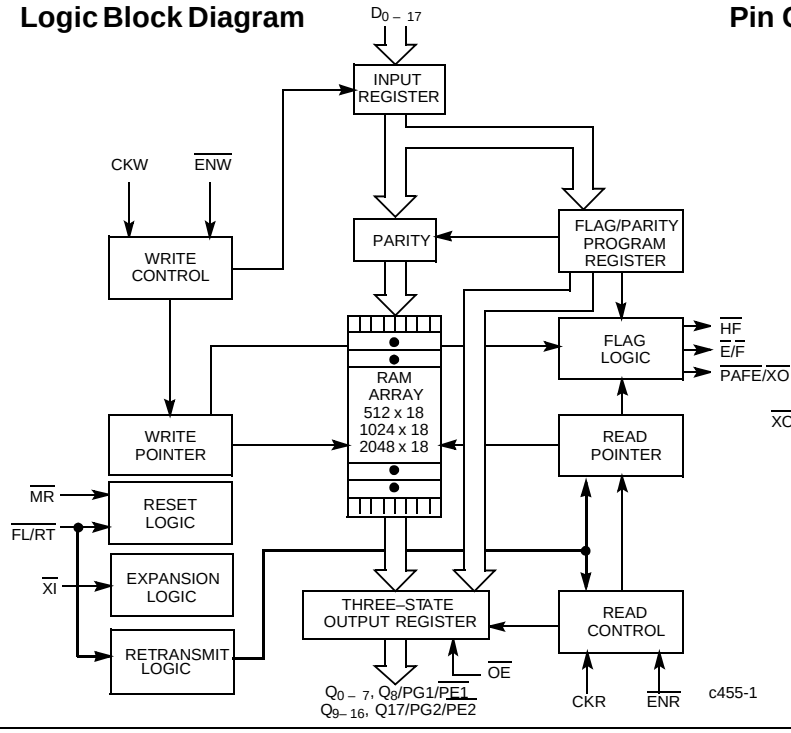
- **High-speed, low-power, first-in first-out (FIFO) memories**
- **512 x 18 (CY7C455)**
- **1,024 x 18 (CY7C456)**
- **2,048 x 18 (CY7C457)**
- **0.65 micron CMOS for optimum speed/power**
- **High-speed 83-MHz operation (12 ns read/write cycle time)**
- **Low power — I_{CC}=90 mA**
- **Fully asynchronous and simultaneous read and write operation**
- **Empty, Full, Half Full, and programmable Almost Empty and Almost Full status flags**
- **TTL compatible**
- **Retransmit function**
- **Parity generation/checking**
- **Output Enable (OE) pins**
- **Independent read and write enable pins**
- **Center power and ground pins for reduced noise**
- **Supports free-running 50% duty cycle clock inputs**
- **Width Expansion Capability**
- **Depth Expansion Capability**
- **52-pin PLCC and 52-pin PQFP**

Functional Description

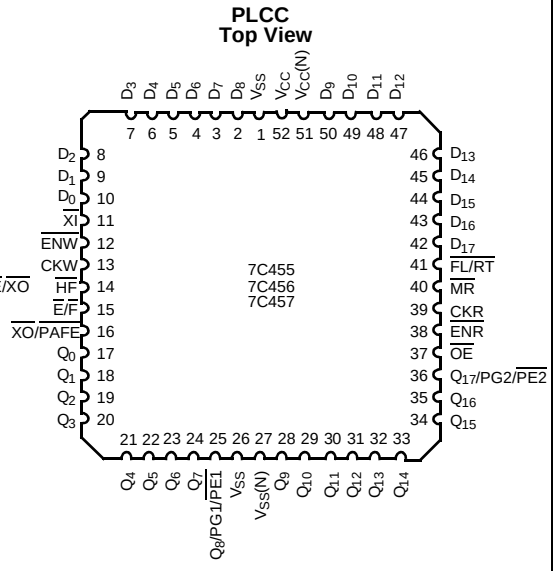
The CY7C455, CY7C456, and CY7C457 are high-speed, low-power, first-in first-out (FIFO) memories with clocked read and write interfaces. All are 18 bits wide. The CY7C455 has a 512-word memory array, the CY7C456 has a 1,024-word memory array, and the CY7C457 has a 2,048-word memory array. The CY7C455, CY7C456, and CY7C457 can be cascaded to increase FIFO depth. Programmable features include Almost Full/Empty flags and generation/checking of parity. These FIFOs provide solutions for a wide variety of data buffering needs, including high-speed data acquisition, multiprocessor interfaces, and communications buffering.

These FIFOs have 18-bit input and output ports that are controlled by separate clock and enable signals. The input port is controlled by a free-running clock (CKW) and a write enable pin ($\overline{ENW}$).

Logic Block Diagram

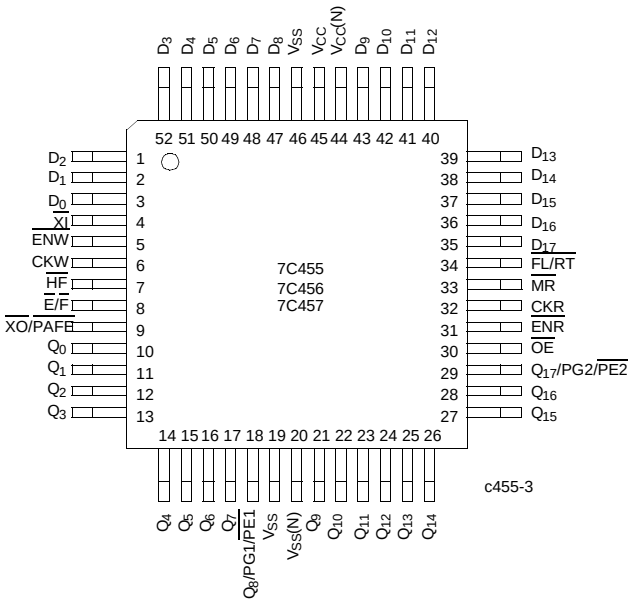


Pin Configurations



Pin Configurations (continued)

PQFP
Top View



Functional Description (continued)

In the standalone and width expansion configurations, a LOW on the retransmit ($\overline{RT}$) input causes the FIFOs to retransmit the data. Read enable ($\overline{ENR}$) and the write enable ($\overline{ENW}$) must both be HIGH during the retransmit, and then $\overline{ENR}$ is used to access the data.When $\overline{ENW}$ is asserted, data is written into the FIFO on the rising edge of the CKW signal. While $\overline{ENW}$ is held active, data is continually written into the FIFO on each CKW cycle. The output port is controlled in a similar manner by a free-running read clock (CKR) and a read enable pin ($\overline{ENR}$). In addition, the CY7C455, CY7C456, and CY7C457 have an output enable pin ($\overline{OE}$). The read (CKR) and write (CKW) clocks may be tied together for single-clock operation or the two clocks may be run independently for asynchronous read/write applications. Clock frequencies up to 83.3 MHz are achievable in the standalone configuration, and up to 83.3 MHz is achievable when FIFOs are cascaded for depth expansion.

Depth expansion is possible using the cascade input ($\overline{XI}$), cascade output ($\overline{XO}$), and First Load ($\overline{FL}$) pins. The $\overline{XO}$ pin is connected to the $\overline{XI}$ pin of the next device, and the $\overline{XO}$ pin of the last device should be connected to the $\overline{XI}$ pin of the first device. The $\overline{FL}$ pin of the first device is tied to V_{SS}.

The CY7C455, CY7C456, and CY7C457 provide three status pins. These pins are decoded to determine one of six states: Empty, Almost Empty, Less than or Equal to Half Full, Greater than Half Full, Almost Full, and Full (see *Table 1*). The Almost Empty/Full flag ($\overline{PAFE}$) shares the $\overline{XO}$ pin on the CY7C455, CY7C456, and CY7C457. This flag is valid in the standalone and width-expansion configurations. In the depth expansion, this pin provides the expansion out ($\overline{XO}$) information that is used to signal the next FIFO when it will be activated.

The flags are synchronous, i.e., they change state relative to either the read clock (CKR) or the write clock (CKW). When entering or exiting the Empty and Almost Empty states, the flags are updated exclusively by the CKR. The flags denoting Half Full, Almost Full, and Full states are updated exclusively by CKW. The synchronous flag architecture guarantees that the flags maintain their status for some minimum time. This time is typically equal to approximately one cycle time.

The CY7C455/6/7 uses center power and ground for reduced noise. All configurations are fabricated using an advanced 0.65u CMOS technology. Input ESD protection is greater than 2001V, and latch-up is prevented by the use of guard rings.

Selection Guide

		7C455/6/7–12	7C455/6/7–14	7C455/6/7–20	7C455/6/7–30
Maximum Frequency (MHz)		83.3	71.4	50	33.3
Maximum Cascadable Frequency		83.3	71.4	50	33.3
Maximum Access Time (ns)		9	10	15	20
Minimum Cycle Time (ns)		12	14	20	30
Minimum Clock HIGH Time (ns)		5	6.5	9	12
Minimum Clock LOW Time (ns)		5	6.5	9	12
Minimum Data or Enable Set-Up (ns)		4	5	6	7
Minimum Data or Enable Hold (ns)		0	0	0	0
Maximum Flag Delay (ns)		9	10	15	20
Maximum Current (mA)	Commercial	160	160	140	120
	Industrial	180	180	160	140

Selection Guide (continued)

	CY7C455	CY7C456	CY7C457
Density	512 x 18	1,024 x 18	2,048 x 18
$\overline{OE}$, Depth Cascadable	Yes	Yes	Yes
Package	52-Pin PLCC/PQFP	52-Pin PLCC/PQFP	52-Pin PLCC/PQFP

Maximum Ratings[1]

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature .....–65°C to +150°C

Ambient Temperature with Power Applied.....–55°C to +125°C

Supply Voltage to Ground Potential..... –0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State ..... –0.5V to +7.0V

DC Input Voltage..... –3.0V to +7.0V

Output Current into Outputs (LOW) .....20 mA

Static Discharge Voltage..... >2001V (per MIL-STD-883, Method 3015)

Latch-Up Current..... >200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ± 10%
Industrial[2]	–40°C to +85°C	5V ± 10%

Notes:
1. The Voltage on any input or I/O pin cannot exceed the power pin during power-up.
2. T_A is the “instant on” case temperature.

Pin Definitions

Signal Name	I/O	Description
D_{0-17}	I	Data Inputs: When the FIFO is not full and $\overline{ENW}$ is active, CKW (rising edge) writes data (D_{0-17}) into the FIFO's memory. If $\overline{MR}$ is asserted at the rising edge of CKW, data is written into the FIFO's programming register. $D_{8,17}$ are ignored if the device is configured for parity generation.
Q_{0-7} Q_{9-16}	O	Data Outputs: When the FIFO is not empty and $\overline{ENR}$ is active, CKR (rising edge) reads data (Q_{0-7}, Q_{9-16}) out of the FIFO's memory. If $\overline{MR}$ is active at the rising edge of CKR, data is read from the programming register.
Q_8/PG1/$\overline{PE1}$ Q_{17}/PG2/$\overline{PE2}$	O	Function varies according to mode: Parity disabled – same function as Q_{0-7} and Q_{9-16} Parity enabled, generation – parity generation bit (PG_x) Parity enabled, check – Parity Error Flag ($\overline{PE_x}$)
$\overline{ENW}$	I	Enable Write: Enables the CKW input (for both non-program and program modes).
$\overline{ENR}$	I	Enable Read: Enables the CKR input (for both non-program and program modes).
CKW	I	Write Clock: The rising edge clocks data into the FIFO when $\overline{ENW}$ is LOW; updates Half Full, Almost Full, and Full flag states. When $\overline{MR}$ is asserted, CKW writes data into the program register.
CKR	I	Read Clock: The rising edge clocks data out of the FIFO when $\overline{ENR}$ is LOW; updates the Empty and Almost Empty flag states. When $\overline{MR}$ is asserted, CKR reads data out of the program register.
$\overline{HF}$	O	Half Full Flag: Synchronized to CKW.
$\overline{E}$/$\overline{F}$	O	Empty or Full Flag: $\overline{E}$ is synchronized to CKR; $\overline{F}$ is synchronized to CKW.
$\overline{PAFE}$/$\overline{XO}$	O	Dual-Mode Pin: Not Cascaded – programmable Almost Full is synchronized to CKW; Programmable Almost Empty is synchronized to CKR. Cascaded – expansion out signal, connected to $\overline{XI}$ of next device.
$\overline{XI}$	I	Expansion-In Pin: Not Cascaded – $\overline{XI}$ is tied to V_{SS}. Cascaded – expansion Input, connected to $\overline{XO}$ of previous device.
$\overline{FL}$/$\overline{RT}$	I	First Load/Retransmit Pin: Cascaded – the first device in the daisy chain will have $\overline{FL}$ tied to V_{SS}; all other devices will have $\overline{FL}$ tied to V_{CC} (*Figure 1*). Not Cascaded – tied to V_{CC}. Retransmit function is also available in standalone mode by strobing $\overline{RT}$.
$\overline{MR}$	I	Master Reset: Resets device to empty condition. Non-Programming Mode: Program register is reset to default condition of no parity and $\overline{PAFE}$ active at 16 or less locations from Full/Empty. Programming Mode: Data present on $D_{0-9,10, \text{ or } 11}$ and D_{15-17} is written into the programmable register on the rising edge of CKW. Program register contents appear on $Q_{0-9,10, \text{ or } 11}$ and Q_{15-17} after the rising edge of CKR.
$\overline{OE}$	I	Output Enable for Q_{0-7}, Q_{9-16}, Q_8/PG1/$\overline{PE1}$ and Q_{17}/PG2/$\overline{PE2}$ pins.

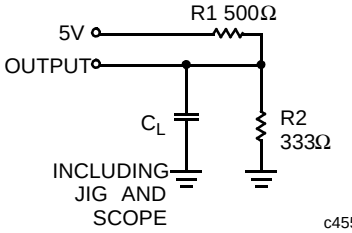
Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions		7C455/6/7–12 Min.	7C455/6/7–12 Max	7C455/6/7–14 Min.	7C455/6/7–14 Max	7C455/6/7–20 Min.	7C455/6/7–20 Max	7C455/6/7–30 Min.	7C455/6/7–30 Max	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = –2.0 mA		2.4		2.4		2.4		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8.0 mA			0.4		0.4		0.4		0.4	V
V_{IH}[3]	Input HIGH Voltage			2.2	V_{CC}	2.2	V_{CC}	2.2	V_{CC}	2.2	V_{CC}	V
V_{IL}[3]	Input LOW Voltage			–0.5	0.8	–0.5	0.8	–0.5	0.8	–0.5	0.8	V
I_{IX}	Input Leakage Current	V_{CC} = Max.		–10	+10	–10	+10	–10	+10	–10	+10	µA
I_{OS}[4]	Output Short Circuit Current	V_{CC} = Max., V_{OUT} = GND		–90		–90		–90		–90		mA
I_{OZL} I_{OZH}	Output OFF, High Z Current	$\overline{OE} \geq V_{IH}$, $V_{SS} < V_O < V_{CC}$		–10	+10	–10	+10	–10	+10	–10	+10	µA
I_{CC1}[5]	Operating Current	V_{CC} = Max., I_{OUT} = 0 mA	Com'l		160		160		140		120	mA
			Ind		180		180		160		140	mA
I_{CC2}[6]	Operating Current	V_{CC} = Max., I_{OUT} = 0 mA	Com'l		90		90		90		90	mA
			Ind		100		100		100		100	mA
I_{SB}[7]	Standby Current	V_{CC} = Max., I_{OUT} = 0 mA	Com'l		40		40		40		40	mA
			Ind		40		40		40		40	mA

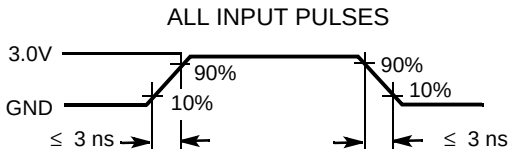
Capacitance[8]

Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	10	pF
C_{OUT}	Output Capacitance		12	pF

AC Test Loads and Waveforms[9, 10, 11, 12, 13]

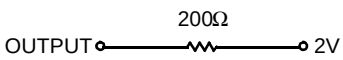


c455-4



c455-5

Equivalent to: THÉVENIN EQUIVALENT



Notes:

3. The V_{IH} and V_{IL} specifications apply for all inputs except $\overline{XI}$. The $\overline{XI}$ pin is not a TTL input. It is connected to either $\overline{XO}$ of the previous device or V_{SS}.
4. Test no more than one output at a time for not more than one second.
5. Input signals switch from 0V to 3V with a rise/fall time of less than 3 ns, clocks and clock enables switch at maximum frequency (f_{MAX}), while data inputs switch at $f_{MAX}/2$. Outputs are unloaded.
6. Input signals switch from 0V to 3V with a rise/fall time less than 3 ns, clocks and clock enables switch at 20 MHz, while the data inputs switch at 10 MHz. Outputs are unloaded.
7. All input signals are connected to V_{CC}. All outputs are unloaded. Read and write clocks switch at maximum frequency (f_{MAX}).
8. Tested initially and after any design or process changes that may affect these parameters.
9. C_L = 30 pF for all AC parameters except for t_{OHZ}.
10. C_L = 5 pF for t_{OHZ}.
11. All AC measurements are referenced to 1.5V except t_{OE}, t_{OLZ}, and t_{OHZ}.
12. t_{OE} and t_{OLZ} are measured at ± 100 mV from the steady state.
13. t_{OHZ} is measured at +500 mV from V_{OL} and – 500 mV from V_{OH}.

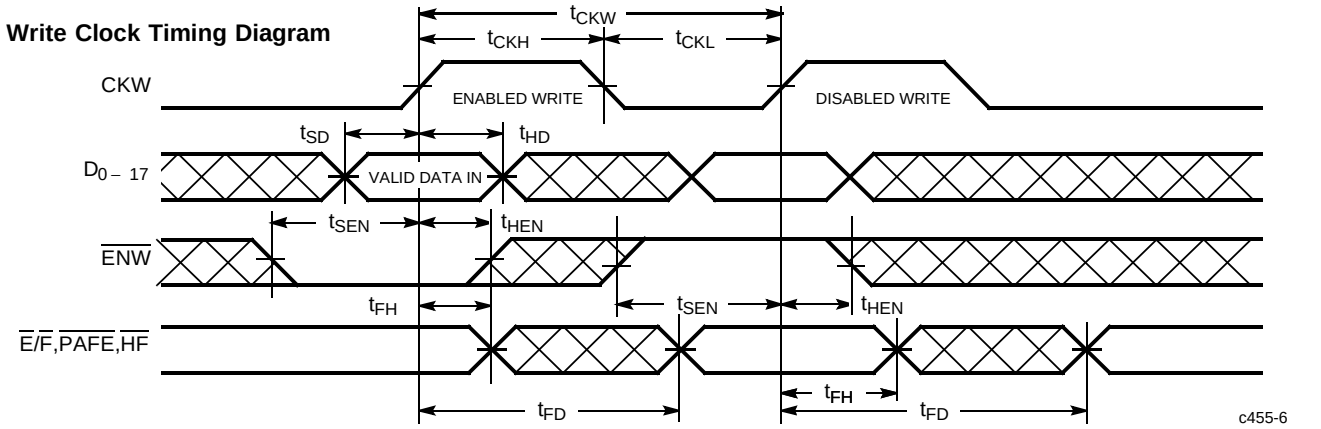
Switching Characteristics Over the Operating Range[14]

Parameter	Description	7C455/6/7–12		7C455/6/7–14		7C455/6/7–20		7C455/6/7–30		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{CKW}	Write Clock Cycle	12		14		20		30		ns
t_{CKR}	Read Clock Cycle	12		14		20		30		ns
t_{CKH}	Clock HIGH	5		6.5		9		12		ns
t_{CKL}	Clock LOW	5		6.5		9		12		ns
t_A	Data Access Time		9		10		15		20	ns
t_{OH}	Previous Output Data Hold After Read HIGH	0		0		0		0		ns
t_{FH}	Previous Flag Hold After Read/Write HIGH	0		0		0		0		ns
t_{SD}	Data Set-Up	4		5		6		7		ns
t_{HD}	Data Hold	0		0		0		0		ns
t_{SEN}	Enable Set-Up	4		5		6		7		ns
t_{HEN}	Enable Hold	0		0		0		0		ns
t_{OE}	$\overline{OE}$ LOW to Output Data Valid		9		10		15		20	ns
t_{OLZ}[8, 15]	$\overline{OE}$ LOW to Output Data in Low Z	0		0		0		0		ns
t_{OHZ}[8, 15]	$\overline{OE}$ HIGH to Output Data in High Z		9		10		15		20	ns
t_{PG}	Read HIGH to Parity Generation		9		10		15		20	ns
t_{PE}	Read HIGH to Parity Error Flag		9		10		15		20	ns
t_{FD}	Flag Delay		9		10		15		20	ns
t_{SKEW1}[16]	Opposite Clock After Clock	0		0		0		0		ns
t_{SKEW2}[17]	Opposite Clock Before Clock	12		14		20		30		ns
t_{PMR}	Master Reset Pulse Width ($\overline{MR}$ LOW)	14		14		20		30		ns
t_{SCMR}	Last Valid Clock LOW Set-Up to $\overline{MR}$ LOW	0		0		0		0		ns
t_{OHMR}	Data Hold From $\overline{MR}$ LOW	0		0		0		0		ns
t_{MRR}	Master Reset Recovery ($\overline{MR}$ HIGH Set-Up to First Enabled Write/Read)	12		14		20		30		ns
t_{MRF}	$\overline{MR}$ HIGH to Flags Valid		12		14		20		30	ns
t_{AMR}	$\overline{MR}$ HIGH to Data Outputs LOW		12		14		20		30	ns
t_{SMRP}	Program Mode—$\overline{MR}$ LOW Set-Up	12		14		20		30		ns
t_{HMRP}	Program Mode—$\overline{MR}$ LOW Hold	9		10		15		20		ns
t_{FTP}	Program Mode—Write HIGH to Read HIGH	12		14		20		30		ns
t_{AP}	Program Mode—Data Access Time		12		14		20		30	ns
t_{OHP}	Program Mode—Data Hold Time from $\overline{MR}$ HIGH	0		0		0		0		ns
t_{PRT}	Retransmit Pulse Width	12		14		20		30		ns
t_{RTR}	Retransmit Recovery Time	12		14		20		30		ns

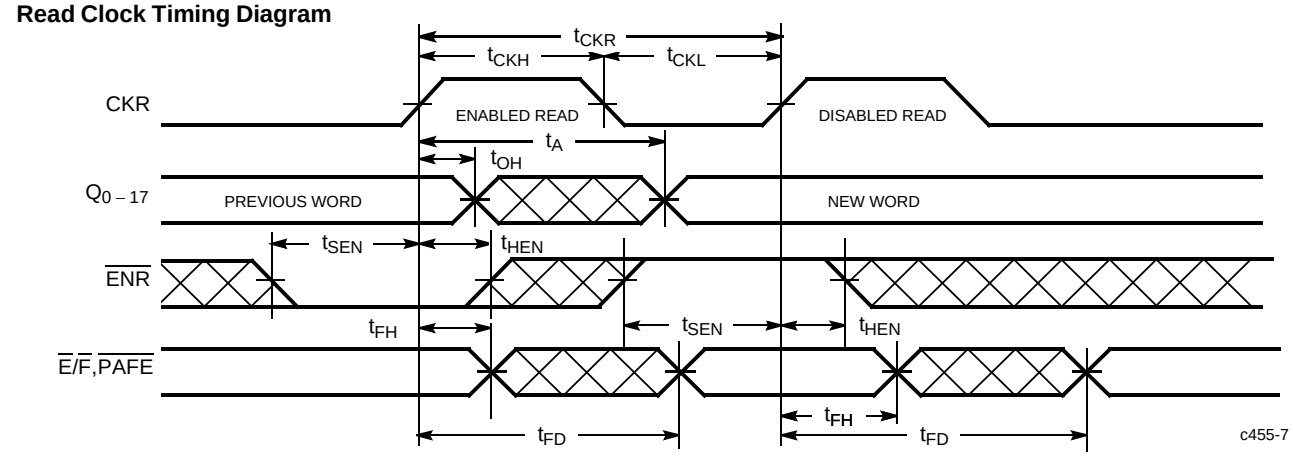
14. Test conditions assume signal transition time of 3 ns or less, timing reference levels of 1.5V, and output loading as shown in AC Test Loads and Waveforms and capacitance as in notes 9 and 10, unless otherwise specified.
15. At any given temperature and voltage condition, t_{OLZ} is greater than t_{OHZ} for any given device.
16. t_{SKEW1} is the minimum time an opposite clock can occur after a clock and still be guaranteed not to be included in the current clock cycle (for purposes of flag update). If the opposite clock occurs less than t_{SKEW1} after the clock, the decision of whether or not to include the opposite clock in the current clock cycle is arbitrary. *Note*: The opposite clock is the signal to which a flag is not synchronized; i.e., CKW is the opposite clock for Empty and Almost Empty flags, CKR is the opposite clock for the Almost Full, Half Full, and Full flags. The clock is the signal to which a flag is synchronized; i.e., CKW is the clock for the Half Full, Almost Full, and Full flags, CKR is the clock for Empty and Almost Empty flags.
17. t_{SKEW2} is the minimum time an opposite clock can occur before a clock and still be guaranteed to be included in the current clock cycle (for purposes of flag update). If the opposite clock occurs less than t_{SKEW2} before the clock, the decision of whether or not to include the opposite clock in the current clock cycle is arbitrary. See Note 16 for definition of clock and opposite clock.

Switching Waveforms

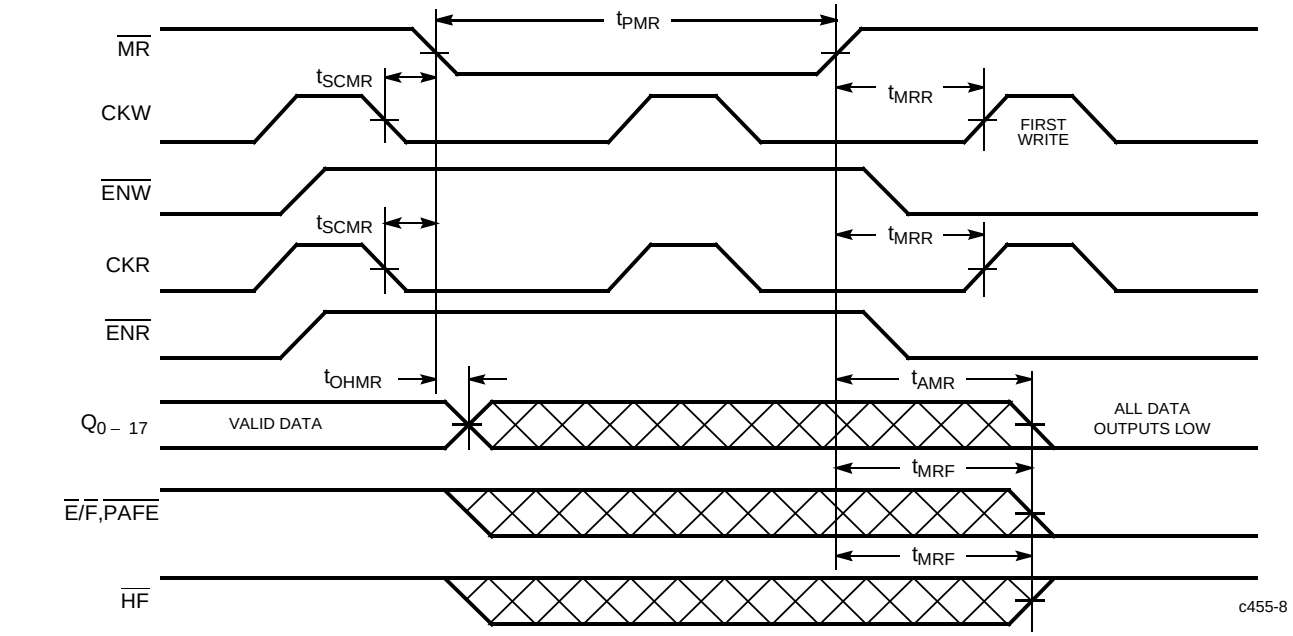
Write Clock Timing Diagram



Read Clock Timing Diagram



MasterReset (Default with Free-Running Clocks) Timing Diagram[18, 19, 20, 21]

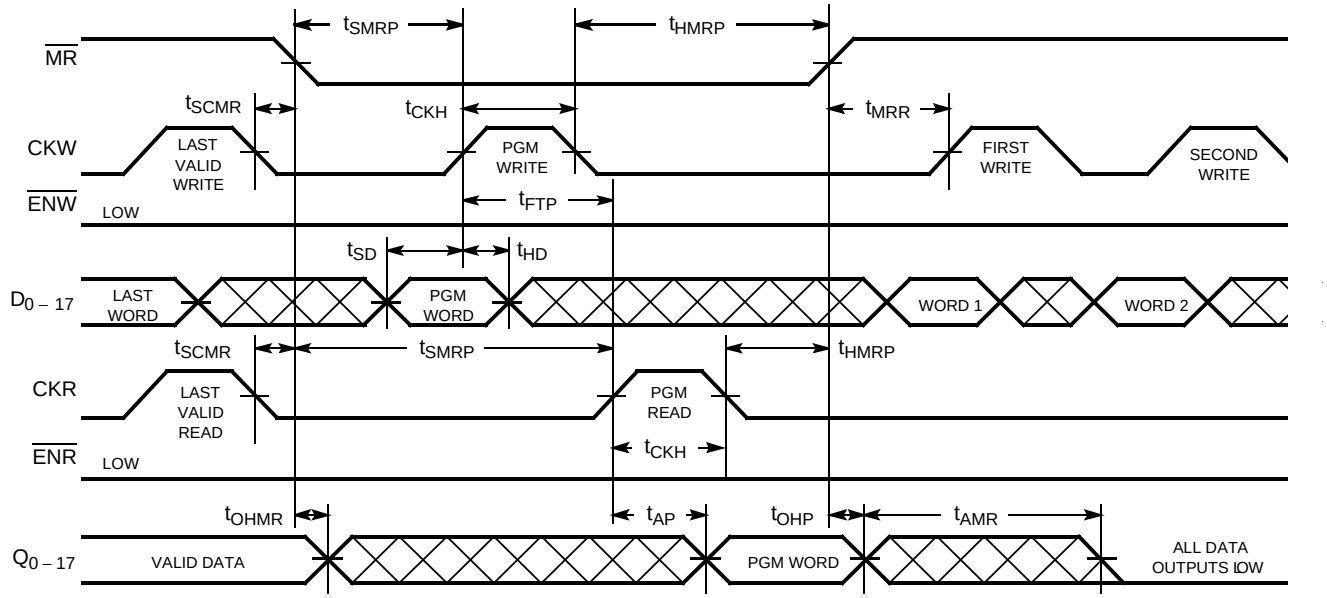


Notes:

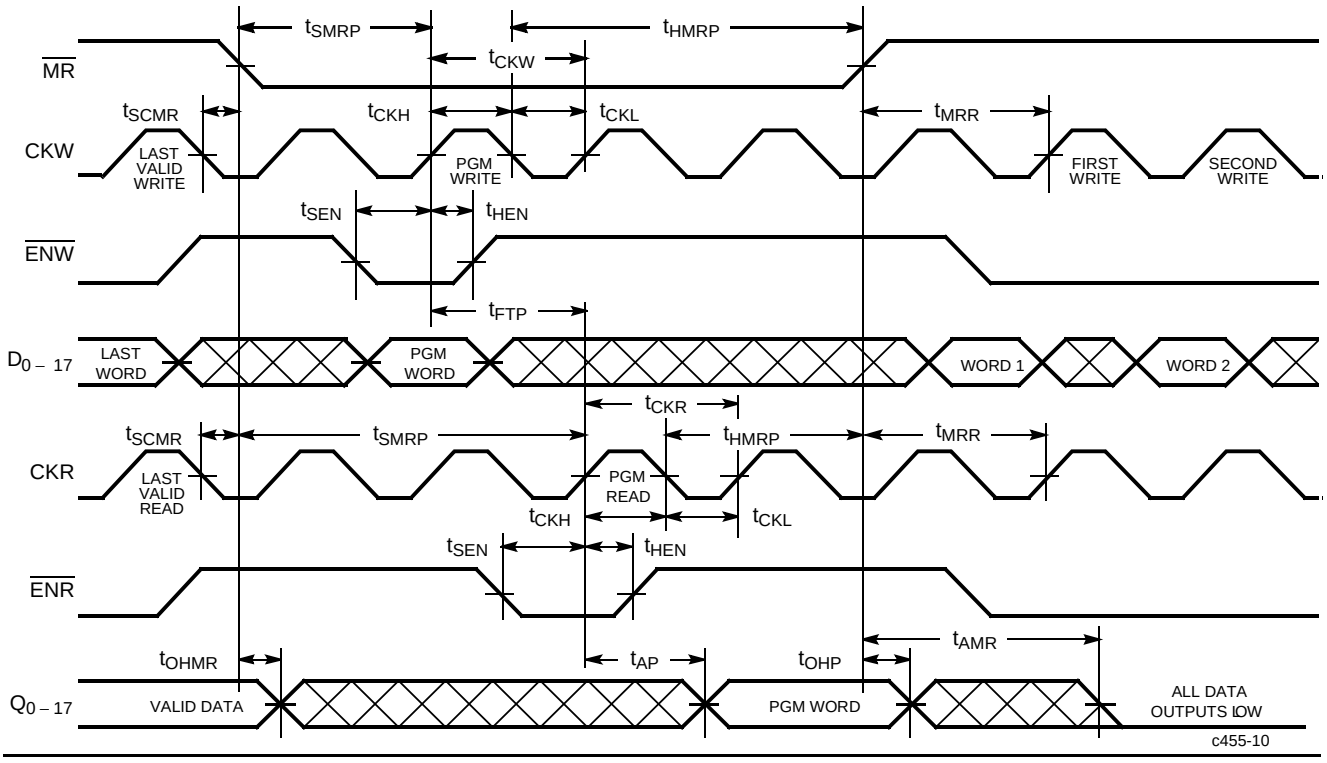
18. To only perform reset (no programming), the following criteria must be met: $\overline{ENW}$ or CKW must be inactive while $\overline{MR}$ is LOW.
19. To only perform reset (no programming), the following criteria must be met: ENR or CKR must be inactive while $\overline{MR}$ is LOW.
20. All data outputs (Q_{0-17}) go LOW as a result of the rising edge of $\overline{MR}$ after t_{AMR}.
21. In this example, Q_{0-17} will remain valid until t_{OHMR} if either the first read shown did not occur or if the read occurred soon enough such that the valid data was caused by it.

Switching Waveforms (continued)

Master Reset (Programming Mode) Timing Diagram[20, 21]

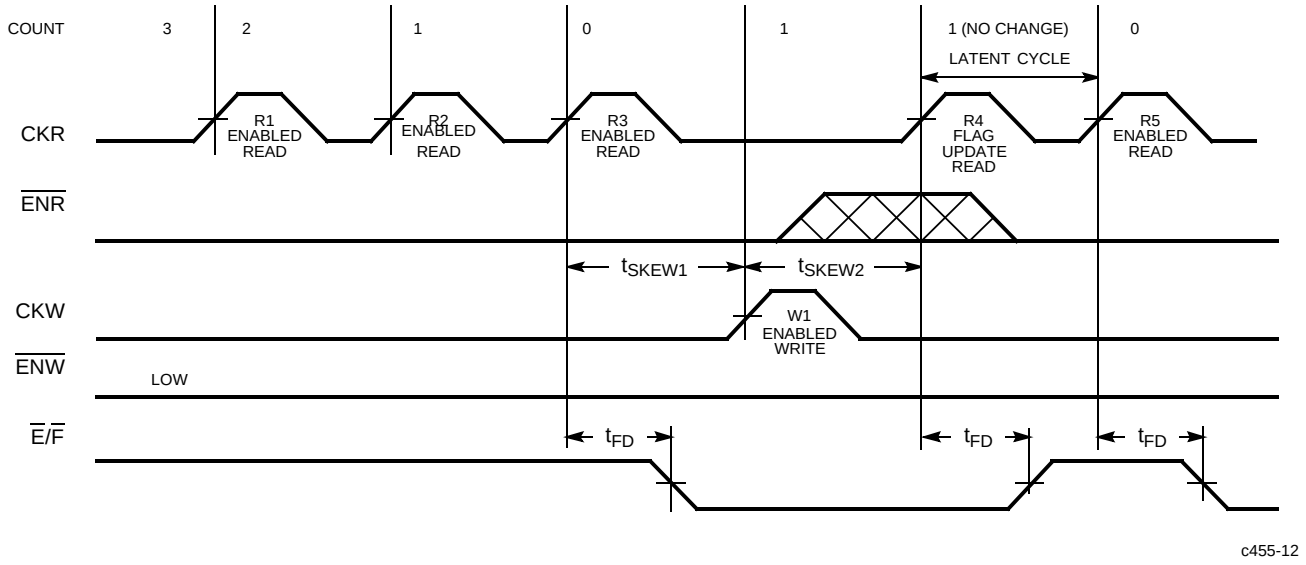


Master Reset (Programming Mode with Free-Running Clocks) Timing Diagram[20, 21]



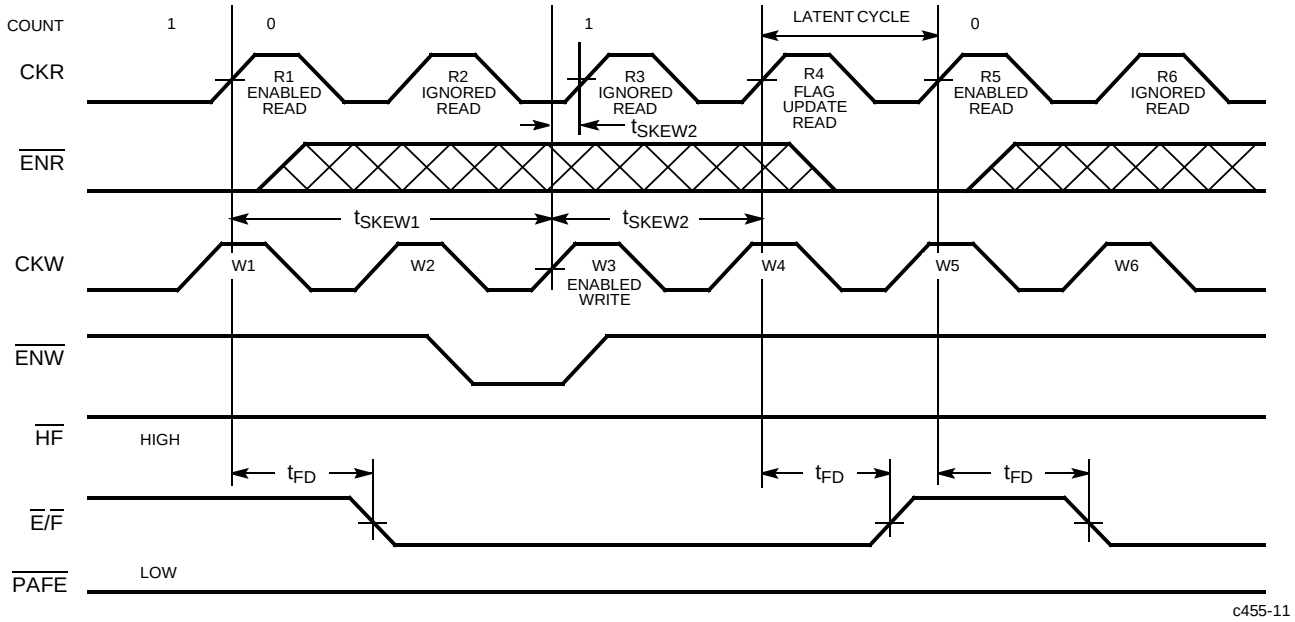
Switching Waveforms (continued)

Read to Empty Timing Diagram[22, 25, 26]



c455-12

Read to Empty Timing Diagram with Free-Running Clocks[22, 23, 24, 25]



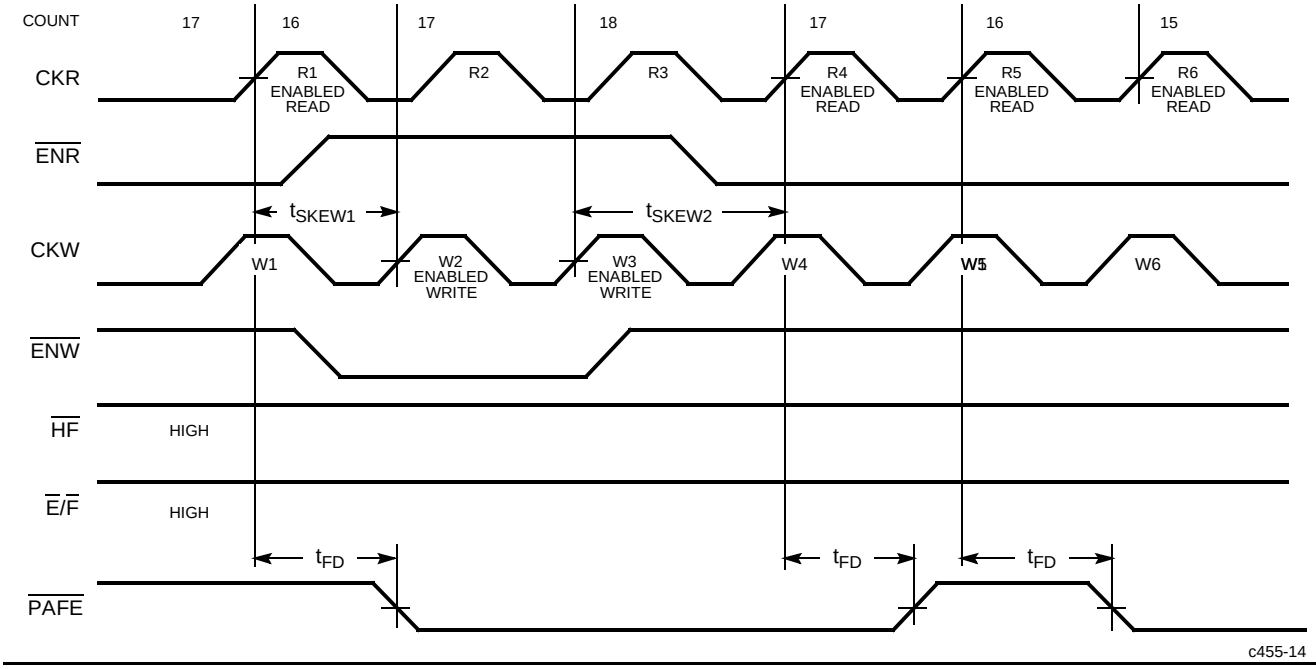
c455-11

Notes:

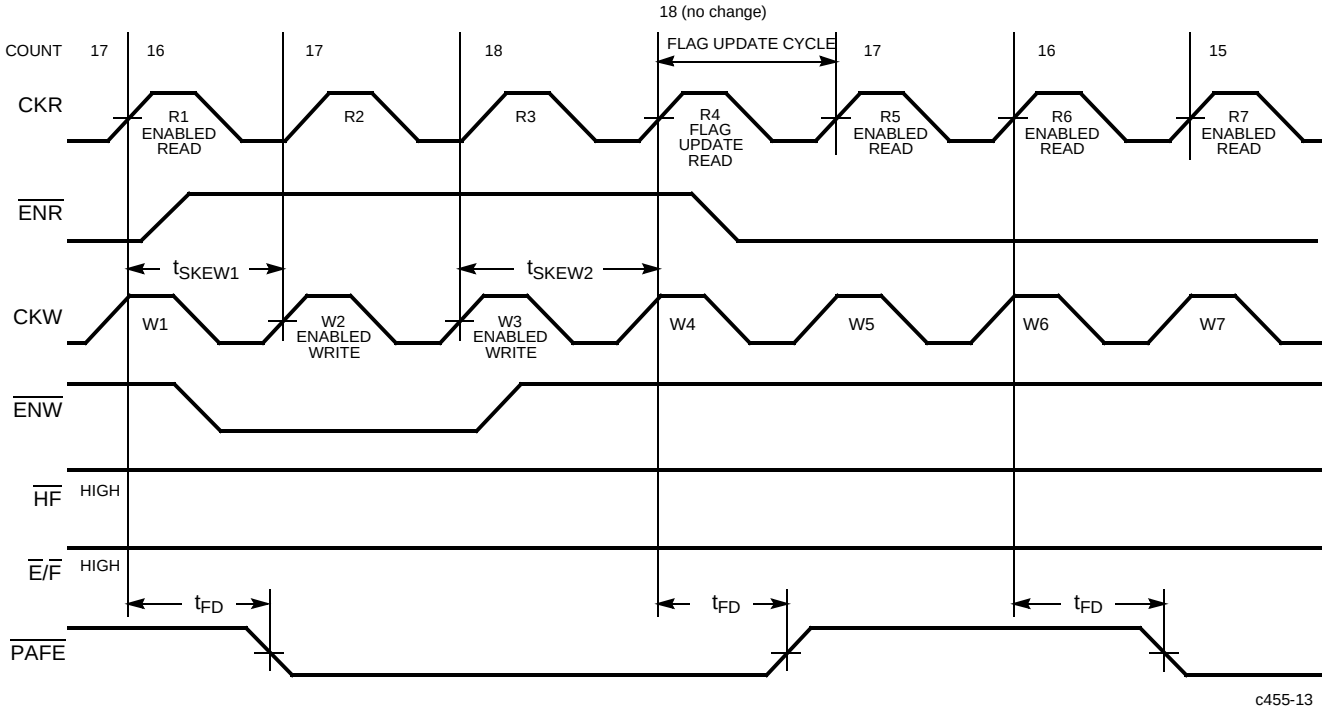
22. "Count" is the number of words in the FIFO.
23. The FIFO is assumed to be programmed with P>0 (i.e., $\overline{PAFE}$ does not transition at Empty or Full).
24. R2 is ignored because the FIFO is empty (count = 0). It is important to note that R3 is also ignored because W3, the first enabled write after empty, occurs less than t_{SKEW2} before R3. Therefore, the FIFO still appears empty when R3 occurs. Because W3 occurs greater than t_{SKEW2} before R4, R4 includes W3 in the flag update.
25. CKR is clock and CKW is opposite clock.
26. R3 updates the flag to the Empty state by asserting $\overline{E}/\overline{F}$. Because W1 occurs greater than t_{SKEW1} after R3, R3 does not recognize W1 when updating flag status. But because W1 occurs t_{SKEW2} before R4, R4 includes W1 in the flag update and, therefore, updates FIFO to Almost Empty state. It is important to note that R4 is a latent cycle; i.e., it only updates the flag status regardless of the state of $\overline{ENR}$. It does not change the count or the FIFO's data outputs.

Switching Waveforms (continued)

Read to Almost Empty Timing Diagram with Free-Running Clocks[22, 25, 27]



Read to Almost Empty Timing Diagram with Read Flag Update Cycle with Free-Running Clocks [22, 25, 27, 28, 29]

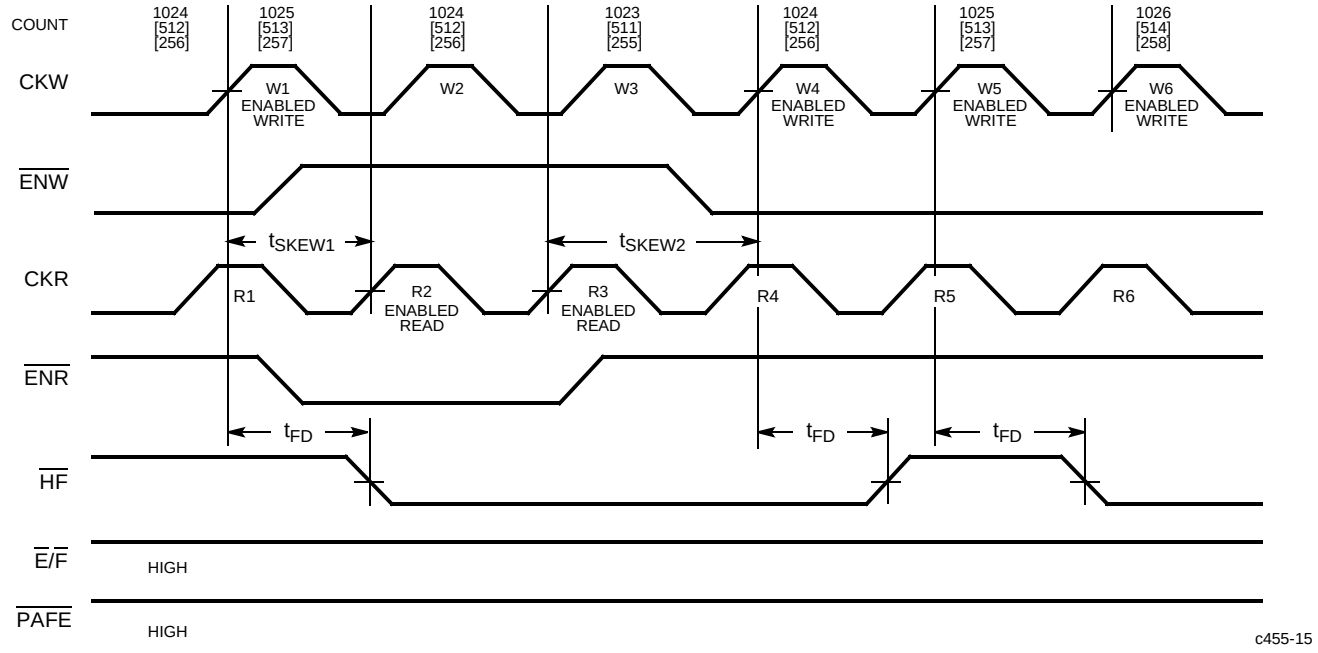


Notes:

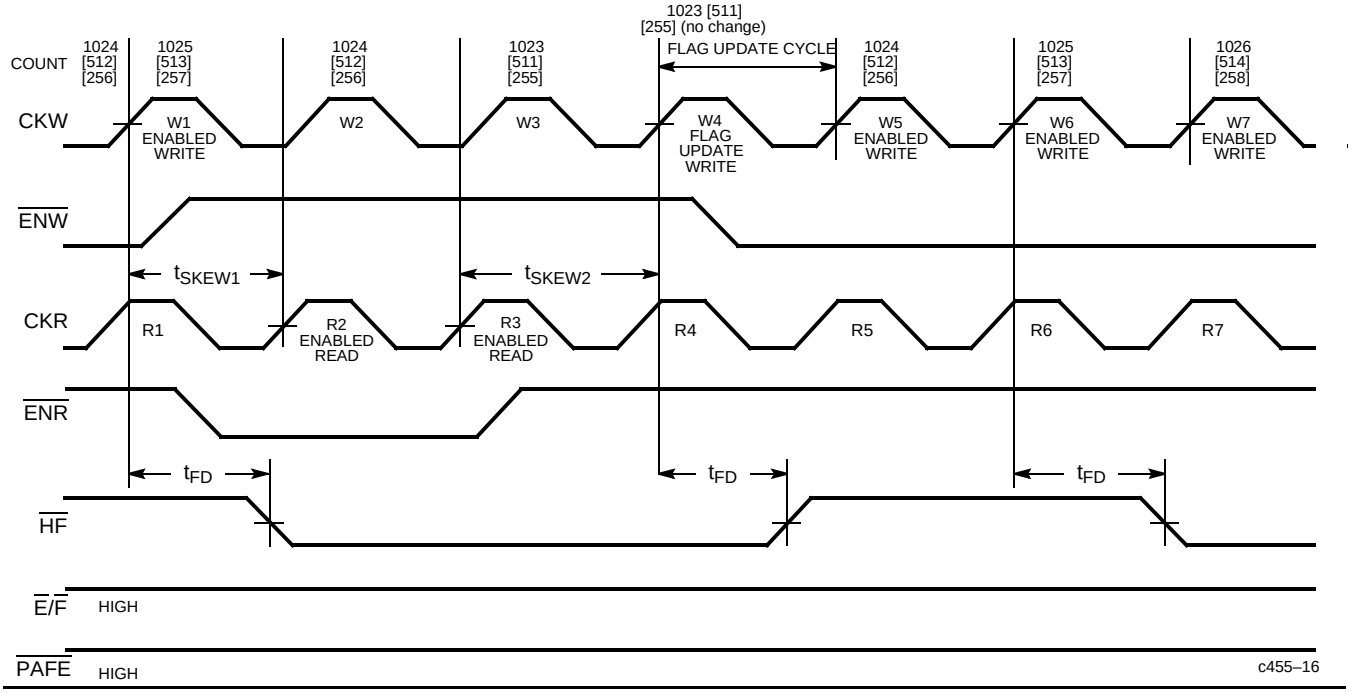
27. The FIFO in this example is assumed to be programmed to its default flag values. Almost Empty is 16 words from Empty; Almost Full is 16 locations from Full.
28. R4 only updates the flag status. It does not affect the count because ENR is HIGH.
29. When making the transition from Almost Empty to Intermediate, the count must increase by two (16 Á18; two enabled writes: W2, W3) before a read (R4) can update flags to the Less Than Half Full state.

Switching Waveforms (continued)

Write to Half Full Timing Diagram with Free-Running Clocks[22, 30, 31, 32]



Write to Half Full Timing Diagram with Write Flag Update Cycle with Free-Running Clocks[22, 30, 31, 32, 33, 34]

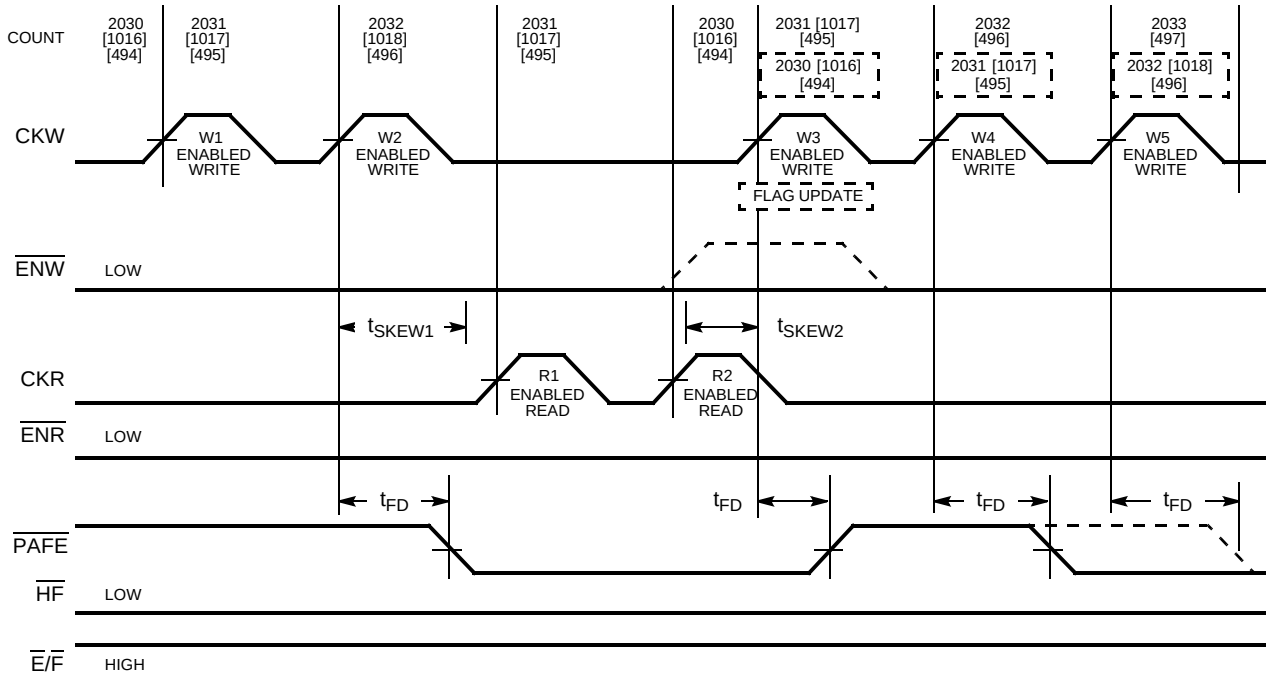


Notes:

30. CKW is clock and CKR is opposite clock.
31. Count = 1,025 indicates Half Full for the CY7C446 and CY7C456. Count = 513 indicates Half Full for the CY7C447 and CY7C457. Count = 257 indicates Half Full for the CY7C448 and CY7C458.
32. When the FIFO contains 1,024 [512] [256] words, the rising edge of the next enabled write causes the $\overline{HF}$ to be true (LOW).
33. The HF write flag update cycle does not affect the count because $\overline{ENW}$ is HIGH. It only updates $\overline{HF}$ to HIGH.
34. When making the transition from Half Full to Less Than Half Full, the count must decrease by two (i.e., 1,025 Á1,023; two enabled reads: R2 and R3) before a write (W4) can update flags to less than Half Full.

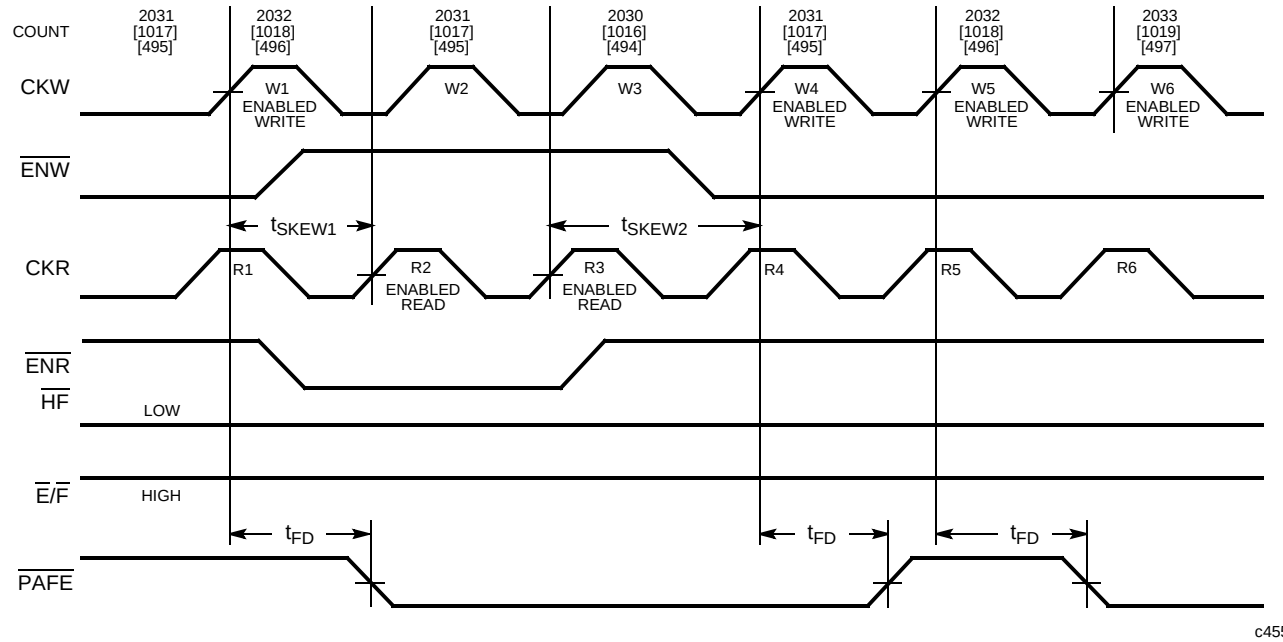
Switching Waveforms (continued)

Write to Almost Full Timing Diagram [22, 27, 30, 35, 36]



c455-18

Write to Almost Full Timing Diagram with Free-Running Clocks [22, 27, 30]



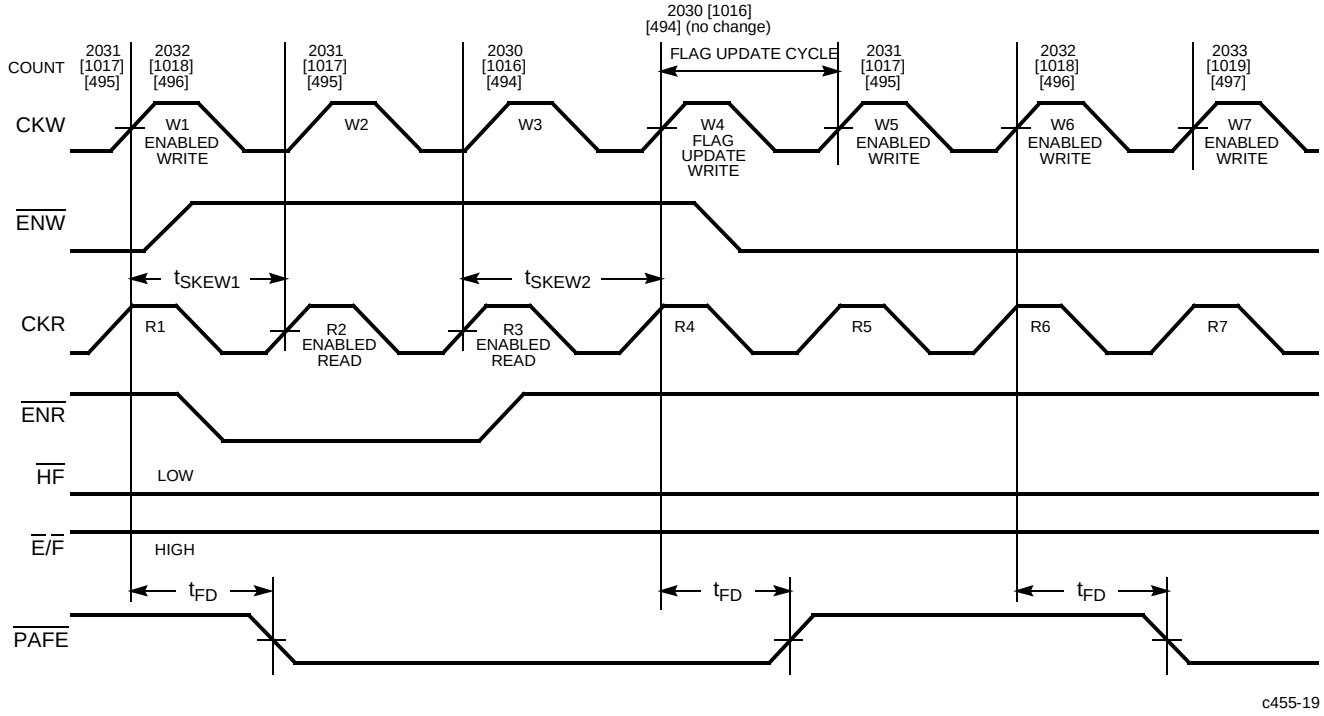
c455-17

Notes:

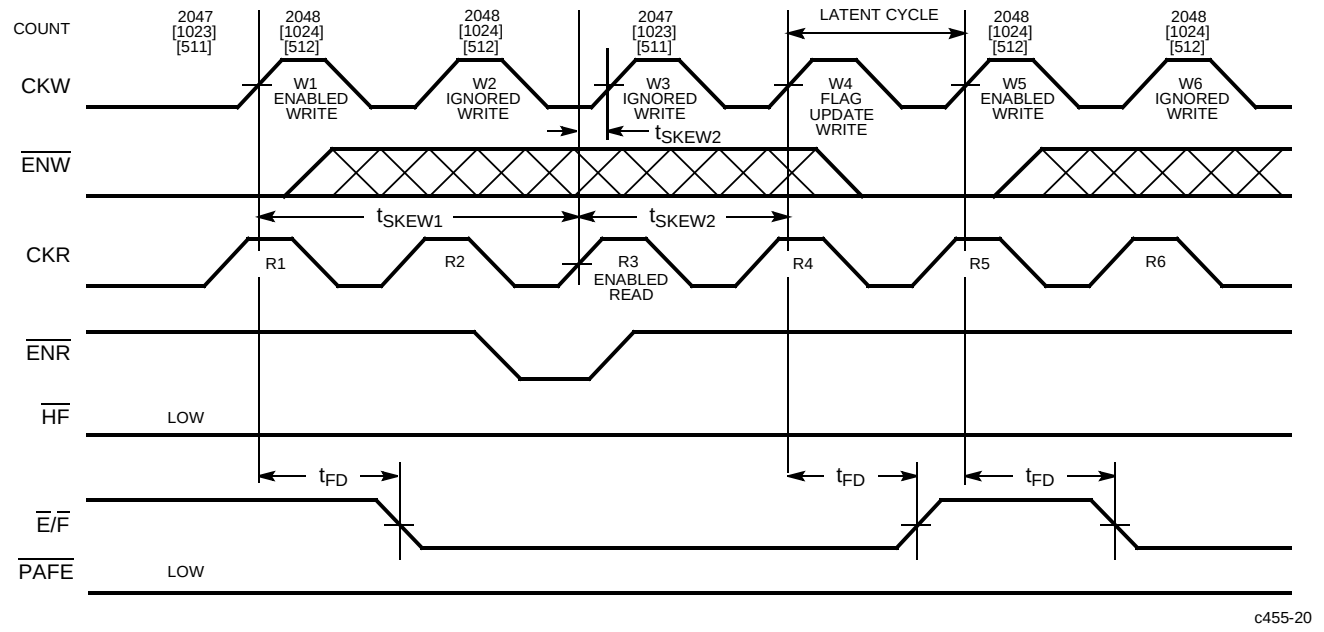
35. W2 updates the flag to the Almost Full state by asserting $\overline{\text{PAFE}}$. Because R1 occurs greater than t_{SKEW1} after W2, W2 does not recognize R1 when updating flag status. W3 includes R2 in the flag update because R2 occurs greater than t_{SKEW2} before W3. Note that W3 does not have to be enabled to update flags.
36. The dashed lines show W3 as a flag update write rather than an enabled write because $\overline{\text{ENW}}$ is HIGH.

Switching Waveforms (continued)

Write to Almost Full Timing Diagram with Write Flag Update Cycle and Free-Running Clocks[22, 27, 30]



Write to Full Flag Timing Diagram with Free-Running Clocks[22, 30, 37]

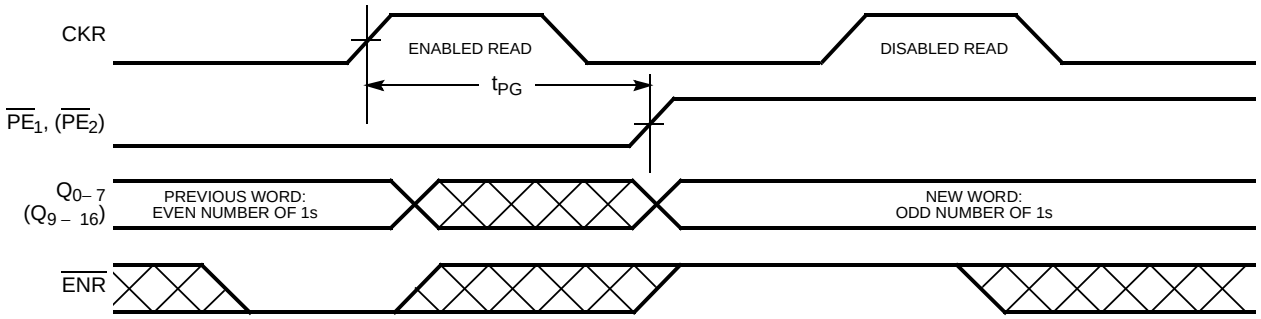


Note:

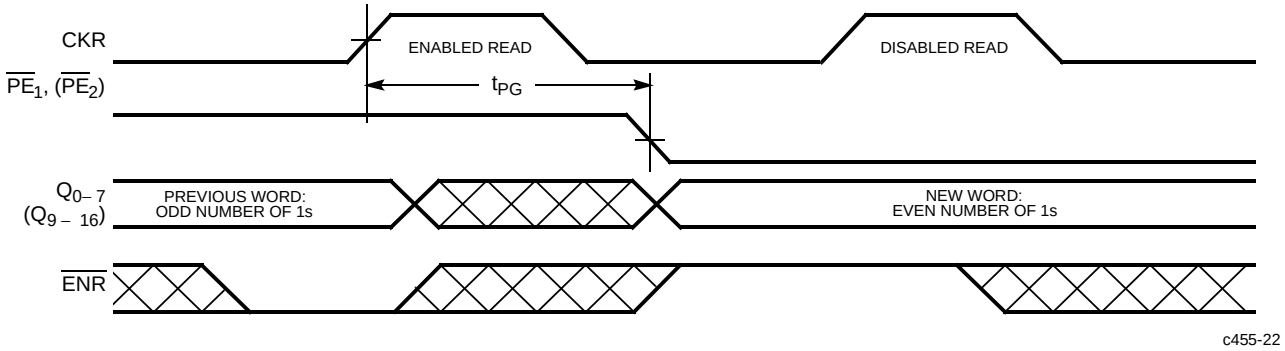
37. W2 is ignored because the FIFO is full (count = 2,048 [1,024] [512]). It is important to note that W3 is also ignored because R3, the first enabled read after full, occurs less than t_{SKEW2} before W3. Therefore, the FIFO still appears full when W3 occurs. Because R3 occurs greater than t_{SKEW2} before W4, W4 includes R3 in the flag update.

Switching Waveforms (continued)

Even Parity Generation Timing Diagram [38, 39]



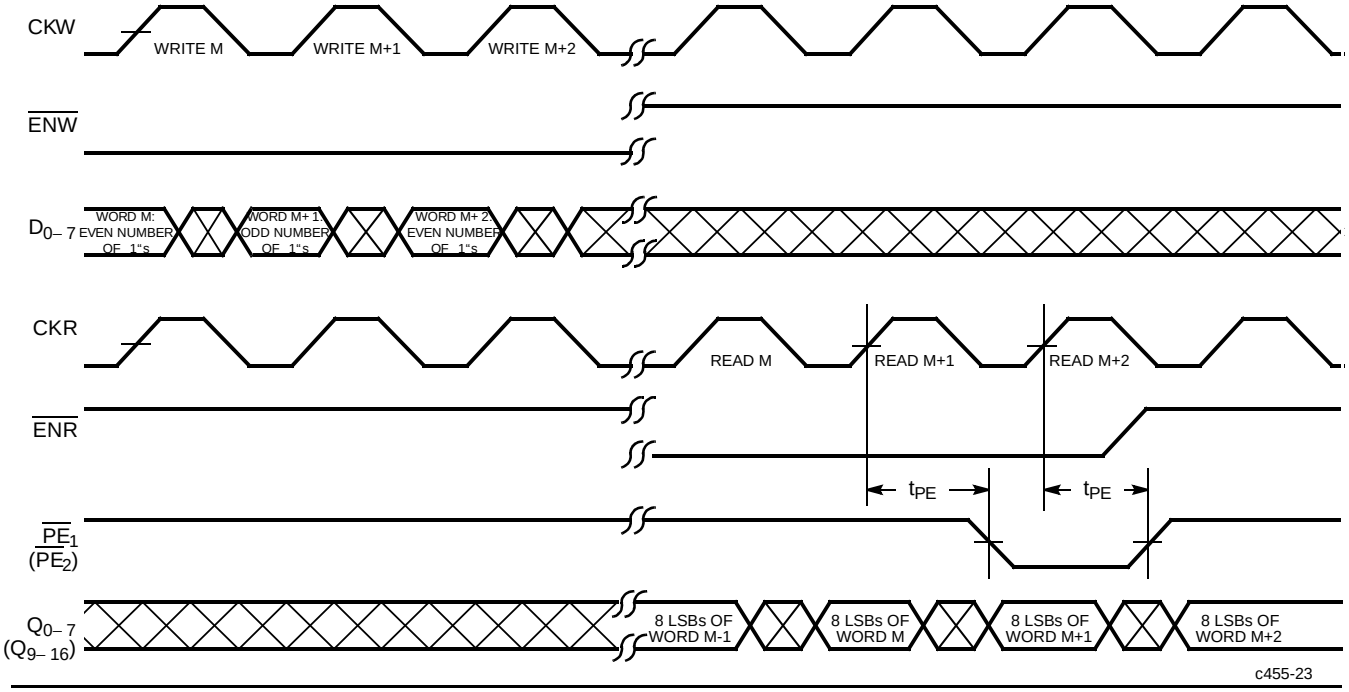
Even Parity Generation Timing Diagram [38, 40]



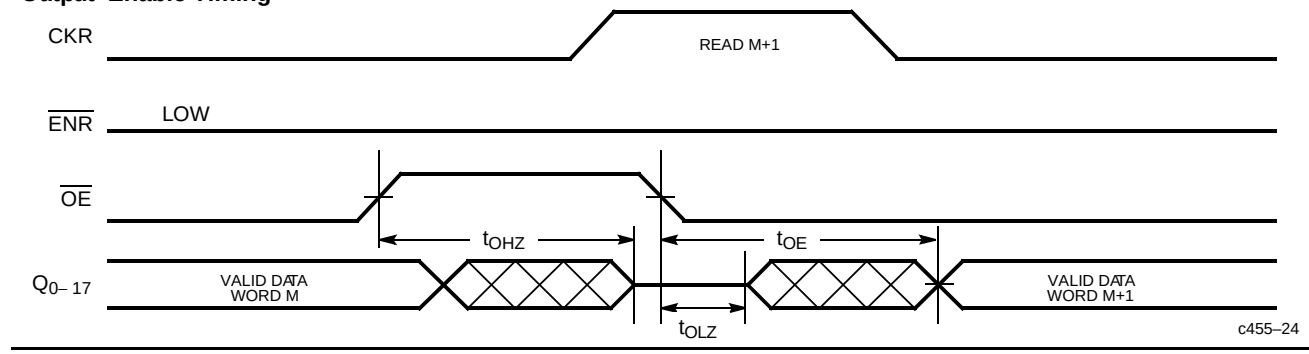
Notes:
38. In this example, the FIFO is assumed to be programmed to generate even parity. The Q_{0-7} word is shown. The example is similar for the Q_{9-16} word.
39. If Q_{0-7} "new word" also has an even number of 1s, then PG1 stays LOW.
40. If Q_{0-7} "new word" also has odd number of 1s, then PG1 stays HIGH.

Switching Waveforms (continued)

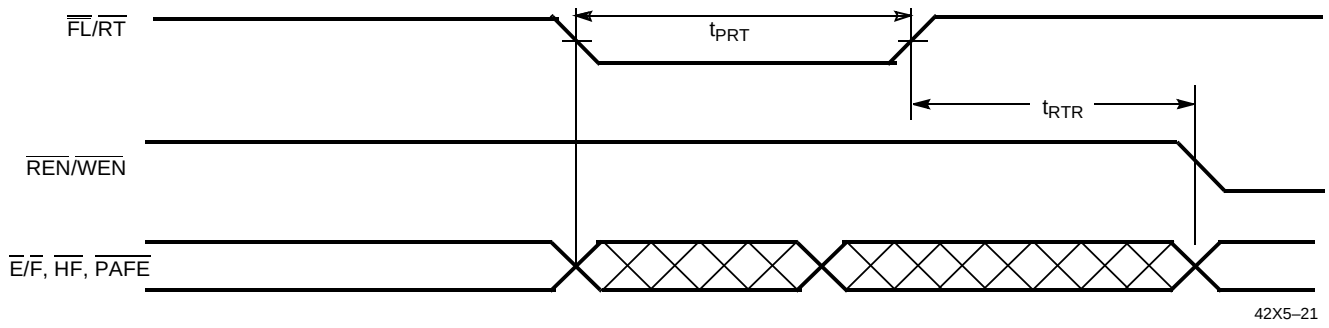
Even Parity Checking[41]



Output Enable Timing[42, 43]



Retransmit Timing[44, 45]



Notes:

41. In this example, the FIFO is assumed to be programmed to check for even parity. The Q_{0-7} word is shown.
42. This example assumes that the time from the CKR rising edge to valid word M+1 $\geq t_A$. The Q_{0-7} word is shown.
43. If ENR was HIGH around the rising edge of CKR (i.e., read disabled), the valid data at the far right would once again be word M instead of word M+1.
44. Clocks are free running in this case.
45. The flags may change state during Retransmit as a result of the offset of the read and write pointers, but flags will be valid at t_{RTR}.

Architecture

The CY7C455/6/7 consists of an array of 512, 1024, or 2048 words of 18 bits each (implemented by a dual-port array of SRAM cells), a read pointer, a write pointer, control signals (CKR, CKW, ENR, ENW, and MR), and flags (HF, E/F, PAFE). The CY7C455/6/7 also includes the control signals OE, FL, XI, and XO for depth expansion.

Resetting the FIFO

Upon power-up, the FIFO must be reset with a Master Reset (MR) cycle. This causes the FIFO to enter the Empty condition signified by E/F and PAFE being LOW and HF being HIGH. All data outputs ($Q_{0–17}$) go low at the rising edge of MR. In order for the FIFO to reset to its default state, a falling edge must occur on MR and the user must not read or write while MR is LOW (unless ENR and ENW are HIGH or unless the device is being programmed). Upon completion of the master reset cycle, all data outputs will go LOW t_{AMR} after MR is deasserted. All flags are guaranteed to be valid t_{MRF} after MR is taken HIGH.

FIFO Operation

When the ENW signal is active (LOW), data present on the $D_{0–17}$ pins is written into the FIFO on each rising edge of the CKW signal. Similarly, when the ENR signal is active, data in the FIFO memory will be presented on the $Q_{0–17}$ outputs. New data will be presented on each rising edge of CKR while ENR is active. ENR must set up t_{SEN} before CKR for it to be a valid read. ENW must occur t_{SEN} before CKW for it to be a valid write.

An output enable (OE) pin is provided to three-state the $Q_{0–17}$ outputs when OE is asserted. When OE is enabled (low), data in the output register will be available to the $Q_{0–17}$ outputs after t_{OE}. If devices are cascaded, the OE function will only output data on the FIFO that is read enabled.

The FIFO contains overflow circuitry to disallow additional writes when the FIFO is full, and underflow circuitry to disallow additional reads when the FIFO is empty. An empty FIFO maintains the data of the last valid read on its $Q_{0–17}$ outputs even after additional reads occur.

Programming

The CY7C455/6/7 is programmed during a master reset cycle. If MR and ENW are LOW, a rising edge on CKW will write the $D_{0–7,8,or9}$ and $D_{15–17}$ inputs into the programming register[46]. MR must be set up a minimum of t_{SMRP} before the program write rising edge and held t_{HMRP} after the program write falling edge. The user has the ability to also perform a program read during the master reset cycle. This will occur at the rising edge of CKR when MR and ENR are asserted. The program read must be performed a minimum of t_{FTP} after a program write, and the program word will be available t_{AP} after the read occurs. If a program write does not occur, a program read may occur a minimum of t_{SMRP} after MR is asserted. This will read the default program value.

When free-running clocks are tied to CKW and CKR, programming can still occur during a master reset cycle with the adherence to a few additional timing parameters. The enable pins must be set-up t_{SEN} before the rising edge of CKW or CKR. Hold times of t_{HEN} must also be met for ENW and ENR.

Data present on $D_{0–9}$ during a program write will determine the distance from Empty (Full) that the Almost Empty (Almost Full) flags will become active. See *Table 1* for a description of the six possible FIFO states. P in *Table 1* refers to the decimal equivalent of the binary number represented by $D_{0–7, 8 or 9}$. Programming options for the CY7C455/6/7 are listed in *Table 4*.

The programmable PAFE function on the CY7C455/6/7 is only valid when not cascaded. If the user elects not to program the FIFO's flags, the default is as follows: the Almost Empty condition (Almost Full condition) is activated when the FIFO contains 16 or less words (empty locations).

Parity is programmed with the $D_{15–17}$ bits. See *Table 4* for a summary of the various parity programming options. Data present on $D_{15–17}$ during a program write will determine whether the FIFO will generate or check even/odd parity for the data present on $D_{0–7}$ and $D_{9–16}$ thereafter. If the user elects not to program the FIFO, the parity function is disabled. Flag operation and parity are described in greater detail in subsequent sections.

Flag Operation

The CY7C455/6/7 provides three status pins when not cascaded. The three pins, E/F, PAFE, and HF, allow decoding of six FIFO states (*Table 1*). PAFE is not available when the CY7C455/6/7 is cascaded for depth expansion. All flags are synchronous, meaning that the change of states is relative to one of the clocks (CKR or CKW, as appropriate).[47] The Empty and Almost Empty flag states are exclusively updated by each rising edge of the read clock (CKR). For example, when the FIFO contains 1 word, the next read (rising edge of CKR while ENR=LOW) causes the flag pins to output a state that represents Empty. The Half Full, Almost Full, and Full flag states are updated exclusively by the write clock (CKW). For example, if the CY7C457 contains 2,047 words (2,048 words indicate Full for the CY7C457), the next write (rising edge of CKW while ENW=LOW) causes the flag pins to output a state that is decoded as Full.

Since the flags denoting emptiness (Empty, Almost Empty) are only updated by CKR and the flags signifying fullness (Half Full, Almost Full, Full) are exclusively updated by CKW, careful attention must be given to the flag operation. The user must be aware that if a boundary (Empty, Almost Empty, Half Full, Almost Full, or Full) is crossed due to an operation from a clock that the flag is not synchronized to (i.e., CKW does not affect Empty or Almost Empty), a flag update cycle is necessary to represent the FIFO's new state. The signal to which a flag is not synchronized will be referred to as the opposite clock (CKW is opposite clock for Empty and Almost Empty flags; CKR is the opposite clock for Half Full, Almost Full, and Full flags). Until a proper flag update cycle is executed, the synchronous flags will not show the new state of the FIFO.

Notes:

46. CKW will write $D_{0–9}$ into the programming register. CKR will read $D_{0–9}$ during a programming register read.
47. The synchronous architecture guarantees the flags valid for approximately one cycle of the clock they are synchronized to.

When updating flags, the FIFO must make a decision as to whether or not the opposite clock was recognized when a clock updates the flag. For example (when updating the Empty flag), if a write occurs at least t_{SKEW1} after a read, the write is guaranteed not to be included when CKR updates the flag. If a write occurs at least t_{SKEW2} before a read, the write is guaranteed to be included when CKR updates flag. If a write occurs within t_{SKEW1} after or t_{SKEW2} before CKR, then the decision of whether or not to include the write when the flag is updated by CKR is arbitrary.

The update cycle for non-boundary flags (Almost Empty, Half Full, Almost Full) is different from that used to update the boundary flags (Empty, Full). Both operations are described below.

Boundary and Non-Boundary Flags

Boundary Flags (Empty)

The Empty flag is synchronized to the CKR signal (i.e., the Empty flag can only be updated by a clock pulse on the CKR pin). An empty FIFO that is written to will be described with an Empty flag state until a rising edge is presented to the CKR pin. When making the transition from Empty to Almost Empty (or Empty to Less than or Equal to Half Full), a clock cycle on CKR is necessary to update the flags to the current state. In such a state (flags showing Empty even though data has been written to the FIFO), two read clock cycles are required to read data out of the FIFO. The first read serves only to update the flags to the Almost Empty or Less than or Equal to Half Full state, while the second read outputs the data. This first read cycle is known as the latent or flag update cycle because it does not affect the data in the FIFO or the count (number of words in FIFO). It simply deasserts the Empty flag. The flag is updated regardless of the $\overline{ENR}$ state. Therefore, the update occurs even when $\overline{ENR}$ is deasserted (HIGH), so that a valid read is not necessary to update the flags to correctly describe the FIFO. In this example, the write must occur at least t_{SKEW2} before the flag update cycle in order for the FIFO to guarantee that the write will be included in the count when CKR updates the flags. When a free-running clock is connected to CKR, the flag is updated each cycle. *Table 2* shows an example of a sequence of operations that update the Empty flag.

Boundary Flags (Full)

The Full flag is synchronized to the CKW signal (i.e., the Full flag can only be updated by a clock pulse on the CKW pin). A full FIFO that is read will be described with a Full flag until a rising edge is presented to the CKW pin. When making the transition from Full to Almost Full (or Full to Greater Than Half Full), a clock cycle on CKW is necessary to update the flags to the current state. In such a state (flags showing Full even through data has been read from the FIFO), two write cycles are required to write data into the FIFO. The first write serves only to update the flags to the Almost Full or Greater Than Half Full state, while the second write inputs the data. This first write cycle is known as the latent or flag update cycle because it does not affect the data in the FIFO or the count (number of words in the FIFO). It simply deasserts the Full flag. The flag is updated regardless of the $\overline{ENW}$ state. Therefore, the update occurs even when $\overline{ENW}$ is deasserted (HIGH), so that a valid write is not necessary to update the flags to correctly describe the FIFO. In this example, the read must occur at least t_{SKEW2} before the flag update cycle in order for the FIFO to guarantee that the read will be included in the count when CKW updates the flags. When a free-running clock is connected to CKW, the flag updates each cycle. Full flag operation is similar to the Empty flag operation described in *Table 2*.

Non-Boundary Flags (Almost Empty, Half Full, Almost Full)

The CY7C455/6/7 features programmable Almost Empty and Almost Full flags. Each flag can be programmed a specific distance from the corresponding boundary flags (Empty or Full). The flags can be programmed to be activated at the Empty or Full boundary, or at any distance from the Empty/Full boundary. When the FIFO contains the number of words or fewer for which the flags have been programmed, the $\overline{PAFE}$ flag will be asserted signifying that the FIFO is Almost Empty. When the FIFO is within that same number of empty locations from being Full, the $\overline{PAFE}$ will also be asserted signifying that the FIFO is Almost Full. The $\overline{HF}$ flag is decoded to distinguish the states.

The default distance from where $\overline{PAFE}$ becomes active to the boundary (Empty, Full) is 16 words/locations. The Almost Full and Almost Empty flags can be programmed so that they are only active at Full and Empty boundaries. However, the operation will remain consistent with the non-boundary flag operation that is discussed below.

Table 1. Flag Truth Table[48]

$\overline{E}/\overline{F}$	PAFE	$\overline{HF}$	State	7C455 Words in FIFO	7C456 Words in FIFO	7C457 Words in FIFO
0	0	1	Empty	0	0	0
1	0	1	Almost Empty	1 => P	1 => P	1 => P
1	1	1	Less than or Equal to Half Full	P + 1 => 256	P + 1 => 512	P + 1 => 1024
1	1	0	Greater than Half Full	257 => 511 – P	513 => 1023 – P	1025 => 2047 – P
1	0	0	Almost Full	512 – P => 511	1024 – P => 1023	2048 – P => 2047
0	0	0	Full	512	1024	2048

Notes:
48. P is the decimal value of the binary number represented by D_{0-7} for the CY7C455, D_{0-8} for the CY7C456, and D_{0-9} for the CY7C457. P = 0 signifies that the Almost Empty state = Empty state.

Table 2. Empty Flag (Boundary Flag) Operation Example

Status Before Operation						Status After Operation					
Current State of FIFO	$\overline{E}/\overline{F}$	$\overline{AFE}$	$\overline{HF}$	Number of Words in FIFO	Operation	Next State of FIFO	$\overline{E}/\overline{F}$	$\overline{AFE}$	$\overline{HF}$	Number of Words in FIFO	Comments
Empty	0	0	1	0	Write ($\overline{ENW}$ = 0)	Empty	0	0	1	1	Write
Empty	0	0	1	1	Write ($\overline{ENW}$ = 0)	Empty	0	0	1	2	Write
Empty	0	0	1	2	Read ($\overline{ENR}$ = X)	AE	1	0	1	2	Flag Update
AE	1	0	1	2	Read ($\overline{ENR}$ = 0)	AE	1	0	1	1	Read
AE	1	0	1	1	Read ($\overline{ENR}$ = 0)	Empty	0	0	1	0	Read (transition from Almost Empty to Empty)
Empty	0	0	1	0	Write ($\overline{ENR}$ = 0)	Empty	0	0	1	1	Write
Empty	1	0	1	1	Read ($\overline{ENR}$ = X)	AE	1	0	1	1	Flag Update
AE	1	0	1	1	Read ($\overline{ENR}$ = 0)	Empty	0	0	1	0	Read (transition from Almost Empty to Empty)

Almost Empty is only updated by CKR while Half Full and Almost Full are updated by CKW. Non-boundary flags employ flag update cycles similar to the boundary flag latent cycles in order to update the FIFO status. For example, if the FIFO just reaches the Greater than Half Full state, and then two words are read from the FIFO, a write clock (CKW) will be required to update the flags to the Less than Half Full state. However, unlike the boundary flag latent cycle, the state of the enable pin ($\overline{ENW}$ in this case) affects the operation. Therefore, set-up and hold times for the enable pins must be met (t_{SEN} and t_{HEN}). If the enable pin is active during the flag update cycle, the count and data are updated in addition to $\overline{PAFE}$ and $\overline{HF}$. If the enable pin is not asserted during the flag update cycle, only the flags are updated. *Table 3* shows an example of a sequence of operations that update the Almost Empty and Almost Full flags

The CY7C455/6/7 also features even or odd parity checking and generation. $D_{15–17}$ are used during a program write to describe the parity option desired. *Table 4* summarizes programmable parity options. If the user elects not to program the device, then parity is disabled. Parity information is provided on two multi-mode output pins (Q_8/PG1/$\overline{PE1}$ and Q_{17}/PG2/$\overline{PE2}$). The three possible modes are described in the following paragraphs.

Programmable Parity

Parity Disabled (Q_8/Q_{17} mode)

When parity is disabled (or the user does not program parity option) the FIFO stores all 18 bits present on $D_{0–17}$ inputs internally and will output all 18 bits on $Q_{0–17}$.

Parity Generate (PG mode)

This mode is used to generate either even or odd parity (as programmed) from $D_{0–7}$ and $D_{9–16}$. D_8 and D_{17} inputs are ignored. The parity bits are stored internally as D_8 and D_{17}, and during a subsequent read will be available on the PG1 and PG2 pins along with the data words from which the parity was generated ($Q_{0–7}$ and $Q_{9–16}$). For example, if parity generate is set to ODD and the $D_{0–7}$ inputs have an EVEN number of 1s, PG1 will be HIGH.

Parity Check ($\overline{PE}$ mode)

If the FIFO is programmed for parity checking, it will compare the parity of $D_{0–8}$ and $D_{9–17}$ with the program register. For example, D_8 and D_{17} will be set according to the result of the parity check on each word. When these words are later read, $\overline{PE_1}$ and $\overline{PE_2}$ will reflect the result of the parity check. If a parity error occurs in $D_{0–8}$, D_8 will be set LOW internally. When this word is later read, $\overline{PE_1}$ will be LOW.

Retransmit

The retransmit feature is beneficial when transferring packets of data. It enables the receipt of data to be acknowledged by the receiver and retransmitted if necessary.

The Retransmit ($\overline{RT}$) input is active in the standalone and width expansion modes. The retransmit feature is intended for use when a number of writes equal to or less than the depth of the FIFO have occurred since the last $\overline{MR}$ cycle. A LOW pulse on $\overline{RT}$ resets the internal read pointer to the first physical location of the FIFO. WCLK and RCLK may be free running but must be disabled during and t_{RTR} after the retransmit pulse. With every valid read cycle after retransmit, previously accessed data is read and the read pointer is incremented until it is equal to the write pointer. Flags are governed by the relative locations of the read and write pointers and are updated during a retransmit cycle. Data written to the FIFO after activation of $\overline{RT}$ are transmitted also.

The full depth of the FIFO can be repeatedly retransmitted.

Width Expansion Modes

During width expansion all flags (programmable and nonprogrammable) are available. These FIFOs can be expanded in width to provide word width greater than 18 in increments of 18. During width expansion mode all control line inputs are common. When the FIFO is being read near the Empty (Full) boundary, it is important to note that both sets of flags should be checked to see if they have been updated to the Not Empty (Not Full) condition to insure that the next read (write) will perform the same operation on all devices.

Checking all sets of flags is critical so that data is not read from the FIFOs "staggered" by one clock cycle. This situation could occur when the first write to an empty FIFO and a read are very close together. If the read occurs less than t_{SKEW2} after the first write to two width-expanded devices, A and B, device A may go Almost Empty (read recognized as flag update) while device B stays Empty (read ignored). This occurs because a read can be either recognized or ignored if it occurs within t_{SKEW2} of a write. The next read cycle outputs the first half of the first word on device A while device B updates its flags to Almost Empty. Subsequent reads will continue to output "staggered" data assuming more data has been written to FIFOs.

Depth Expansion Mode

The CY7C455/6/7 can operate up to 83.3 MHz when cascaded. Depth expansion is accomplished by connecting expansion out ($\overline{XO}$) of the first device to expansion in ($\overline{XI}$) of the next device, with $\overline{XO}$ of the last device connected to $\overline{XI}$ of the first device. The first device has its first load pin ($\overline{FL}$) tied to V_{SS} while all other devices must have this pin tied to V_{CC}. The first device will be the first to be write and read enabled after a master reset.

Proper operation also requires that all cascaded devices have common CKW, CKR, $\overline{ENW}$, $\overline{ENR}$, $D_{0–17}$, $Q_{0–17}$, and $\overline{MR}$ pins. When cascaded, one device at a time will be read enabled so as to avoid bus contention. By asserting $\overline{XO}$ when appropriate, the currently enabled FIFO alerts the next FIFO that it should be enabled. The next rising edge on CKR puts $Q_{0–17}$ outputs of the first device into a high-impedance state. This occurs regardless of the state of $\overline{ENR}$ or the next FIFO's Empty flag. Therefore, if the next FIFO is empty or undergoing a latent cycle, the $Q_{0–17}$ bus will be in a high-impedance state until the next device receives its first read, which brings its data to the $Q_{0–17}$ bus.

Program Write/Read of Cascaded Devices

Programming of cascaded FIFOs is the same as for a single device. Because the controls of the FIFOs are in parallel when cascaded, they all get programmed the same. During program mode, only parity is programmed since Almost Full and Almost Empty flags are not available when CY7C455/6/7 is cascaded. Only the "first device" (FIFO with $\overline{FL}$=LOW) will output its program register contents on $Q_{0–7}$ during a program read. $Q_{0–17}$ of all other devices will remain in a high-impedance state to avoid bus contention.

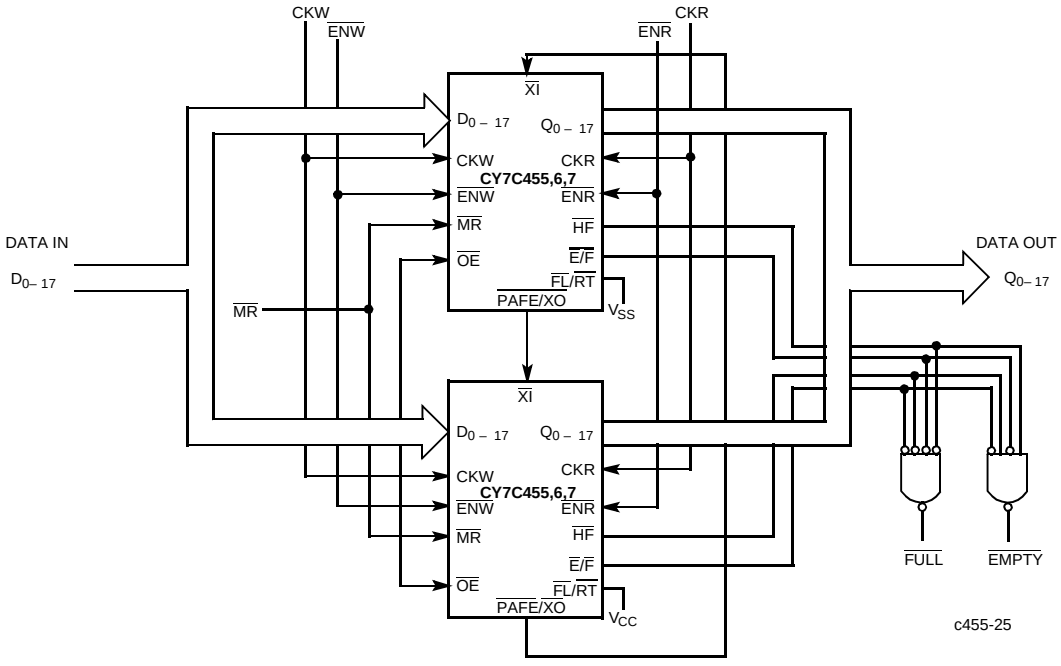


Figure 1. Depth Expansion with CY7C455/6/7

Table 3. Almost Empty Flag (Non-Boundary Flag) Operation Example[49]

Status Before Operation						Status After Operation					
Current State of FIFO	$\overline{E}/\overline{F}$	$\overline{AFE}$	$\overline{HF}$	Number of Words in FIFO	Operation	Next State of FIFO	$\overline{E}/\overline{F}$	$\overline{PAFE}$	$\overline{HF}$	Number of words in FIFO	Comments
AE	1	0	1	32	Write ($\overline{ENW}$ = 0)	AE	1	0	1	33	Write
AE	1	0	1	33	Write ($\overline{ENW}$ = 0)	AE	1	0	1	34	Write
AE	1	0	1	34	Read ($\overline{ENR}$ = 0)	<HF	1	1	1	33	Flag Update and Read
<HF	1	1	1	33	Read ($\overline{ENR}$ = 1)	<HF	1	1	1	33	Ignored Read ($\overline{ENR}$ = 1)
<HF	1	1	1	33	Read ($\overline{ENR}$ = 0)	AE	1	0	1	32	Read (transition from <HF to AE)

Table 4. Programmable Parity Options

D17	D16	D15	Condition
0	X	X	Parity disabled.
1	0	0	Generate even parity on PG output pin.
1	0	1	Generate odd parity on PG output pin.
1	1	0	Check for even parity. Indicate error on $\overline{PE}$ output pin.
1	1	1	Check for odd parity. Indicate error on $\overline{PE}$ output pin.

Note:
49. Applies to CY7C455/6/7 operations when devices are programmed so that Almost Empty becomes active when the FIFO contains 32 or fewer words.

Ordering Information

512x18 Clocked FIFO

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
12	CY7C455–12JC	J69	52-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C455–12NC	N52	52-Pin Plastic Quad Flatpack	
	CY7C455–12JI	J69	52-Lead Plastic Leaded Chip Carrier	Industrial
14	CY7C455–14JC	J69	52-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C455–14NC	N52	52-Pin Plastic Quad Flatpack	
	CY7C455–14JI	J69	52-Lead Plastic Leaded Chip Carrier	Industrial
20	CY7C455–20JC	J69	52-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C455–20NC	N52	52-Pin Plastic Quad Flatpack	
	CY7C455–20JI	J69	52-Lead Plastic Leaded Chip Carrier	Industrial
30	CY7C455–30JC	J69	52-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C455–30NC	N52	52-Pin Plastic Quad Flatpack	
	CY7C455–30JI	J69	52-Lead Plastic Leaded Chip Carrier	Industrial

1Kx18 Clocked FIFO

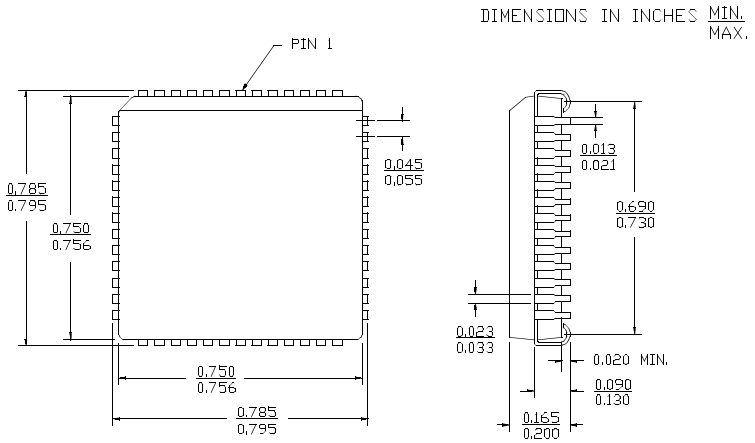
Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
12	CY7C456–12JC	J69	52-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C456–12NC	N52	52-Pin Plastic Quad Flatpack	
	CY7C456–12JI	J69	52-Lead Plastic Leaded Chip Carrier	Industrial
14	CY7C456–14JC	J69	52-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C456–14NC	N52	52-Pin Plastic Quad Flatpack	
	CY7C456–14JI	J69	52-Lead Plastic Leaded Chip Carrier	Industrial
20	CY7C456–20JC	J69	52-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C456–20NC	N52	52-Pin Plastic Quad Flatpack	
	CY7C456–20JI	J69	52-Lead Plastic Leaded Chip Carrier	Industrial
30	CY7C456–30JC	J69	52-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C456–30NC	N52	52-Pin Plastic Quad Flatpack	
	CY7C456–30JI	J69	52-Lead Plastic Leaded Chip Carrier	Industrial

2Kx18 Clocked FIFO

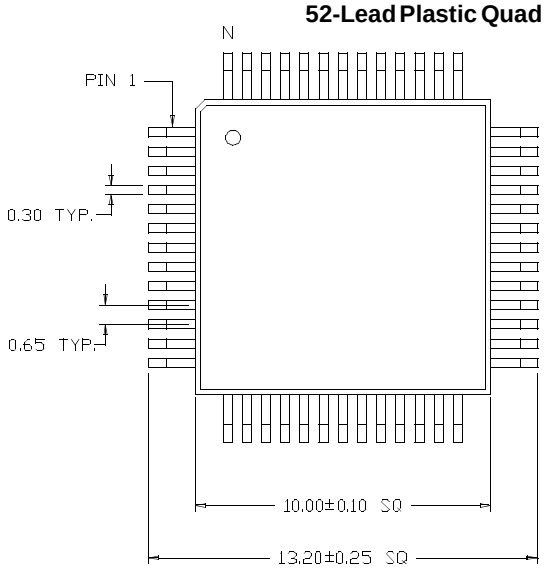
Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
12	CY7C457–12JC	J69	52-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C457–12NC	N52	52-Pin Plastic Quad Flatpack	
	CY7C457–12JI	J69	52-Lead Plastic Leaded Chip Carrier	Industrial
14	CY7C457–14JC	J69	52-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C457–14NC	N52	52-Pin Plastic Quad Flatpack	
	CY7C457–14JI	J69	52-Lead Plastic Leaded Chip Carrier	Industrial
20	CY7C457–20JC	J69	52-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C457–20NC	N52	52-Pin Plastic Quad Flatpack	
	CY7C457–20JI	J69	52-Lead Plastic Leaded Chip Carrier	Industrial
30	CY7C457–30JC	J69	52-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C457–30NC	N52	52-Pin Plastic Quad Flatpack	
	CY7C457–30JI	J69	52-Lead Plastic Leaded Chip Carrier	Industrial

Package Diagrams

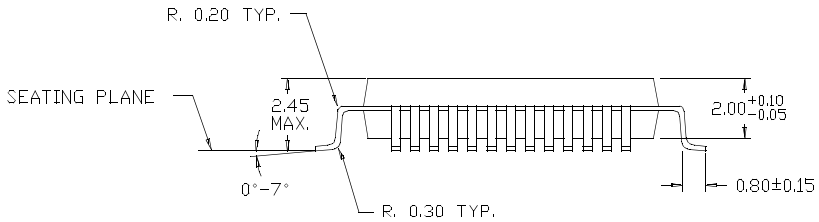
52-Lead Plastic Leaded Chip Carrier J69



52-Lead Plastic Quad Flatpack N52



DIMENSIONS ARE IN MILLIMETERS
LEAD COPLANARITY 0.102 MAX.



Document Title: CY7C455, CY7C456, CY7C457 512 X 18, 1K X 18 and 2K X 18 Cascadable Clocked Fifo's with Programmable Flags Document Number: 38-06003				
REV.	**ECN NO.**	**Issue Date**	**Orig. of Change**	**Description of Change**
**	106464	07/11/01	SZV	Change from Spec Number: 38-00211 to 38-06003
*A	122256	12/26/02	RBI	Power up requirements added to Maximum Ratings Information