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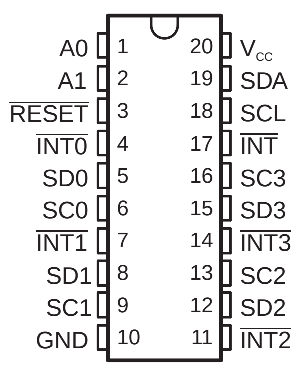
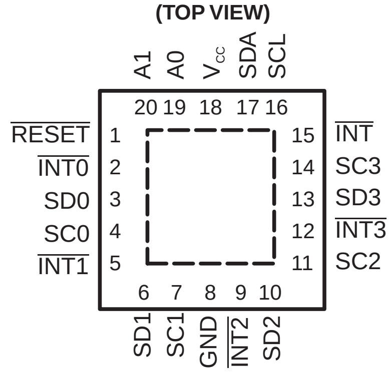
FEATURES

- **1-of-4 Bidirectional Translating Switches**
- **I²C Bus and SMBus Compatible**
- **Four Active-Low Interrupt Inputs**
- **Active-Low Interrupt Output**
- **Active-Low Reset Input**
- **Two Address Pins, Allowing up to Four Devices on the I²C Bus**
- **Channel Selection Via I²C Bus, In Any Combination**
- **Power Up With All Switch Channels Deselected**
- **Low R_{ON} Switches**
- **Allows Voltage-Level Translation Between 1.8-V, 2.5-V, 3.3-V, and 5-V Buses**
- **No Glitch on Power Up**
- **Supports Hot Insertion**
- **Low Standby Current**
- **Operating Power-Supply Voltage Range of 2.3 V to 5.5 V**
- **5.5-V Tolerant Inputs**
- **0 to 400-kHz Clock Frequency**
- **Latch-Up Performance Exceeds 100 mA Per JESD 78**
- **ESD Protection Exceeds JESD 22**
  - **2000-V Human-Body Model (A114-A)**
  - **200-V Machine Model (A115-A)**
  - **1000-V Charged-Device Model (C101)**

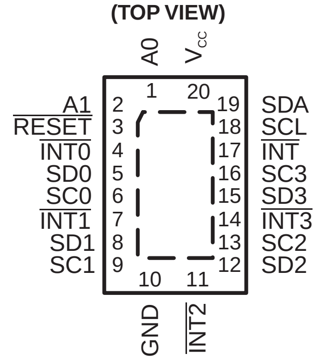
DGV, DW, OR PW PACKAGE (TOP VIEW)



RGW PACKAGE (TOP VIEW)



RGY PACKAGE (TOP VIEW)



DESCRIPTION/ORDERING INFORMATION

The PCA9545A is a quad bidirectional translating switch controlled via the I²C bus. The SCL/SDA upstream pair fans out to four downstream pairs, or channels. Any individual SCn/SDn channel or combination of channels can be selected, determined by the contents of the programmable control register. Four interrupt inputs ($\overline{\text{INT3}}$–$\overline{\text{INT0}}$), one for each of the downstream pairs, are provided. One interrupt ($\overline{\text{INT}}$) output acts as an AND of the four interrupt inputs.

An active-low reset ($\overline{\text{RESET}}$) input allows the PCA9545A to recover from a situation in which one of the downstream I²C buses is stuck in a low state. Pulling $\overline{\text{RESET}}$ low resets the I²C state machine and causes all the channels to be deselected, as does the internal power-on reset function.

The pass gates of the switches are constructed such that the V_{CC} pin can be used to limit the maximum high voltage, which will be passed by the PCA9545A. This allows the use of different bus voltages on each pair, so that 1.8-V, 2.5-V, or 3.3-V parts can communicate with 5-V parts, without any additional protection. External pullup resistors pull the bus up to the desired voltage level for each channel. All I/O pins are 5.5-V tolerant.

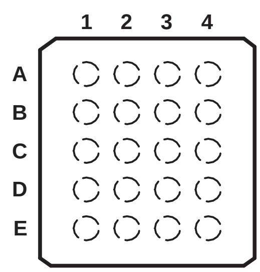
DESCRIPTION/ORDERING INFORMATION (CONTINUED)

ORDERING INFORMATION

T_A	PACKAGE(1)		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	QFN – RGW	Reel of 3000	PCA9545ARGWR	PD545A
	QFN – RGY	Reel of 1000	PCA9545ARGYR	PD545A
	SOIC – DW	Tube of 25	PCA9545ADW	PCA9545A
		Reel of 2000	PCA9545ADWR	
		Reel of 250	PCA9545ADWT	PCA9545A
	TSSOP – PW	Tube of 70	PCA9545APW	PD545A
			PCA9545APWE4	
		Reel of 2000	PCA9545APWR	PD545A
			PCA9545APWRE4	
		Reel of 250	PCA9545APWT	PD545A
			PCA9545APWTE4	
	TVSOP – DGV	Reel of 2000	PCA9545ADGVR	PD545A
		Reel of 250	PCA9545ADGVT	
	VFBGA – GQN	Reel of 1000	PCA9545AGQNR	PD545A
	VFBGA – ZQN (Pb-free)	Reel of 1000	PCA9545AZQNR	PD545A

(1) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

**GQN OR ZQN PACKAGE
(TOP VIEW)**



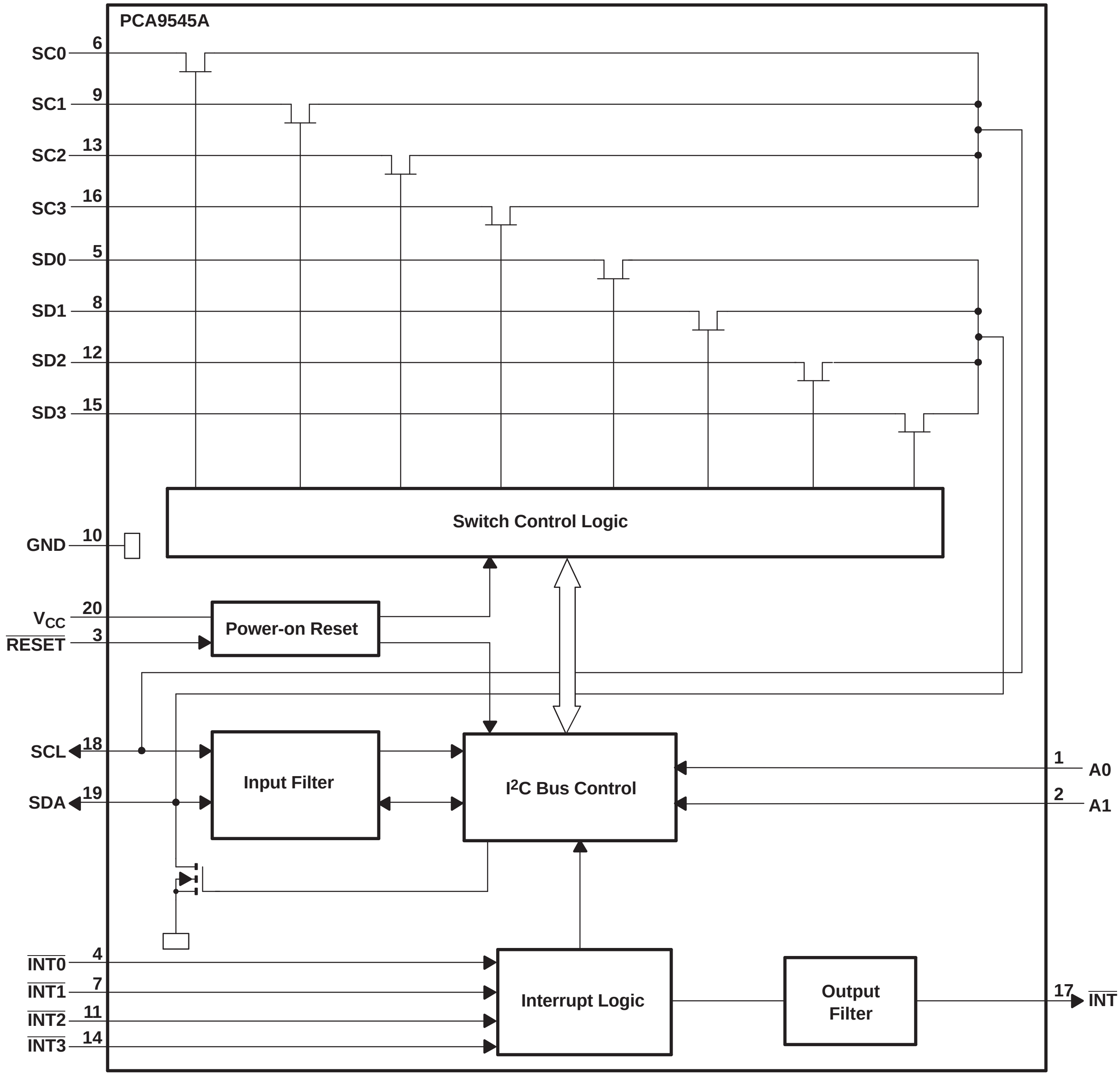
TERMINAL ASSIGNMENTS

	1	2	3	4
A	A1	A0	V_{CC}	SDA
B	$\overline{\text{INT0}}$	$\overline{\text{INT}}$	$\overline{\text{RESET}}$	SCL
C	SC0	SD0	SD3	SC3
D	SD1	SC2	$\overline{\text{INT1}}$	$\overline{\text{INT3}}$
E	GND	SC1	$\overline{\text{INT2}}$	SD2

TERMINAL FUNCTIONS

NO.			NAME	DESCRIPTION
DGV, DW, PW, AND RGY	RGW	GQN AND ZQN		
1	19	A2	A0	Address input 0. Connect directly to V_{CC} or ground.
2	20	A1	A1	Address input 1. Connect directly to V_{CC} or ground.
3	1	B3	$\overline{\text{RESET}}$	Active-low reset input. Connect to V_{CC} through a pullup resistor, if not used.
4	2	B1	$\overline{\text{INT0}}$	Active-low interrupt input 0. Connect to V_{CC} through a pullup resistor.
5	3	C2	SD0	Serial data 0. Connect to V_{CC} through a pullup resistor.
6	4	C1	SC0	Serial clock 0. Connect to V_{CC} through a pullup resistor.
7	5	D3	$\overline{\text{INT1}}$	Active-low interrupt input 1. Connect to V_{CC} through a pullup resistor.
8	6	D1	SD1	Serial data 1. Connect to V_{CC} through a pullup resistor.
9	7	E2	SC1	Serial clock 1. Connect to V_{CC} through a pullup resistor.
10	8	E1	GND	Ground
11	9	E3	$\overline{\text{INT2}}$	Active-low interrupt input 2. Connect to V_{CC} through a pullup resistor.
12	10	E4	SD2	Serial data 2. Connect to V_{CC} through a pullup resistor.
13	11	D2	SC2	Serial clock 2. Connect to V_{CC} through a pullup resistor.
14	12	D4	$\overline{\text{INT3}}$	Active-low interrupt input 3. Connect to V_{CC} through a pullup resistor.
15	13	C3	SD3	Serial data 3. Connect to V_{CC} through a pullup resistor.
16	14	C4	SC3	Serial clock 3. Connect to V_{CC} through a pullup resistor.
17	15	B2	$\overline{\text{INT}}$	Active-low interrupt output. Connect to V_{CC} through a pullup resistor.
18	16	B4	SCL	Serial clock line. Connect to V_{CC} through a pullup resistor.
19	17	A4	SDA	Serial data line. Connect to V_{CC} through a pullup resistor.
20	18	A3	V_{CC}	Supply power

BLOCK DIAGRAM



Pin numbers shown are for DGV, DW, PW, and RGY packages.

Device Address

Following a start condition, the bus master must output the address of the slave it is accessing. The address of the PCA9545A is shown in Figure 1. To conserve power, no internal pullup resistors are incorporated on the hardware-selectable address pins, and they must be pulled high or low.

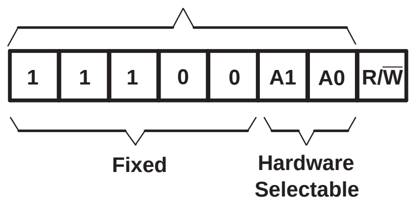


Figure 1. PCA9545A Address

The last bit of the slave address defines the operation to be performed. When set to a logic 1, a read is selected, while a logic 0 selects a write operation.

Control Register

Following the successful acknowledgment of the slave address, the bus master sends a byte to the PCA9545A, which is stored in the control register (see Figure 2). If multiple bytes are received by the PCA9545A, it saves the last byte received. This register can be written and read via the I²C bus.

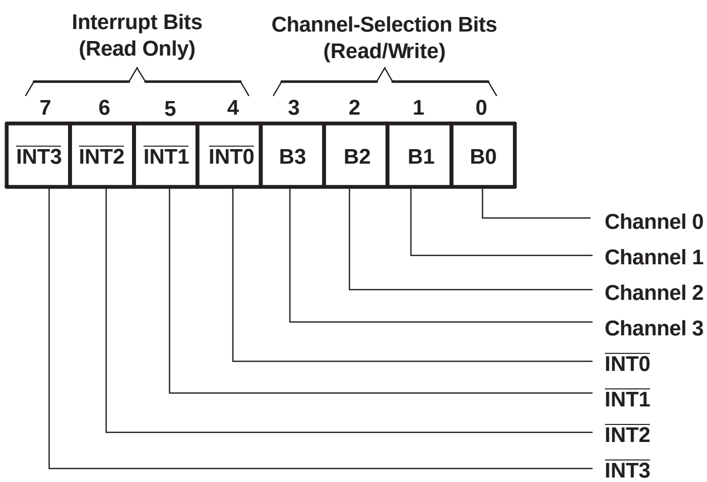


Figure 2. Control Register

Control Register Definition

One or several SCn/SDn downstream pairs, or channels, are selected by the contents of the control register (see Table 1). After the PCA9545A has been addressed, the control register is written. The four LSBs of the control byte are used to determine which channel or channels are to be selected. When a channel is selected, the channel becomes active after a stop condition has been placed on the I²C bus. This ensures that all SCn/SDn lines are in a high state when the channel is made active, so that no false conditions are generated at the time of connection. A stop condition must occur always right after the acknowledge cycle.

Table 1. Control Register Write (Channel Selection), Control Register Read (Channel Status)(1)

<table>
<tr><th>$\overline{\text{INT3}}$</th><th>$\overline{\text{INT2}}$</th><th>$\overline{\text{INT1}}$</th><th>$\overline{\text{INT0}}$</th><th>D3</th><th>B2</th><th>B1</th><th>B0</th><th>COMMAND</th></tr>
<tr><td rowspan="2">X</td><td rowspan="2">X</td><td rowspan="2">X</td><td rowspan="2">X</td><td rowspan="2">X</td><td rowspan="2">X</td><td rowspan="2">X</td><td>0</td><td>Channel 0 disabled</td></tr>
<tr><td>1</td><td>Channel 0 enabled</td></tr>
<tr><td rowspan="2">X</td><td rowspan="2">X</td><td rowspan="2">X</td><td rowspan="2">X</td><td rowspan="2">X</td><td rowspan="2">X</td><td>0</td><td rowspan="2">X</td><td>Channel 1 disabled</td></tr>
<tr><td>1</td><td>Channel 1 enabled</td></tr>
<tr><td rowspan="2">X</td><td rowspan="2">X</td><td rowspan="2">X</td><td rowspan="2">X</td><td rowspan="2">X</td><td>0</td><td rowspan="2">X</td><td rowspan="2">X</td><td>Channel 2 disabled</td></tr>
<tr><td>1</td><td>Channel 2 enabled</td></tr>
<tr><td rowspan="2">X</td><td rowspan="2">X</td><td rowspan="2">X</td><td rowspan="2">X</td><td>0</td><td rowspan="2">X</td><td rowspan="2">X</td><td rowspan="2">X</td><td>Channel 3 disabled</td></tr>
<tr><td>1</td><td>Channel 3 enabled</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>X</td><td>0</td><td>No channel selected,
power-up/reset default state</td></tr>
</table>

(1) Several channels can be enabled at the same time. For example, B3 = 0, B2 = 1, B1 = 1, B0 = 0 means that channels 0 and 3 are disabled, and channels 1 are 2 and enabled. Care should be taken not to exceed the maximum bus capacity.

Interrupt Handling

The PCA9545A provides four interrupt inputs (one for each channel) and one open-drain interrupt output (see Table 2). When an interrupt is generated by any device, it is detected by the PCA9545A and the interrupt output is driven low. The channel does not need to be active for detection of the interrupt. A bit also is set in the control register.

Bits 4–7 of the control register correspond to channels 0–3 of the PCA9545A, respectively. Therefore, if an interrupt is generated by any device connected to channel 1, the state of the interrupt inputs is loaded into the control register when a read is accomplished. Likewise, an interrupt on any device connected to channel 0 would cause bit 4 of the control register to be set on the read. The master then can address the PCA9545A and read the contents of the control register to determine which channel contains the device generating the interrupt. The master then can reconfigure the PCA9545A to select this channel and locate the device generating the interrupt and clear it.

It should be noted that more than one device can provide an interrupt on a channel, so it is up to the master to ensure that all devices on a channel are interrogated for an interrupt.

The interrupt inputs can be used as general-purpose inputs if the interrupt function is not required.

If unused, interrupt input(s) must be connected to V_{CC}.

Table 2. Control Register Read (Interrupt)(1)

<table>
<tr><th>$\overline{\text{INT3}}$</th><th>$\overline{\text{INT2}}$</th><th>$\overline{\text{INT1}}$</th><th>$\overline{\text{INT0}}$</th><th>D3</th><th>B2</th><th>B1</th><th>B0</th><th>COMMAND</th></tr>
<tr><td rowspan="2">X</td><td rowspan="2">X</td><td rowspan="2">X</td><td>0</td><td rowspan="2">X</td><td rowspan="2">X</td><td rowspan="2">X</td><td rowspan="2">X</td><td>No interrupt on channel 0</td></tr>
<tr><td>1</td><td>Interrupt on channel 0</td></tr>
<tr><td rowspan="2">X</td><td rowspan="2">X</td><td>0</td><td rowspan="2">X</td><td rowspan="2">X</td><td rowspan="2">X</td><td rowspan="2">X</td><td rowspan="2">X</td><td>No interrupt on channel 1</td></tr>
<tr><td>1</td><td>Interrupt on channel 1</td></tr>
<tr><td rowspan="2">X</td><td>0</td><td rowspan="2">X</td><td rowspan="2">X</td><td rowspan="2">X</td><td rowspan="2">X</td><td rowspan="2">X</td><td rowspan="2">X</td><td>No interrupt on channel 2</td></tr>
<tr><td>1</td><td>Interrupt on channel 2</td></tr>
<tr><td>0</td><td rowspan="2">X</td><td rowspan="2">X</td><td rowspan="2">X</td><td rowspan="2">X</td><td rowspan="2">X</td><td rowspan="2">X</td><td rowspan="2">X</td><td>No interrupt on channel 3</td></tr>
<tr><td>1</td><td>Interrupt on channel 3</td></tr>
</table>

(1) Several interrupts can be active at the same time. For example, $\overline{\text{INT3}}$ = 0, $\overline{\text{INT2}}$ = 1, $\overline{\text{INT1}}$ = 1, $\overline{\text{INT0}}$ = 0 means that there is no interrupt on channels 0 and 3, and there is interrupt on channels 1 and 2.

$\overline{\text{RESET}}$ Input

The $\overline{\text{RESET}}$ input can be used to recover the PCA9545A from a bus-fault condition. The registers and the I^2C state machine within this device initialize to their default states if this signal is asserted low for a minimum of t_{WL}. All channels also are deselected in this case. $\overline{\text{RESET}}$ must be connected to V_{CC} through a pullup resistor.

Power-On Reset

When power is applied to V_{CC}, an internal power-on reset holds the PCA9545A in a reset condition until V_{CC} has reached V_{POR}. At this point, the reset condition is released and the PCA9545A registers and I^2C state machine are initialized to their default states, all zeroes, causing all the channels to be deselected. Thereafter, V_{CC} must be lowered below 0.2 V to reset the device.

Voltage Translation

The pass-gate transistors of the PCA9545A are constructed such that the V_{CC} voltage can be used to limit the maximum voltage that is passed from one I^2C bus to another.

Figure 3 shows the voltage characteristics of the pass-gate transistors (note that the graph was generated using data specified in the *electrical characteristics* section of this data sheet). In order for the PCA9545A to act as a voltage translator, the V_{pass} voltage must be equal to or lower than the lowest bus voltage. For example, if the main bus is running at 5 V and the downstream buses are 3.3 V and 2.7 V, V_{pass} must be equal to or below 2.7 V to effectively clamp the downstream bus voltages. As shown in Figure 3, V_{pass} (max) is at 2.7 V when the PCA9545A supply voltage is 3.5 V or lower, so the PCA9545A supply voltage could be set to 3.3 V. Pullup resistors then can be used to bring the bus voltages to their appropriate levels (see Figure 13).

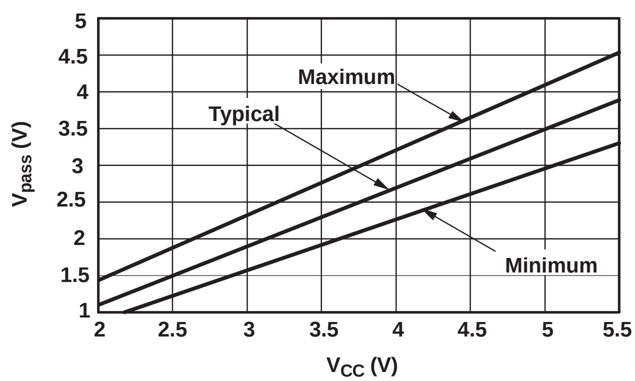


Figure 3. V_{pass} Voltage vs V_{CC}

I²C Interface

The I^2C bus is for two-way two-line communication between different ICs or modules. The two lines are a serial data line (SDA) and a serial clock line (SCL). Both lines must be connected to a positive supply via a pullup resistor when connected to the output stages of a device. Data transfer can be initiated only when the bus is not busy.

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the high period of the clock pulse, as changes in the data line at this time are interpreted as control signals (see Figure 4).

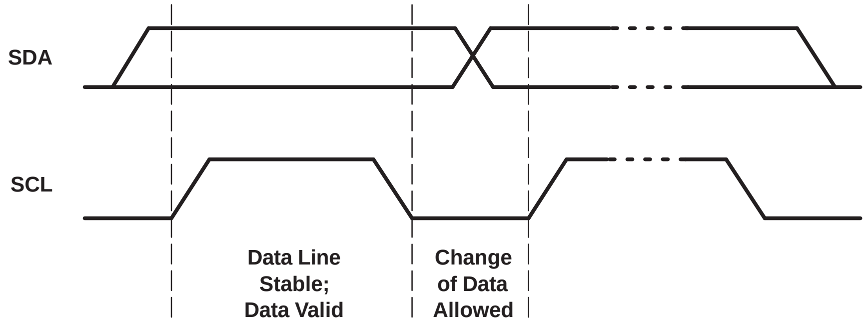


Figure 4. Bit Transfer

Both data and clock lines remain high when the bus is not busy. A high-to-low transition of the data line while the clock is high is defined as the start condition (S). A low-to-high transition of the data line while the clock is high is defined as the stop condition (P) (see Figure 5).

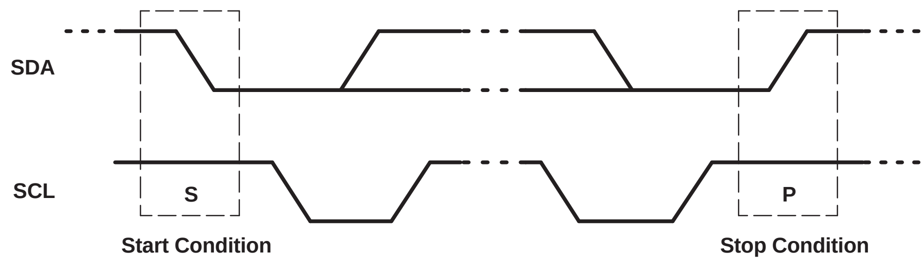


Figure 5. Definition of Start and Stop Conditions

A device generating a message is a transmitter; a device receiving a message is the receiver. The device that controls the message is the master, and the devices that are controlled by the master are the slaves (see Figure 6).

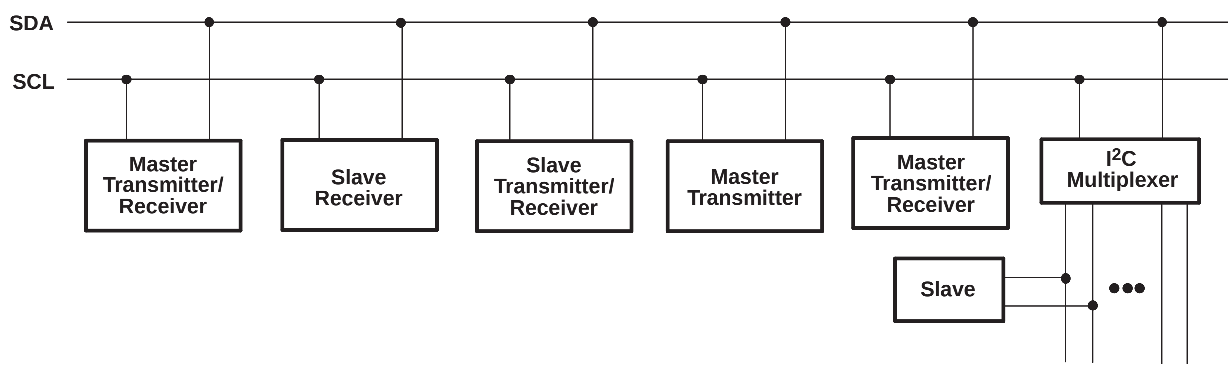


Figure 6. System Configuration

The number of data bytes transferred between the start and the stop conditions from transmitter to receiver is not limited. Each byte of eight bits is followed by one acknowlege (ACK) bit. The transmitter must release the SDA line before the receiver can send an ACK bit.

When a slave receiver is addressed, it must generate an ACK after the reception of each byte. Also, a master must generate an ACK after the reception of each byte that has been clocked out of the slave transmitter. The device that acknowledges must pull down the SDA line during the ACK clock pulse so that the SDA line is stable low during the high pulse of the ACK-related clock period (see Figure 7). Setup and hold times must be taken into account.

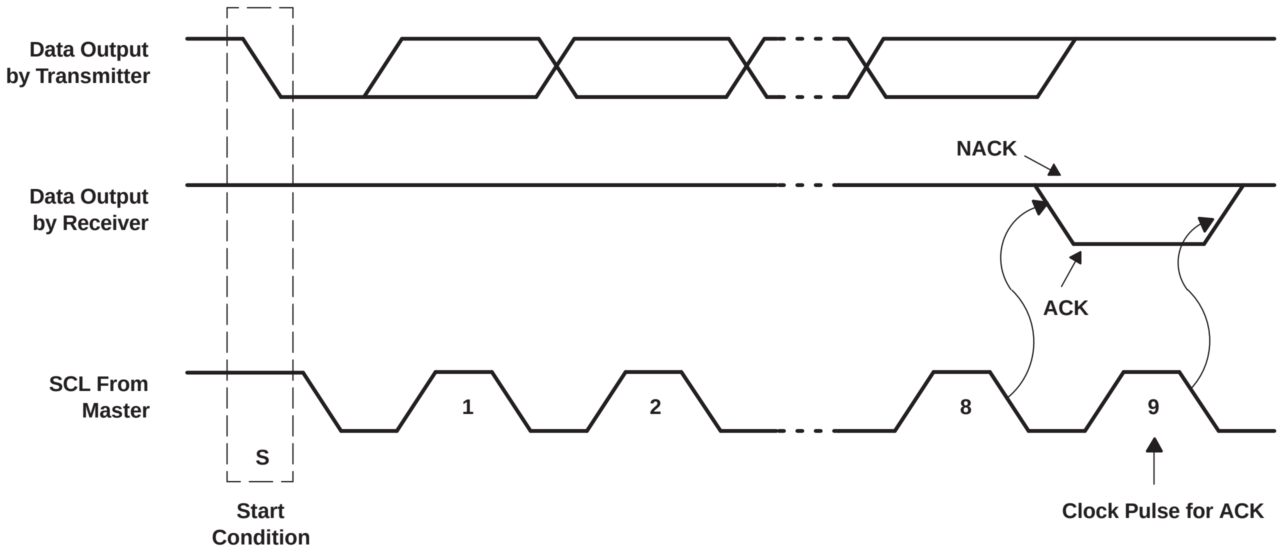


Figure 7. Acknowledgment on the I^{2}C Bus

A master receiver must signal an end of data to the transmitter by not generating an acknowledge (NACK) after the last byte has been clocked out of the slave. This is done by the master receiver by holding the SDA line high. In this event, the transmitter must release the data line to enable the master to generate a stop condition.

Data is transmitted to the PCA9545A control register using the write mode shown in Figure 8.

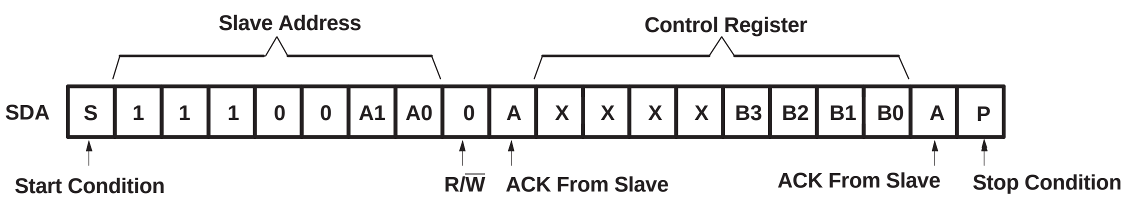


Figure 8. Write Control Register

Data is read from the PCA9545A control register using the read mode shown in Figure 9.

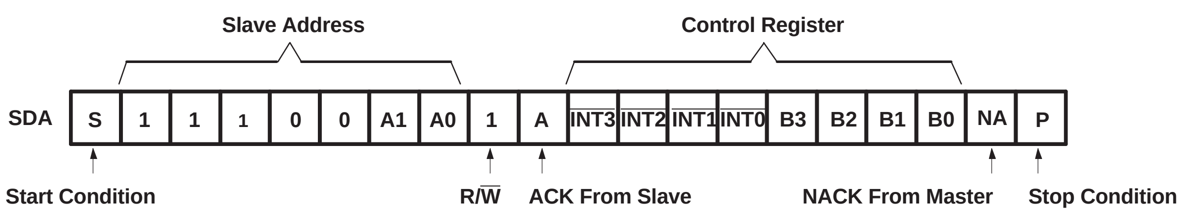


Figure 9. Read Control Register

Absolute Maximum Ratings[1]

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{CC}	Supply voltage range		–0.5	7	V
V_I	Input voltage range[2]		–0.5	7	V
I_I	Input current			±20	mA
I_O	Output current			±25	mA
	Continuous current through V_{CC}			±100	mA
	Continuous current through GND			±100	mA
θ_{JA}	Package thermal impedance[3]	DGV package		92	°C/W
		DW package		58	
		GQN/ZQN package		78	
		PW package		83	
		RGW package		TBD	
		RGY package		47	
P_{tot}	Total power dissipation			400	mW
T_{stg}	Storage temperature range		–65	150	°C
T_A	Operating free-air temperature range		–40	85	°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
(3) The package thermal impedance is calculated in accordance with JESD 51-7.

Recommended Operating Conditions[1]

			MIN	MAX	UNIT
V_{CC}	Supply voltage		2.3	5.5	V
V_{IH}	High-level input voltage	SCL, SDA	$0.7 \times V_{CC}$	6	V
		A1, A0, $\overline{\text{INT3}}$–$\overline{\text{INT0}}$, $\overline{\text{RESET}}$	$0.7 \times V_{CC}$	$V_{CC} + 0.5$	
V_{IL}	Low-level input voltage	SCL, SDA	–0.5	$0.3 \times V_{CC}$	V
		A1, A0, $\overline{\text{INT3}}$–$\overline{\text{INT0}}$, $\overline{\text{RESET}}$	–0.5	$0.3 \times V_{CC}$	
T_A	Operating free-air temperature		–40	85	°C

(1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS	V_{CC}	MIN	TYP(1)	MAX	UNIT
V_{POR}	Power-on reset voltage(2)		No load, $V_I = V_{CC}$ or GND	V_{POR}		1.6	2.1	V
V_{pass}	Switch output voltage		$V_{SWin} = V_{CC}$, I_{SWout} = –100 µA	5 V		3.6		V
				4.5 V to 5.5 V	2.6		4.5	
				3.3 V		1.9		
				3 V to 3.6 V	1.6		2.8	
				2.5 V		1.5		
				2.3 V to 2.7 V	1.1		2	
I_{OH}	$\overline{INT}$		$V_O = V_{CC}$	2.3 V to 5.5 V			10	µA
I_{OL}	SCL, SDA		V_{OL} = 0.4 V	2.3 V to 5.5 V	3	7		mA
			V_{OL} = 0.6 V		6	10		
	$\overline{INT}$		V_{OL} = 0.4 V		3			
I_I	SCL, SDA		$V_I = V_{CC}$ or GND	2.3 V to 5.5 V			±1	µA
	SC3–SC0, SD3–SD0						±1	
	A1, A0						±1	
	$\overline{INT3}$–$\overline{INT0}$						±1	
	$\overline{RESET}$						±1	
I_{CC}	Operating mode	f_{SCL} = 100 kHz	$V_I = V_{CC}$ or GND, $I_O = 0$	5.5 V		3	12	µA
				3.6 V		3	11	
				2.7 V		3	10	
	Standby mode	Low inputs	V_I = GND, $I_O = 0$	5.5 V		0.3	1	
				3.6 V		0.1	1	
				2.7 V		0.1	1	
		High inputs	$V_I = V_{CC}$, $I_O = 0$	5.5 V		0.3	1	
				3.6 V		0.1	1	
				2.7 V		0.1	1	
ΔI_{CC}	Supply-current change	$\overline{INT3}$–$\overline{INT0}$	One $\overline{INT3}$–$\overline{INT0}$ input at 0.6 V, Other inputs at V_{CC} or GND	2.3 V to 5.5 V		8	15	µA
			One $\overline{INT3}$–$\overline{INT0}$ input at V_{CC} – 0.6 V, Other inputs at V_{CC} or GND			8	15	
		SCL, SDA	SCL or SDA input at 0.6 V, Other inputs at V_{CC} or GND			8	15	
			SCL or SDA input at V_{CC} – 0.6 V, Other inputs at V_{CC} or GND			8	15	
C_i	A1, A0		$V_I = V_{CC}$ or GND	2.3 V to 5.5 V		4.5	6	pF
	$\overline{INT3}$–$\overline{INT0}$					4.5	6	
	$\overline{RESET}$					4.5	5.5	
$C_{io(OFF)}$(3)	SCL, SDA		$V_I = V_{CC}$ or GND, Switch OFF	2.3 V to 5.5 V		15	19	pF
	SC3–SC0, SD3–SD0					6	8	
R_{ON}	Switch on-state resistance		V_O = 0.4 V, I_O = 15 mA	4.5 V to 5.5 V	4	9	16	Ω
				3 V to 3.6 V	5	11	20	
			V_O = 0.4 V, I_O = 10 mA	2.3 V to 2.7 V	7	16	45	

(1) All typical values are at nominal supply voltage (2.5-V, 3.3-V, or 5-V V_{CC}), T_A = 25°C.
(2) The power-on reset circuit resets the I²C bus logic with $V_{CC} < V_{POR}$. V_{CC} must be lowered to 0.2 V to reset the device.
(3) $C_{io(ON)}$ depends on the device capacitance and load that is downstream from the device.

I²C Interface Timing Requirements

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 10)

			STANDARD MODE I²C BUS		FAST MODE I²C BUS		UNIT
			MIN	MAX	MIN	MAX	
f_{scl}	I²C clock frequency		0	100	0	400	kHz
t_{sch}	I²C clock high time		4		0.6		µs
t_{scl}	I²C clock low time		4.7		1.3		µs
t_{sp}	I²C spike time			50		50	ns
t_{sds}	I²C serial-data setup time		250		100		ns
t_{sdh}	I²C serial-data hold time		0(1)		0(1)		µs
t_{icr}	I²C input rise time			1000	$20 + 0.1C_b$(2)	300	ns
t_{icf}	I²C input fall time			300	$20 + 0.1C_b$(2)	300	ns
t_{ocf}	I²C output fall time	10-pF to 400-pF bus		300	$20 + 0.1C_b$(2)	300	ns
t_{buf}	I²C bus free time between stop and start		4.7		1.3		µs
t_{sts}	I²C start or repeated start condition setup		4.7		0.6		µs
t_{sth}	I²C start or repeated start condition hold		4		0.6		µs
t_{sps}	I²C stop condition setup		4		0.6		µs
$t_{vdL(Data)}$	Valid-data time (high to low)(3)	SCL low to SDA output low valid		1		1	µs
$t_{vdH(Data)}$	Valid-data time (low to high)(3)	SCL low to SDA output high valid		0.6		0.6	µs
$t_{vd(ack)}$	Valid-data time of ACK condition	ACK signal from SCL low to SDA output low		1		1	µs
C_b	I²C bus capacitive load			400		400	pF

(1) A device internally must provide a hold time of at least 300 ns for the SDA signal (referred to as the V_{IH} min of the SCL signal), in order to bridge the undefined region of the falling edge of SCL.
(2) C_b = total bus capacitance of one bus line in pF
(3) Data taken using a 1-kΩ pullup resistor and 50-pF load (see Figure 10)

Switching Characteristics

over recommended operating free-air temperature range, $C_L \le 100$ pF (unless otherwise noted) (see Figure 12)

PARAMETER			FROM (INPUT)	TO (OUTPUT)	MIN	MAX	UNIT
t_{pd}(1)	Propagation delay time	$R_{ON} = 20\ \Omega$, $C_L = 15$ pF	SDA or SCL	SDn or SCn		0.3	ns
		$R_{ON} = 20\ \Omega$, $C_L = 50$ pF				1	
t_{iv}	Interrupt valid time(2)		$\overline{INTn}$	$\overline{INT}$		4	µs
t_{ir}	Interrupt reset delay time(2)		$\overline{INTn}$	$\overline{INT}$		2	µs

(1) The propagation delay is the calculated RC time constant of the typical ON-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).
(2) Data taken using a 4.7-kΩ pullup resistor and 100-pF load (see Figure 12)

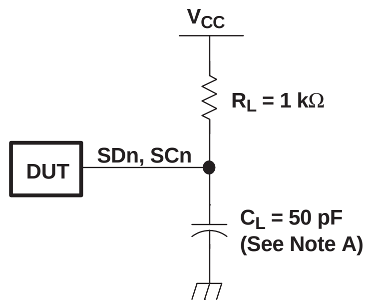
Interrupt and Reset Timing Requirements

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 12)

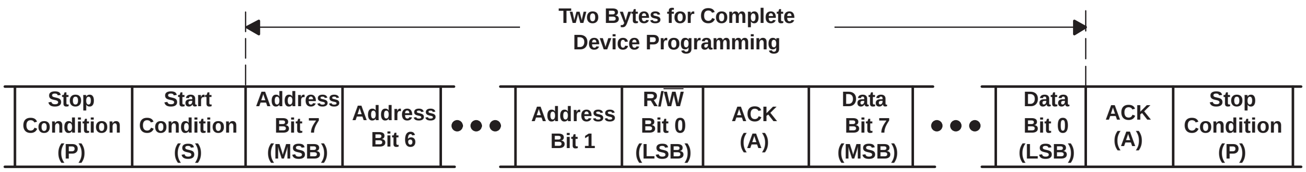
PARAMETER		MIN	MAX	UNIT
t_{PWRL}	Low-level pulse duration rejection of $\overline{\text{INTn}}$ inputs	1		µs
t_{PWRH}	High-level pulse duration rejection of $\overline{\text{INTn}}$ inputs	0.5		µs
t_{WL}	Pulse duration, $\overline{\text{RESET}}$ low	6		ns
t_{rst} (1)	$\overline{\text{RESET}}$ time (SDA clear)		500	ns
$t_{REC(STA)}$	Recovery time from $\overline{\text{RESET}}$ to start	0		ns

(1) t_{rst} is the propagation delay measured from the time the $\overline{\text{RESET}}$ pin is first asserted low to the time the SDA pin is asserted high, signaling a stop condition. It must be a minimum of t_{WL}.

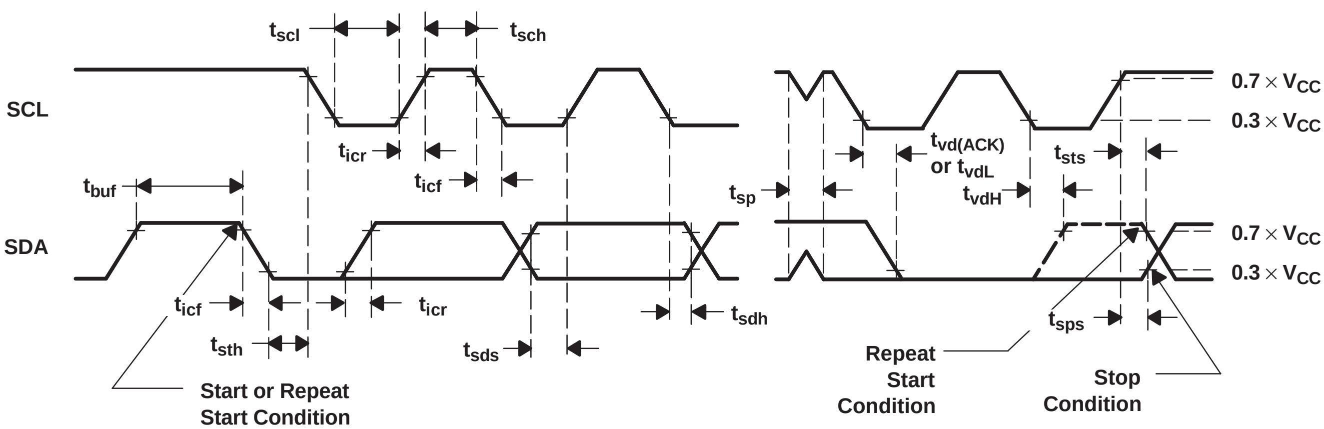
PARAMETER MEASUREMENT INFORMATION



I^2C PORT LOAD CONFIGURATION



BYTE	DESCRIPTION
1	I^2C address + R/$\overline{W}$
2	Control register data



VOLTAGE WAVEFORMS

A. C_L includes probe and jig capacitance.

B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r/t_f = 30 ns.

C. The outputs are measured one at a time, with one transition per measurement.

Figure 10. I^2C Interface Load Circuit, Byte Descriptions, and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION (continued)

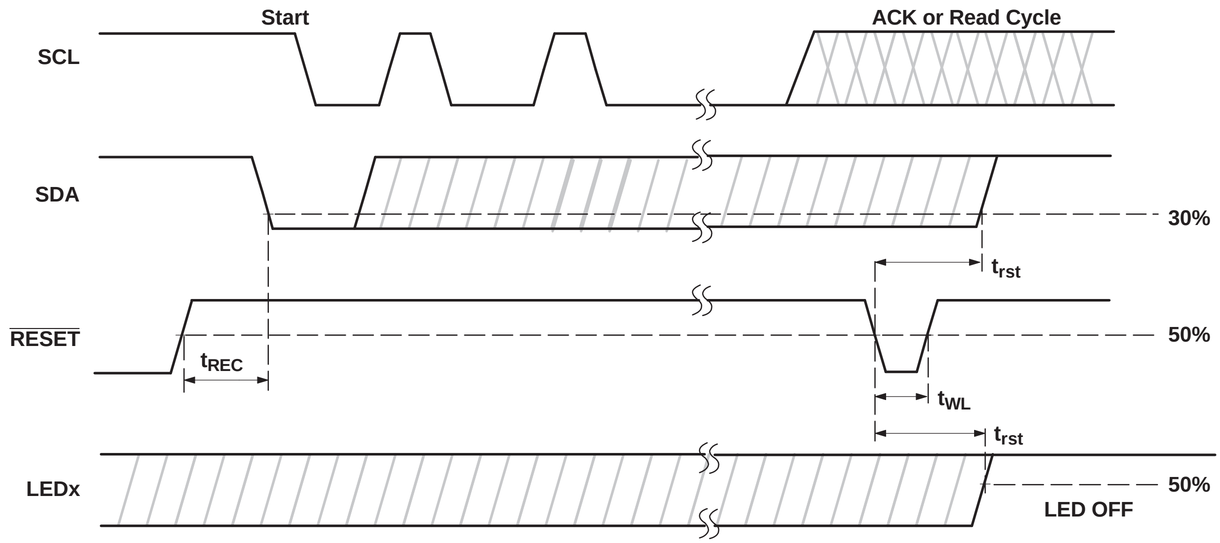
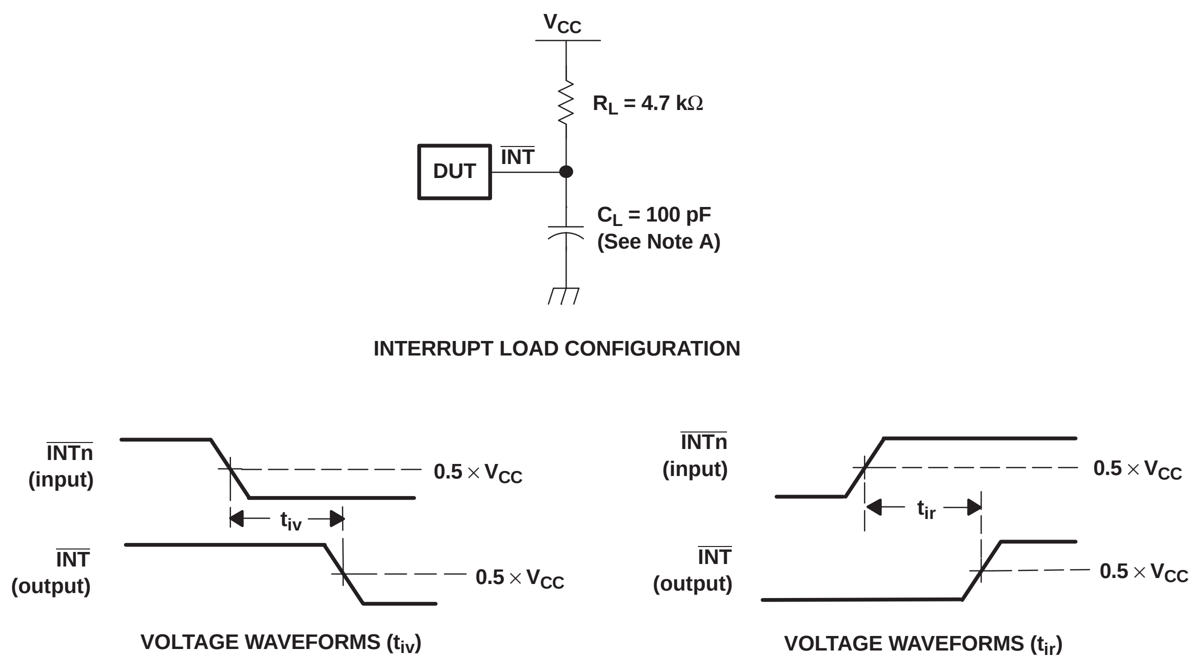


Figure 11. Reset Timing



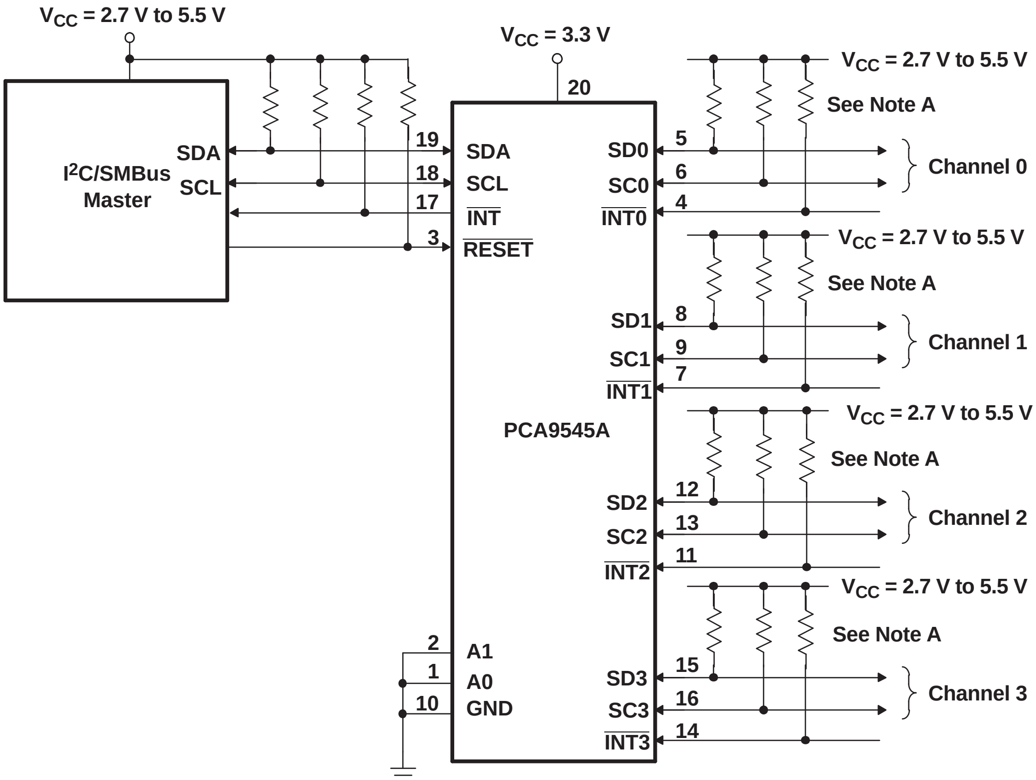
A. C_L includes probe and jig capacitance.

B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r/t_f = 30 ns.

Figure 12. Interrupt Load Circuit and Voltage Waveforms

APPLICATION INFORMATION

Figure 13 shows an application in which the PCA9545A can be used.



A. If the device generating the interrupt has an open-drain output structure or can be 3-stated, a pullup resistor is required. If the device generating the interrupt has a totem-pole output structure and cannot be 3-stated, a pullup resistor is not required. The interrupt inputs should not be left floating.

B. Pin numbers shown are for DGV, DW, PW, and RGY packages.

Figure 13. Typical Application

PACKAGING INFORMATION

Orderable Device	Status [1]	Package Type	Package Drawing	Pins	Package Qty	Eco Plan [2]	Lead/Ball Finish	MSL Peak Temp [3]
PCA9545ADGVR	ACTIVE	TVSOP	DGV	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
PCA9545ADGVT	PREVIEW	TVSOP	DGV	20	250	TBD	Call TI	Call TI
PCA9545ADW	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
PCA9545ADWR	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
PCA9545ADWT	PREVIEW	SOIC	DW	20	250	TBD	Call TI	Call TI
PCA9545AGQNR	NRND	BGA MI CROSTA R JUNI OR	GQN	20	1000	TBD	SNPB	Level-1-240C-UNLIM
PCA9545APW	ACTIVE	TSSOP	PW	20	70	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
PCA9545APWE4	ACTIVE	TSSOP	PW	20	70	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
PCA9545APWR	ACTIVE	TSSOP	PW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
PCA9545APWRE4	ACTIVE	TSSOP	PW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
PCA9545APWT	ACTIVE	TSSOP	PW	20	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
PCA9545APWTE4	ACTIVE	TSSOP	PW	20	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
PCA9545ARGWR	PREVIEW	QFN	RGW	20	3000	TBD	Call TI	Call TI
PCA9545ARGYR	ACTIVE	QFN	RGY	20	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1YEAR
PCA9545ARGYRG4	ACTIVE	QFN	RGY	20	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1YEAR
PCA9545AZQNR	ACTIVE	BGA MI CROSTA R JUNI OR	ZQN	20	1000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM

[1] The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

[2] Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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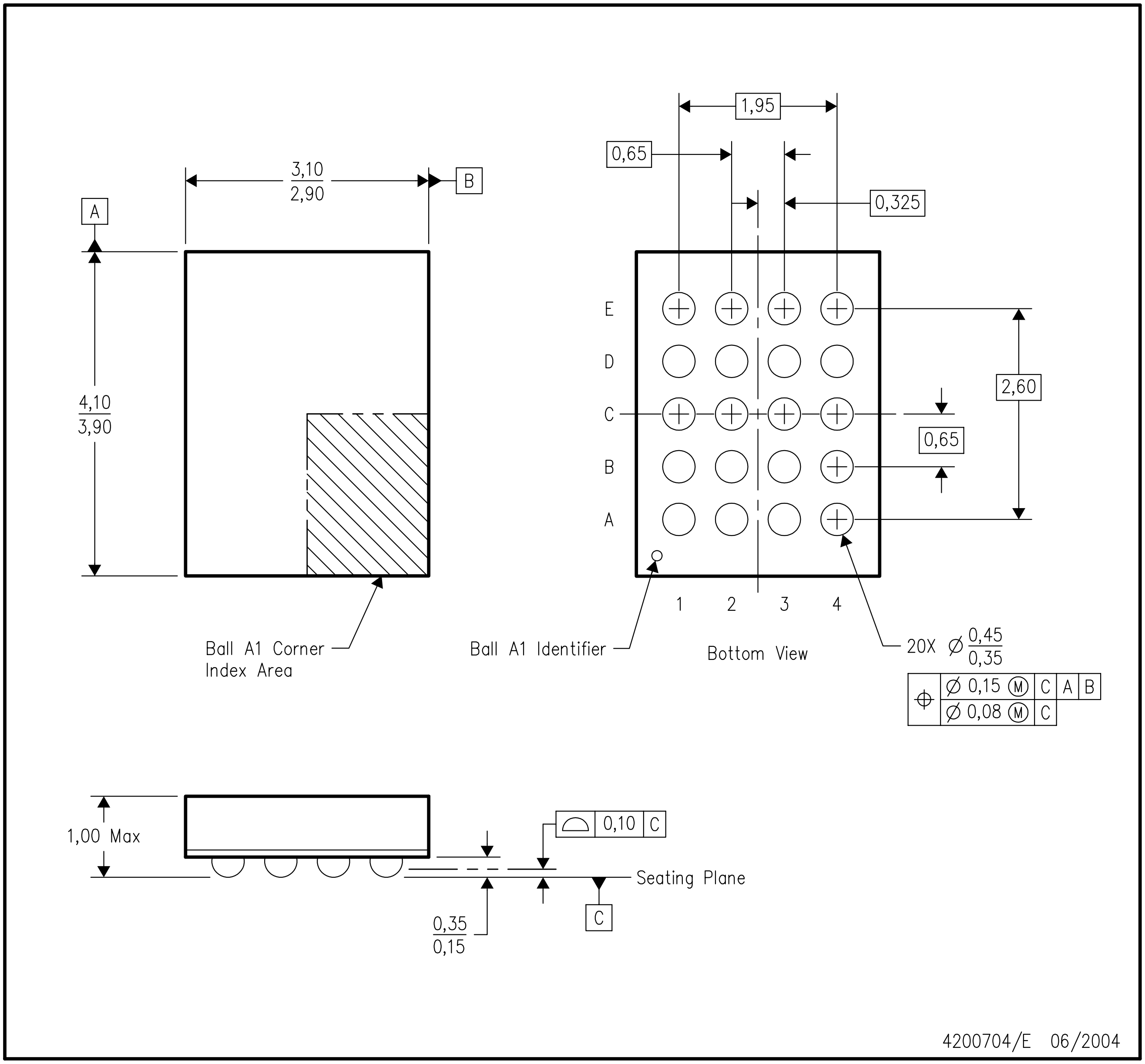
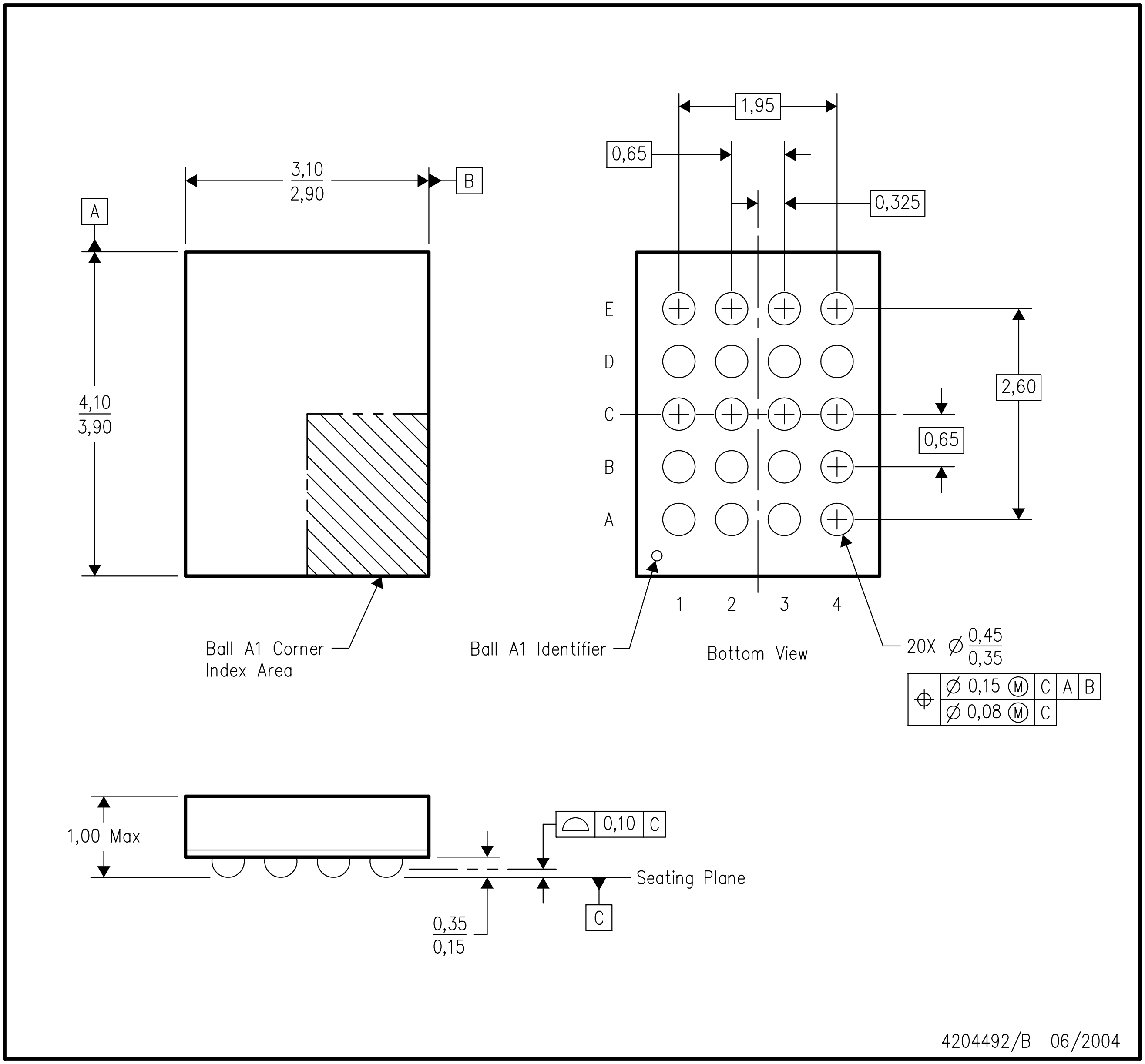
GQN (R-PBGA-N20) PLASTIC BALL GRID ARRAY



NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Falls within JEDEC MO-225 variation BC.
- D. This package is tin-lead (SnPb). Refer to the 20 ZQN package (drawing 4204492) for lead-free.

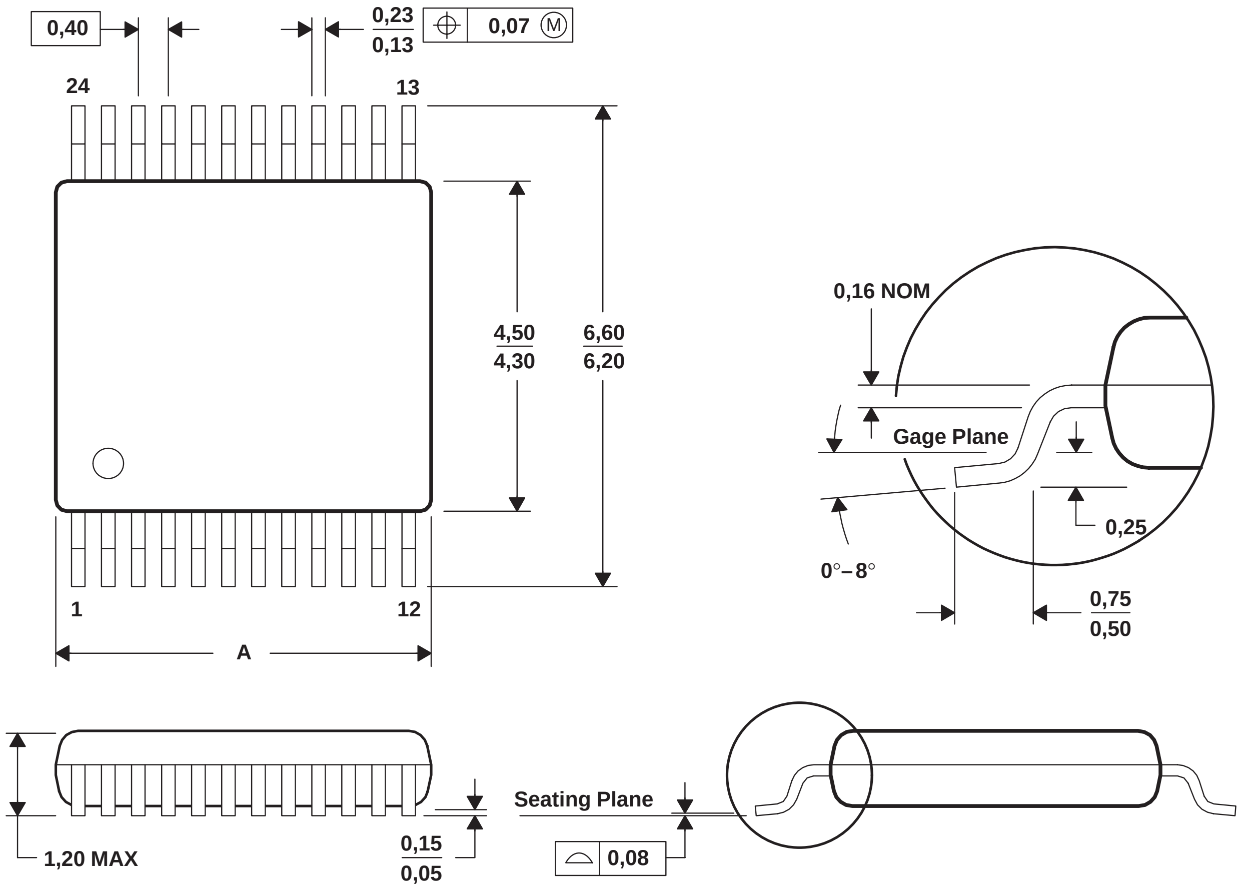
ZQN (R–PBGA–N20) PLASTIC BALL GRID ARRAY



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Falls within JEDEC MO–225 variation BC.
D. This package is lead–free. Refer to the 20 GQN package (drawing 4200704) for tin–lead (SnPb).

DGV (R-PDSO-G)** **PLASTIC SMALL-OUTLINE**

24 PINS SHOWN



PINS ** / DIM	14	16	20	24	38	48	56
A MAX	3,70	3,70	5,10	5,10	7,90	9,80	11,40
A MIN	3,50	3,50	4,90	4,90	7,70	9,60	11,20

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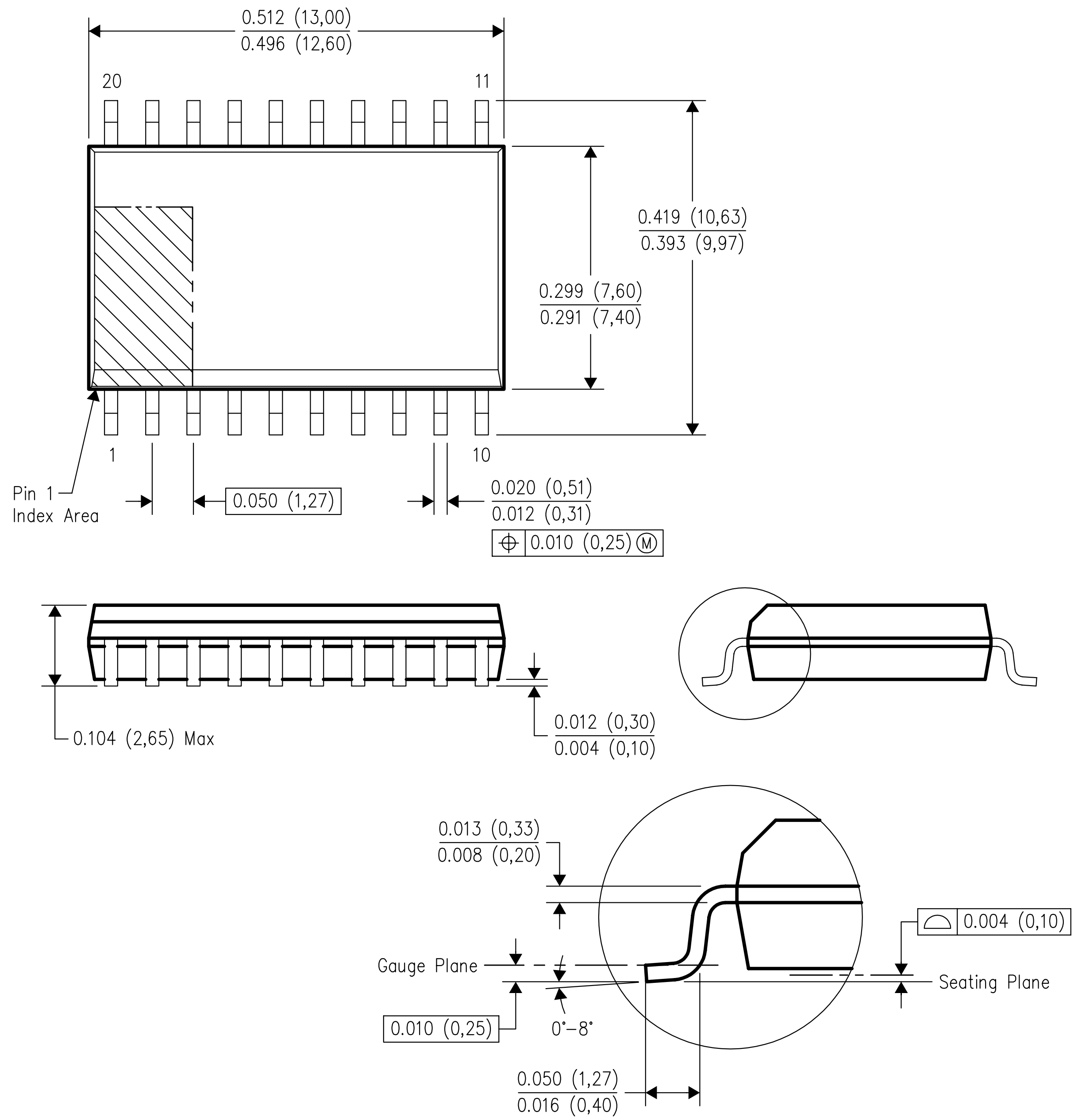
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.
D. Falls within JEDEC: 24/48 Pins – MO-153
14/16/20/56 Pins – MO-194

DW (R-PDSO-G20) PLASTIC SMALL-OUTLINE PACKAGE



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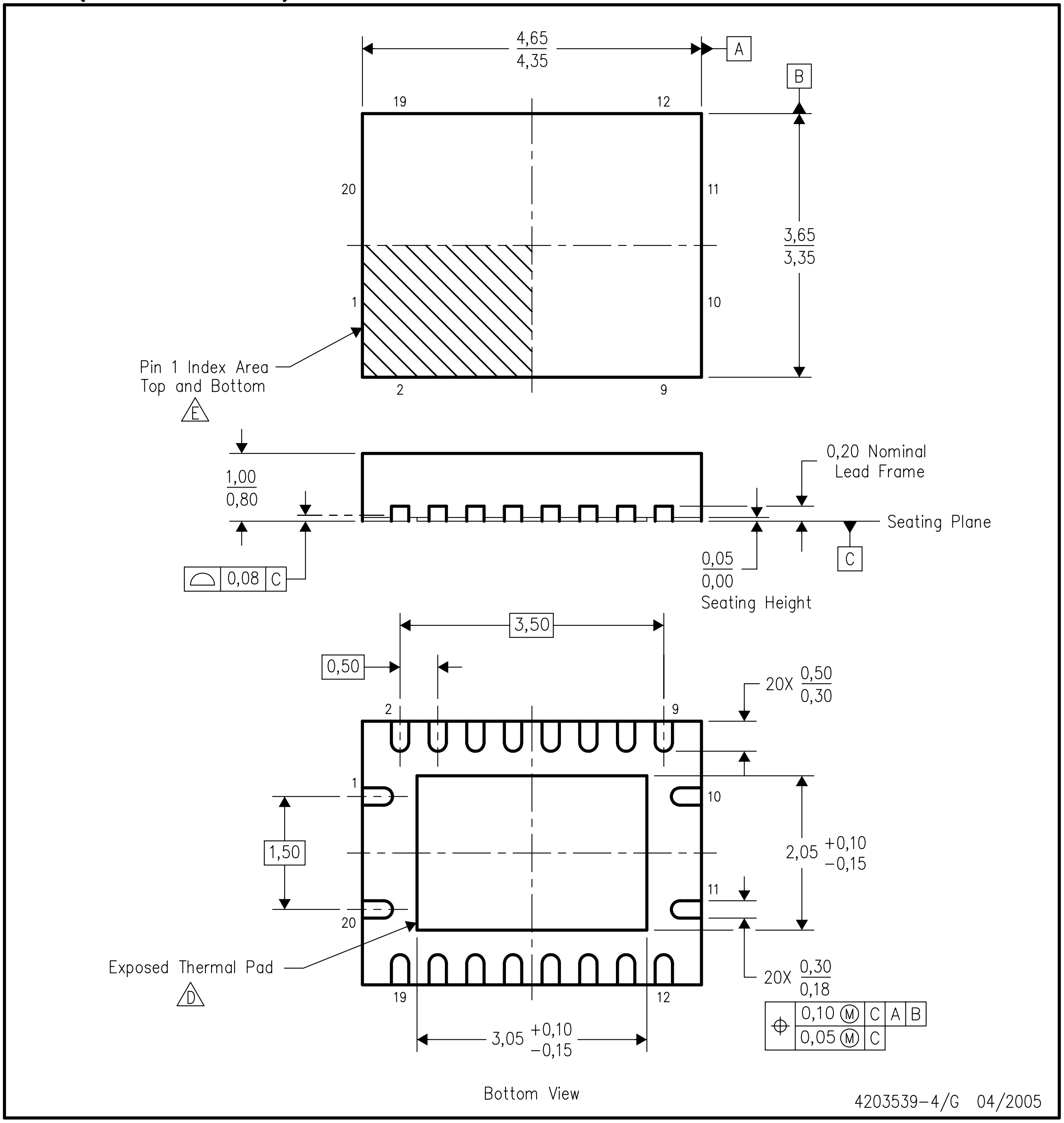
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
D. Falls within JEDEC MS-013 variation AC.

RGY (R–PQFP–N20) PLASTIC QUAD FLATPACK



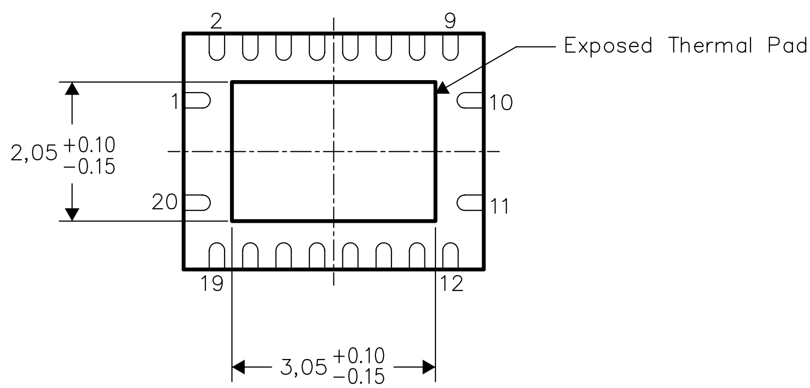
NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. QFN (Quad Flatpack No–Lead) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. Pin 1 identifiers are located on both top and bottom of the package and within the zone indicated. The Pin 1 identifiers are either a molded, marked, or metal feature.
F. Package complies to JEDEC MO–241 variation BC.

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB), the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to a ground plane or special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, Quad Flatpack No–Lead Logic Packages, Texas Instruments Literature No. SCBA017. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.

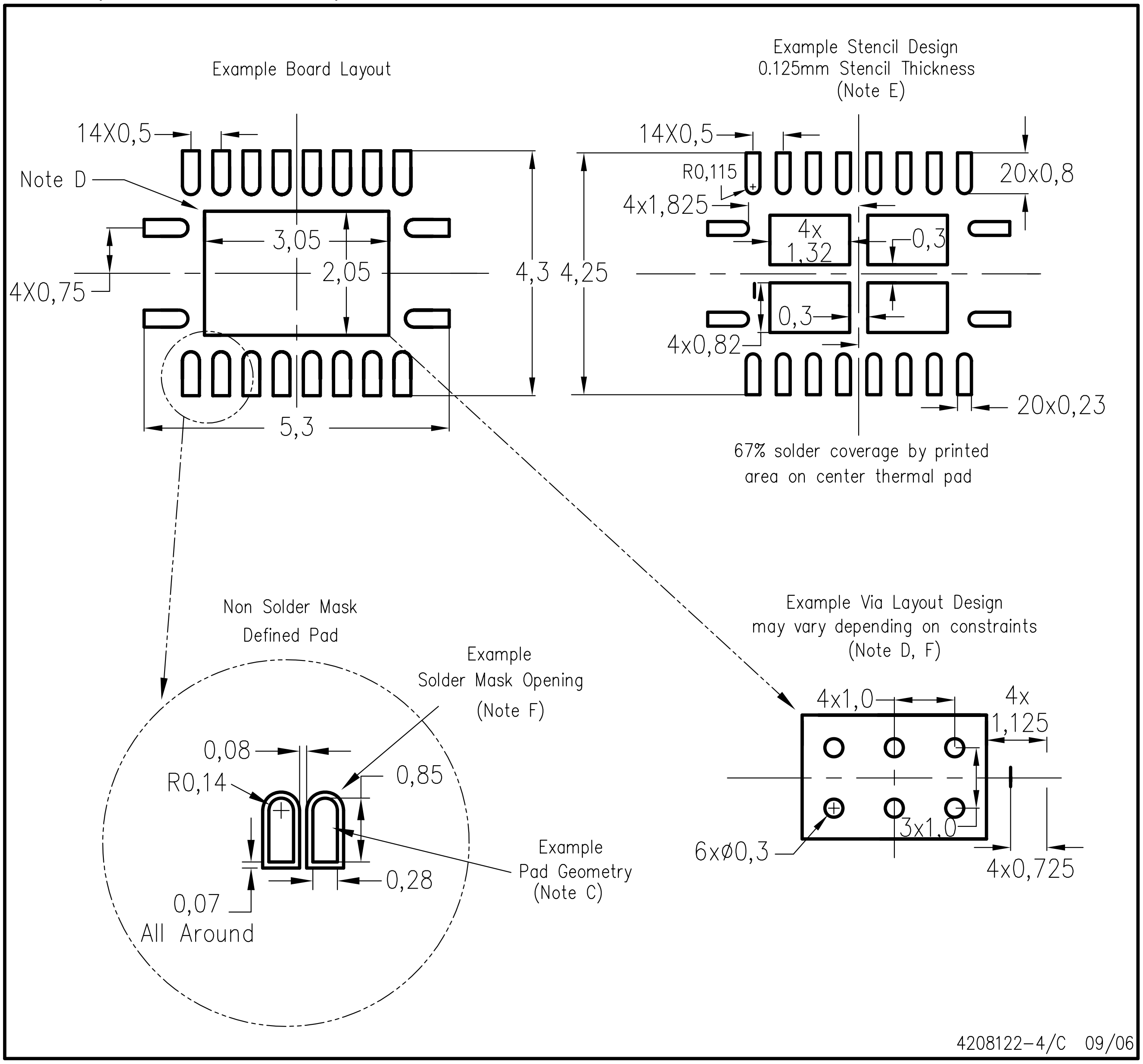


Bottom View

NOTE: All linear dimensions are in millimeters

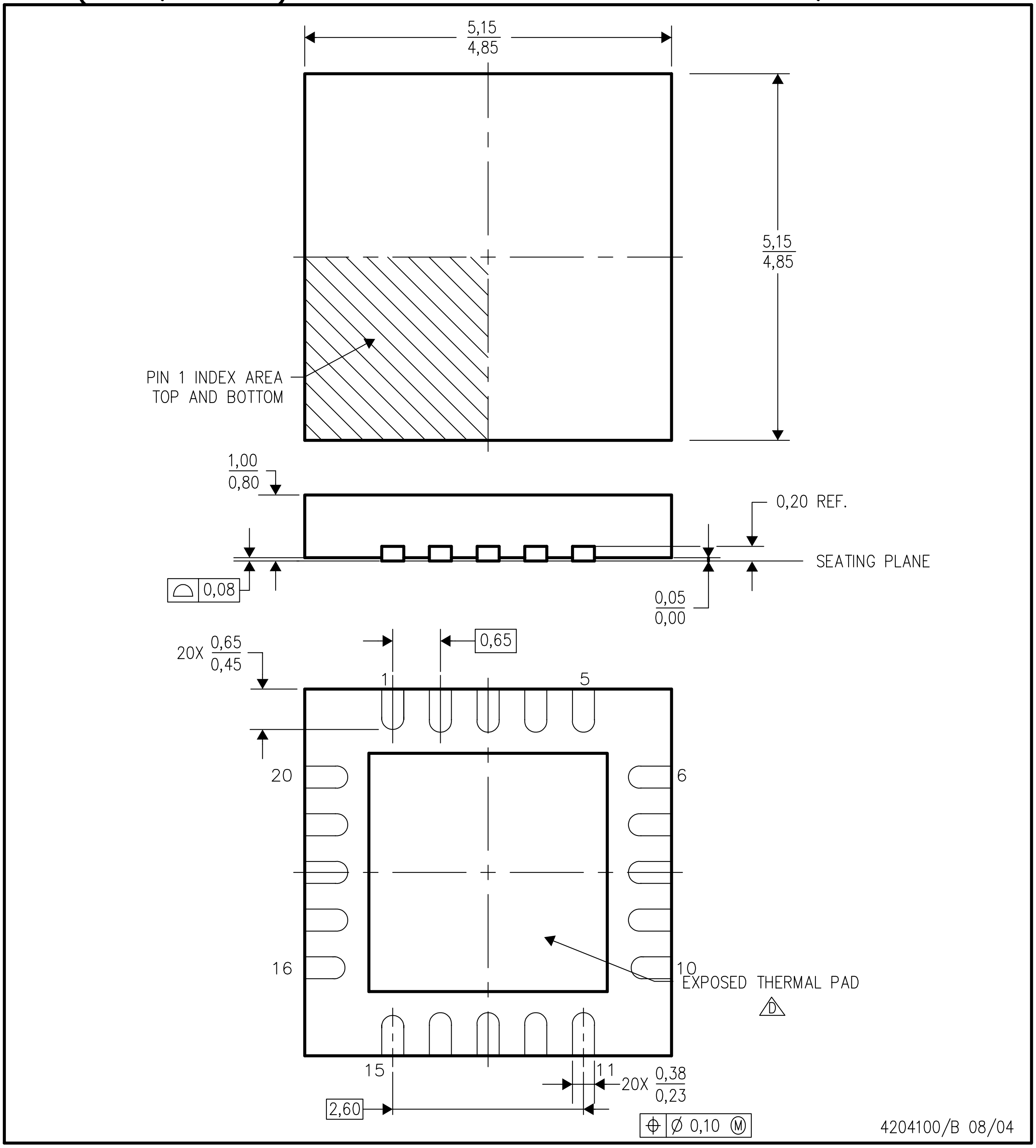
Exposed Thermal Pad Dimensions

RGY (R–PQFP–N20)



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack Packages, Texas Instruments Literature No. SCBA017, SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http: //www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.

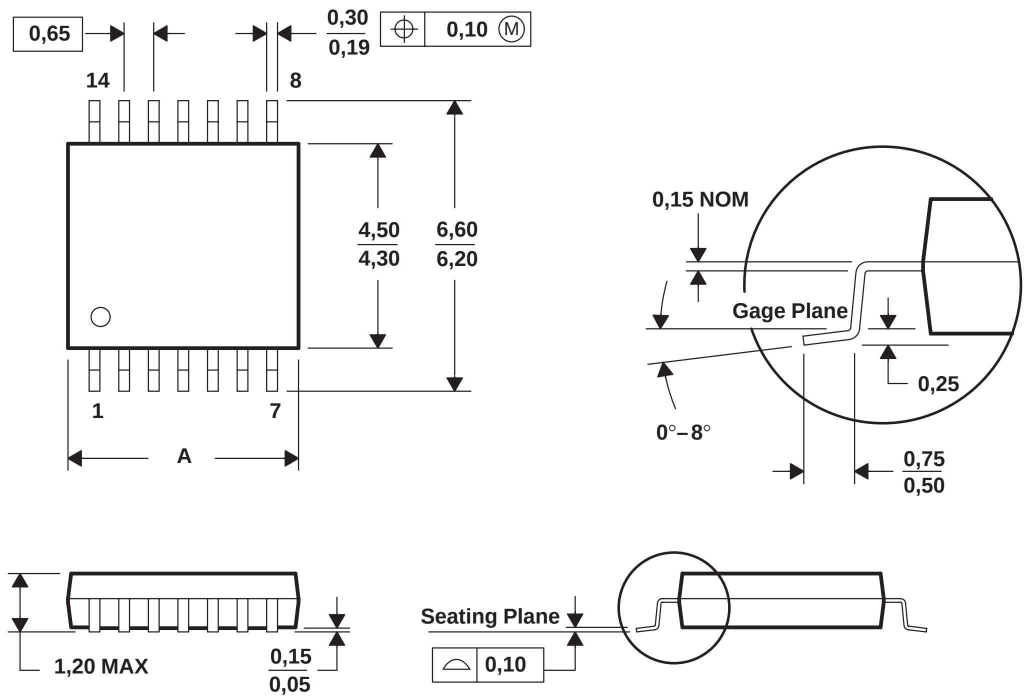
RGW (S-PQFP-N20) PLASTIC QUAD FLATPACK



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5–1994.
B. This drawing is subject to change without notice.
C. Quad Flat pack, No-leads (QFN) package configuration
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.
E. Falls within JEDEC MO-220.

PW (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14 PINS SHOWN



PINS ** / DIM	8	14	16	20	24	28
A MAX	3,10	5,10	5,10	6,60	7,90	9,80
A MIN	2,90	4,90	4,90	6,40	7,70	9,60

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NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. Falls within JEDEC MO-153

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