DESCRIPTION

The 87C54/87C58 Single-Chip 8-Bit Microcontroller is manufactured in an advanced CMOS process and is a derivative of the 80C51 microcontroller family. The 87C54/87C58 has the same instruction set as the 80C51.

This device provides architectural enhancements that make it applicable in a variety of applications for general control systems. The 87C58 contains 32k × 8 EPROM memory, and the 87C54 contains 16k × 8 EPROM memory, a volatile 256 × 8 read/write data memory, four 8-bit I/O ports, three 16-bit timer/event counters, a multi-source, two-priority-level, nested interrupt structure, an enhanced UART and on-chip oscillator and timing circuits. For systems that require extra capability, the 87C54/87C58 can be expanded using standard TTL compatible memories and logic.

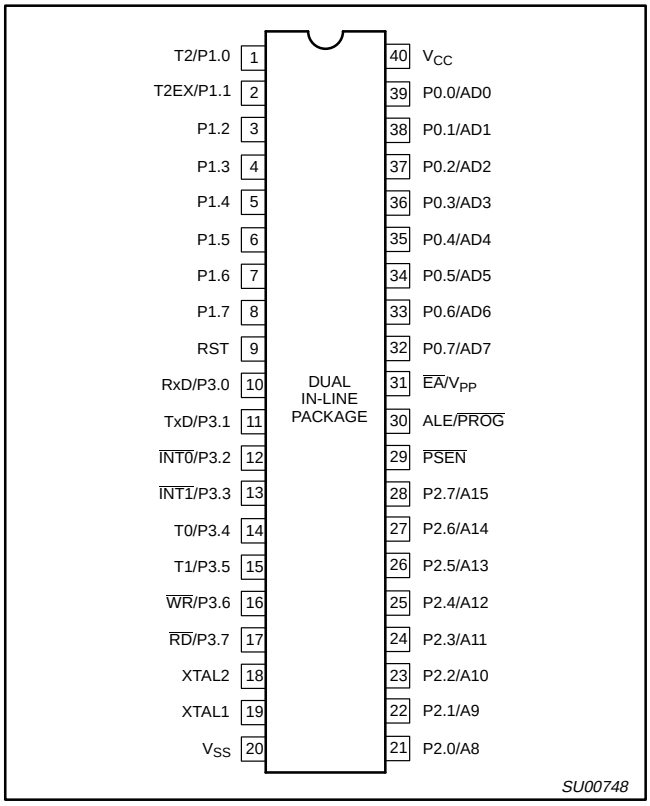
Its added features make it an even more powerful microcontroller for applications that require pulse width modulation, high-speed I/O and up/down counting capabilities such as motor control. It also has a more versatile serial channel that facilitates multiprocessor communications.

See 80C52/54/58 datasheet for ROM device specification.

FEATURES

- 80C51 central processing unit
- 16k × 8 EPROM expandable externally to 64k bytes (87C54)
- 16k × 8 EPROM (87C54) and
  32k × 8 EPROM expandable externally to 64k bytes (87C58)
  - Improved Quick Pulse programming algorithm
  - Two level program security system
  - 32 byte encryption array
- 256 × 8 RAM, expandable externally to 64k bytes
- Three 16-bit timer/counters
  - T2 is an up/down counter
- Four 8-bit I/O ports
- Full-duplex enhanced UART
  - Framing error detection
  - Automatic address recognition
- Power control modes
  - Idle mode
  - Power-down mode
- Once (On Circuit Emulation) Mode
- Five package styles
- OTP package available
- Programmable clock out
- 6 interrupt sources
- 2 level priority

PIN CONFIGURATIONS

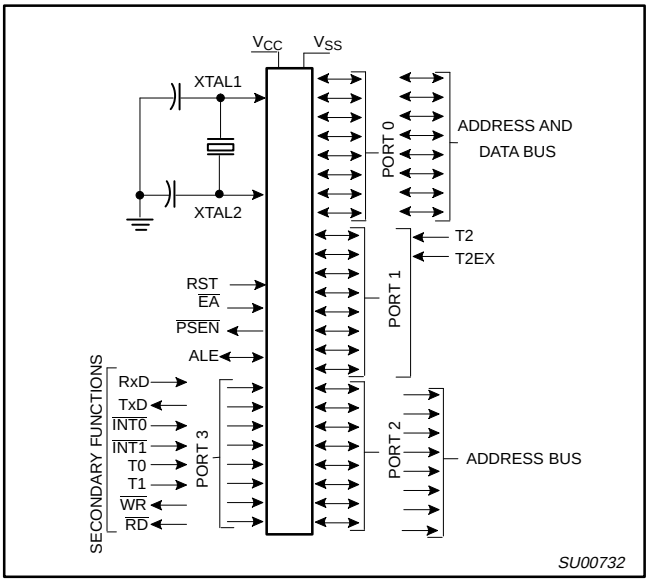


ORDERING INFORMATION

16k × 8 EPROM[1]	32k × 8 EPROM[1]		TEMPERATURE RANGE °C AND PACKAGE	FREQUENCY	DRAWING NUMBER
P87C54EBP N	P87C58EBP N	OTP	0 to +70, 40-Pin Plastic Dual In-line Package	16MHz	SOT129-1
P87C54EBF FA	P87C58EBF FA	UV	0 to +70, 40-Pin Ceramic Dual In-line Package w/Window	16MHz	0590B
P87C54EBA A	P87C58EBA A	OTP	0 to +70, 44-Pin Plastic Leaded Chip Carrier	16MHz	SOT187-2
P87C54EBL KA	P87C58EBL KA	UV	0 to +70, 44-Pin Ceramic Leaded Chip Carrier w/Window	16MHz	1472A
P87C54EBB B	P87C58EBB B	OTP	0 to +70, 44-Pin Plastic Quad Flat Pack	16MHz	SOT307-2
P87C54EFP N	P87C58EFP N	OTP	–40 to +85, 40-Pin Plastic Dual In-line Package	16MHz	SOT129-1
P87C54EFF FA	P87C58EFF FA	UV	–40 to +85, 40-Pin Ceramic Dual In-line Package w/Window	16MHz	0590B
P87C54EFA A	P87C58EFA A	OTP	–40 to +85, 44-Pin Plastic Leaded Chip Carrier	16MHz	SOT187-2
P87C54EFB B	P87C58EFB B	OTP	–40 to +85, 44-Pin Plastic Quad Flat Pack	16MHz	SOT307-2
P87C54IBP N	P87C58IBP N	OTP	0 to +70, 40-Pin Plastic Dual In-line Package	24MHz	SOT129-1
P87C54IBF FA	P87C58IBF FA	UV	0 to +70, 40-Pin Ceramic Dual In-line Package w/Window	24MHz	0590B
P87C54IBA A	P87C58IBA A	OTP	0 to +70, 44-Pin Plastic Leaded Chip Carrier	24MHz	SOT187-2
P87C54IBL KA	P87C58IBL KA	UV	0 to +70, 44-Pin Ceramic Leaded Chip Carrier w/Window	24MHz	1472A
P87C54IBB B	P87C58IBB B	OTP	0 to +70, 44-Pin Plastic Quad Flat Pack	24MHz	SOT307-2
P87C54IFP N	P87C58IFP N	OTP	–40 to +85, 40-Pin Plastic Dual In-line Package	24MHz	SOT129-1
P87C54IFF FA	P87C58IFF FA	UV	–40 to +85, 40-Pin Ceramic Dual In-line Package w/Window	24MHz	0590B
P87C54IFA A	P87C58IFA A	OTP	–40 to +85, 44-Pin Plastic Leaded Chip Carrier	24MHz	SOT187-2
P87C54IFB B	P87C58IFB B	OTP	–40 to +85, 44-Pin Plastic Quad Flat Pack	24MHz	SOT307-2

NOTE:
1. OTP = One Time Programmable EPROM. UV = Erasable EPROM.

LOGIC SYMBOL



BLOCK DIAGRAM

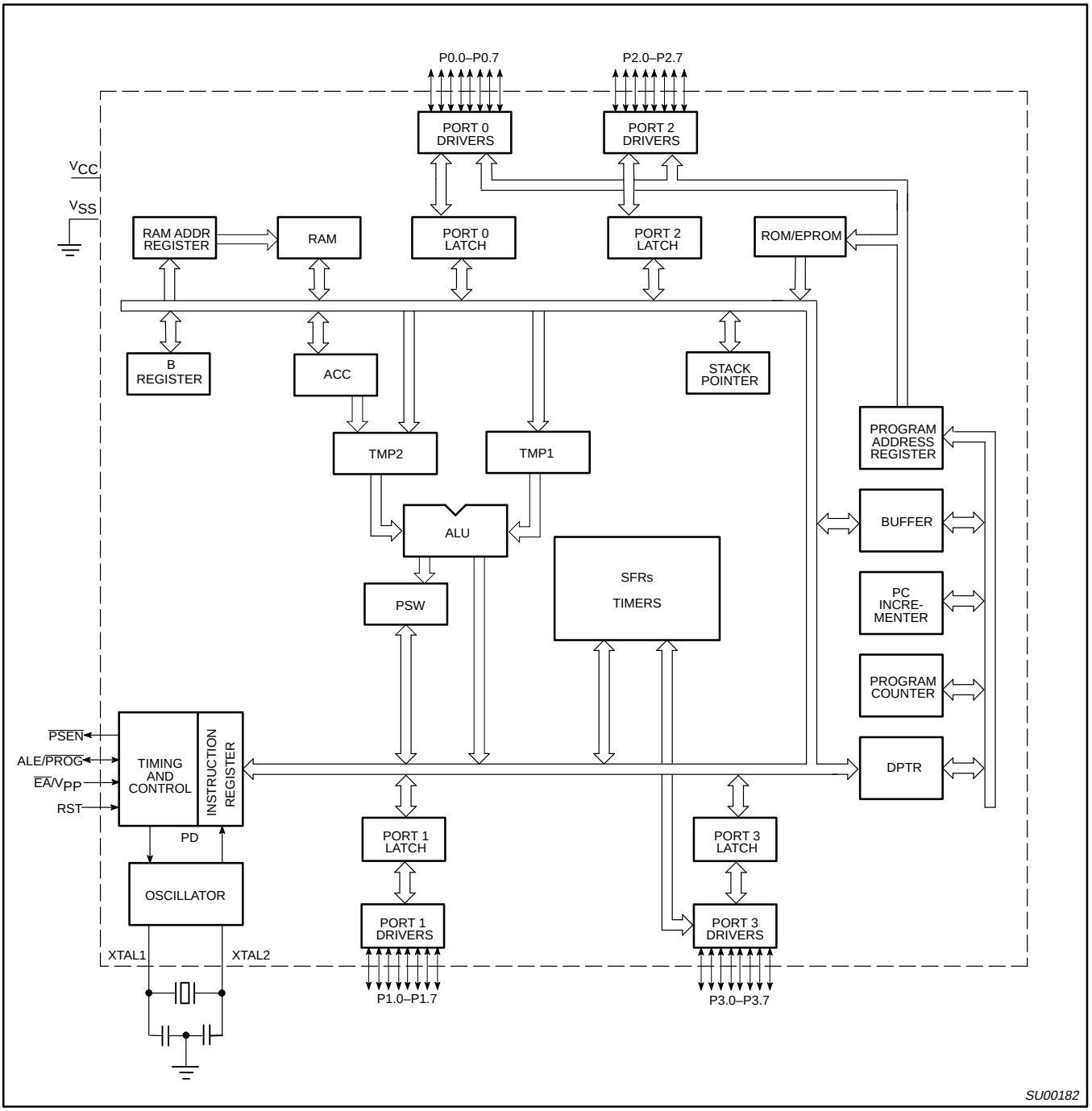
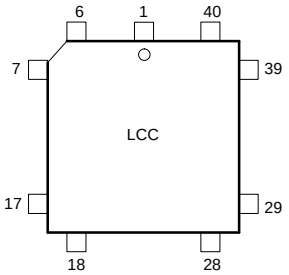


Table 1. 87C54/87C58 Special Function Registers

SYMBOL	DESCRIPTION	DIRECT ADDRESS	BIT ADDRESS, SYMBOL, OR ALTERNATIVE PORT FUNCTION MSB							LSB	RESET VALUE
ACC*	Accumulator	E0H	E7	E6	E5	E4	E3	E2	E1	E0	00H
AUXR#	Auxiliary	8EH	–	–	–	–	–	–	–	AO	xxxxxxx0B
B*	B register	F0H	F7	F6	F5	F4	F3	F2	F1	F0	00H
DPTR:	Data Pointer (2 bytes)										
DPH	Data Pointer High	83H									00H
DPL	Data Pointer Low	82H									00H
			AF	AE	AD	AC	AB	AA	A9	A8	
IE*	Interrupt Enable	A8H	EA	–	ET2	ES	ET1	EX1	ET0	EX0	00H
			BF	BE	BD	BC	BB	BA	B9	B8	
IP*	Interrupt Priority	B8H	–	–	PT2	PS	PT1	PX1	PT0	PX0	x0000000B
			87	86	85	84	83	82	81	80	
P0*	Port 0	80H	AD7	AD6	AD5	AD4	AD3	AD2	AD1	AD0	FFH
			97	96	95	94	93	92	91	90	
P1*	Port 1	90H	–	–	–	–	–	–	T2EX	T2	FFH
			A7	A6	A5	A4	A3	A2	A1	A0	
P2*	Port 2	A0H	AD15	AD14	AD13	AD12	AD11	AD10	AD9	AD8	FFH
			B7	B6	B5	B4	B3	B2	B1	B0	
P3*	Port 3	B0H	$\overline{RD}$	$\overline{WR}$	T1	T0	$\overline{INT1}$	$\overline{INT0}$	TxD	RxD	FFH
PCON#	Power Control	87H	SMOD1	SMOD0	–	POF[1]	GF1	GF0	PD	IDL	00xxxx00B
			D7	D6	D5	D4	D3	D2	D1	D0	
PSW*	Program Status Word	D0H	CY	AC	F0	RS1	RS0	OV	–	P	00H
RCAP2H#	Timer 2 Capture High	CBH									00H
RCAP2L#	Timer 2 Capture Low	CAH									00H
SADDR#	Slave Address	A9H									00H
SADEN#	Slave Address Mask	B9H									00H
SBUF	Serial Data Buffer	99H									xxxxxxxxB
			9F	9E	9D	9C	9B	9A	99	98	
SCON*	Serial Control	98H	SM0	SM1	SM2	REN	TB8	RB8	TI	RI	00H
SP	Stack Pointer	81H									07H
			8F	8E	8D	8C	8B	8A	89	88	
TCON*	Timer Control	88H	TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0	00H
			CF	CE	CD	CC	CB	CA	C9	C8	
T2CON#*	Timer 2 Control	C8H	TF2	EXF2	RCLK	TCLK	EXEN2	TR2	C/$\overline{T2}$	CP/$\overline{RL2}$	00H
TH0	Timer High 0	8CH									00H
TH1	Timer High 1	8DH									00H
TH2#	Timer High 2	CDH									00H
TL0	Timer Low 0	8AH									00H
TL1	Timer Low 1	8BH									00H
TL2#	Timer Low 2	CCH									00H
			C7	C6	C5	C4	C3	C2	C1	C0	
TMOD	Timer Mode	89H	GATE	C/T	M1	M0	GATE	C/T	M1	M0	00H
T2MOD#*	Timer 2 Mode Control	C9H	–	–	–	–	–	–	T2OE	DCEN	xxxxxx00B

* SFRs are bit addressable.
\# SFRs are modified from or added to the 80C51 SFRs.
1. Reset value depends on reset source.

CERAMIC AND PLASTIC LEADED CHIP CARRIER PIN FUNCTIONS

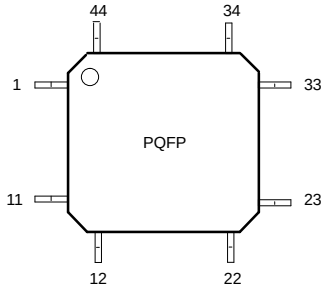


Pin	Function	Pin	Function	Pin	Function
1	NC*	16	T0/P3.4	31	P2.7/A15
2	T2/P1.0	17	T1/P3.5	32	$\overline{PSEN}$
3	T2EX/P1.1	18	$\overline{WR}$/P3.6	33	ALE/$\overline{PROG}$
4	P1.2	19	$\overline{RD}$/P3.7	34	NC*
5	P1.3	20	XTAL2	35	$\overline{EA}$/V_{PP}
6	P1.4	21	XTAL1	36	P0.7/AD7
7	P1.5	22	V_{SS}	37	P0.6/AD6
8	P1.6	23	NC*	38	P0.5/AD5
9	P1.7	24	P2.0/A8	39	P0.4/AD4
10	RST	25	P2.1/A9	40	P0.3/AD3
11	RxD/P3.0	26	P2.2/A10	41	P0.2/AD2
12	NC*	27	P2.3/A11	42	P0.1/AD1
13	TxD/P3.1	28	P2.4/A12	43	P0.0/AD0
14	$\overline{INT0}$/P3.2	29	P2.5/A13	44	V_{CC}
15	$\overline{INT1}$/P3.3	30	P2.6/A14		

* DO NOT CONNECT

SU00061

PLASTIC QUAD FLAT PACK PIN FUNCTIONS



Pin	Function	Pin	Function	Pin	Function
1	P1.5	16	V_{SS}	31	P0.6/AD6
2	P1.6	17	NC*	32	P0.5/AD5
3	P1.7	18	P2.0/A8	33	P0.4/AD4
4	RST	19	P2.1/A9	34	P0.3/AD3
5	RxD/P3.0	20	P2.2/A10	35	P0.2/AD2
6	NC*	21	P2.3/A11	36	P0.1/AD1
7	TxD/P3.1	22	P2.4/A12	37	P0.0/AD0
8	$\overline{INT0}$/P3.2	23	P2.5/A13	38	V_{CC}
9	$\overline{INT1}$/P3.3	24	P2.6/A14	39	NC*
10	T0/P3.4	25	P2.7/A15	40	T2/P1.0
11	T1/P3.5	26	$\overline{PSEN}$	41	T2EX/P1.1
12	$\overline{WR}$/P3.6	27	ALE/$\overline{PROG}$	42	P1.2
13	$\overline{RD}$/P3.7	28	NC*	43	P1.3
14	XTAL2	29	$\overline{EA}$/V_{PP}	44	P1.4
15	XTAL1	30	P0.7/AD7		

* DO NOT CONNECT

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PIN DESCRIPTIONS

MNEMONIC	PIN NUMBER DIP	PIN NUMBER LCC	PIN NUMBER QFP	TYPE	NAME AND FUNCTION
V_{SS}	20	22	16	I	**Ground:** 0V reference.
V_{CC}	40	44	38	I	**Power Supply:** This is the power supply voltage for normal, idle, and power-down operation.
P0.0–0.7	39–32	43–36	37–30	I/O	**Port 0:** Port 0 is an open-drain, bidirectional I/O port. Port 0 pins that have 1s written to them float and can be used as high-impedance inputs. Port 0 is also the multiplexed low-order address and data bus during accesses to external program and data memory. In this application, it uses strong internal pull-ups when emitting 1s. Port 0 also outputs the code bytes during program verification and receives code bytes during EPROM programming. External pull-ups are required during program verification.
P1.0–P1.7	1–8	2–9	40–44, 1–3	I/O	**Port 1:** Port 1 is an 8-bit bidirectional I/O port with internal pull-ups, except P1.6 and P1.7 which are open drain. Port 1 pins that have 1s written to them are pulled high by the internal pull-ups and can be used as inputs. As inputs, port 1 pins that are externally pulled low will source current because of the internal pull-ups. (See DC Electrical Characteristics: I_{IL}). Port 1 also receives the low-order address byte during program memory verification. Alternate functions include:
	1	2	40	I	**T2 (P1.0):** Timer/Counter 2 external count input/Clockout
	2	3	41	I	**T2EX (P1.1):** Timer/Counter 2 Reload/Capture/Direction Control
P2.0–P2.7	21–28	24–31	18–25	I/O	**Port 2:** Port 2 is an 8-bit bidirectional I/O port with internal pull-ups. Port 2 pins that have 1s written to them are pulled high by the internal pull-ups and can be used as inputs. As inputs, port 2 pins that are externally being pulled low will source current because of the internal pull-ups. (See DC Electrical Characteristics: I_{IL}). Port 2 emits the high-order address byte during fetches from external program memory and during accesses to external data memory that use 16-bit addresses (MOVX @DPTR). In this application, it uses strong internal pull-ups when emitting 1s. During accesses to external data memory that use 8-bit addresses (MOV @Ri), port 2 emits the contents of the P2 special function register. Some Port 2 pins receive the high order address bits during EPROM programming and verification.
P3.0–P3.7	10–17	11, 13–19	5, 7–13	I/O	**Port 3:** Port 3 is an 8-bit bidirectional I/O port with internal pull-ups. Port 3 pins that have 1s written to them are pulled high by the internal pull-ups and can be used as inputs. As inputs, port 3 pins that are externally being pulled low will source current because of the pull-ups. (See DC Electrical Characteristics: I_{IL}). Port 3 also serves the special features of the 80C51 family, as listed below:
	10	11	5	I	**RxD (P3.0):** Serial input port
	11	13	7	O	**TxD (P3.1):** Serial output port
	12	14	8	I	**$\overline{INT0}$ (P3.2):** External interrupt
	13	15	9	I	**$\overline{INT1}$ (P3.3):** External interrupt
	14	16	10	I	**T0 (P3.4):** Timer 0 external input
	15	17	11	I	**T1 (P3.5):** Timer 1 external input
	16	18	12	O	**$\overline{WR}$ (P3.6):** External data memory write strobe
	17	19	13	O	**$\overline{RD}$ (P3.7):** External data memory read strobe
RST	9	10	4	I	**Reset:** A high on this pin for two machine cycles while the oscillator is running, resets the device. An internal diffused resistor to V_{SS} permits a power-on reset using only an external capacitor to V_{CC}.
ALE/$\overline{PROG}$	30	33	27	I/O	**Address Latch Enable/Program Pulse:** Output pulse for latching the low byte of the address during an access to external memory. In normal operation, ALE is emitted at a constant rate of 1/6 the oscillator frequency, and can be used for external timing or clocking. Note that one ALE pulse is skipped during each access to external data memory. This pin is also the program pulse input ($\overline{PROG}$) during EPROM programming. ALE can be disabled by setting SFR auxiliary.0. With this bit set, ALE will be active only during a MOVX instruction.
$\overline{PSEN}$	29	32	26	O	**Program Store Enable:** The read strobe to external program memory. When the 8XC58 is executing code from the external program memory, $\overline{PSEN}$ is activated twice each machine cycle, except that two $\overline{PSEN}$ activations are skipped during each access to external data memory. $\overline{PSEN}$ is not activated during fetches from internal program memory.
$\overline{EA}$/V_{PP}	31	35	29	I	**External Access Enable/Programming Supply Voltage:** $\overline{EA}$ must be externally held low to enable the device to fetch code from external program memory locations 0000H and 7FFFH. If $\overline{EA}$ is held high, the device executes from internal program memory unless the program counter contains an address greater than 7FFFH. This pin also receives the 12.75V programming supply voltage (V_{PP}) during EPROM programming. If security bit 1 is programmed, $\overline{EA}$ will be internally latched on Reset.
XTAL1	19	21	15	I	**Crystal 1:** Input to the inverting oscillator amplifier and input to the internal clock generator circuits.
XTAL2	18	20	14	O	**Crystal 2:** Output from the inverting oscillator amplifier.

NOTE:
To avoid “latch-up” effect at power-on, the voltage on any pin at any time must not be higher than V_{CC} + 0.5V or V_{SS} – 0.5V, respectively.

TIMER 2

This is a 16-bit up or down counter, which can be operated as either a timer or event counter. It can be operated in one of three different modes (autoreload, capture or as the baud rate generator for the UART).

In the autoreload mode the Timer can be set to count up or down by setting or clearing the bit DCEN in the T2CON Special Function Register. The SFR's RCAP2H and RCAP2L are used to reload the Timer upon overflow or a 1-to-0 transition on the T2EX input (P1.1).

In the Capture mode Timer 2 can either set TF2 and generate an interrupt or capture its value. To capture Timer 2 in response to a 1-to-0 transition on the T2EX input, the EXEN2 bit in the T2CON must be set. Timer 2 is then captured in SFR's RCAP2H and RCAP2L.

As the baud rate generator, Timer 2 is selected by setting TCLK and/or RCLK in T2CON. As the baud rate generator Timer 2 is incremented at $^1/_2$ the oscillator frequency.

POWER OFF FLAG

The Power Off Flag (POF) is set by on-chip circuitry when the V_{CC} level on the 8XC58 rises from 0 to 5V. The POF bit can be set or cleared by software allowing a user to determine if the reset is the result of a power-on or a warm start after powerdown. The V_{CC} level must remain above 3V for the POF to remain unaffected by the V_{CC} level.

OSCILLATOR CHARACTERISTICS

XTAL1 and XTAL2 are the input and output, respectively, of an inverting amplifier. The pins can be configured for use as an on-chip oscillator.

To drive the device from an external clock source, XTAL1 should be driven while XTAL2 is left unconnected. There are no requirements on the duty cycle of the external clock signal, because the input to the internal clock circuitry is through a divide-by-two flip-flop. However, minimum and maximum high and low times specified in the data sheet must be observed.

Reset

A reset is accomplished by holding the RST pin high for at least two machine cycles (24 oscillator periods), while the oscillator is running. To insure a good power-on reset, the RST pin must be high long enough to allow the oscillator time to start up (normally a few milliseconds) plus two machine cycles. At power-on, the voltage on V_{CC} and RST must come up at the same time for a proper start-up. Ports 1, 2, and 3 will asynchronously be driven to their reset condition when a voltage above V_{IH1} is applied to RESET.

Idle Mode

In the idle mode, the CPU puts itself to sleep while all of the on-chip peripherals stay active. The instruction to invoke the idle mode is the last instruction executed in the normal operating mode before the idle mode is activated. The CPU contents, the on-chip RAM, and all of the special function registers remain intact during this mode. The idle mode can be terminated either by any enabled interrupt (at which time the process is picked up at the interrupt service routine and continued), or by a hardware reset which starts the processor in the same manner as a power-on reset.

Power-Down Mode

To save even more power, a Power Down mode can be invoked by software. In this mode, the oscillator is stopped and the instruction that invoked Power Down is the last instruction executed. The on-chip RAM and Special Function Registers retain their values until the Power Down mode is terminated.

On the 8XC58 either a hardware reset or external interrupt can use an exit from Power Down. Reset redefines all the SFRs but does not change the on-chip RAM. An external interrupt allows both the SFRs and the on-chip RAM to retain their values.

To properly terminate Power Down the reset or external interrupt should not be executed before V_{CC} is restored to its normal operating level and must be held active long enough for the oscillator to restart and stabilize (normally less than 10ms).

With an external interrupt, INT0 and INT1 must be enabled and configured as level-sensitive. Holding the pin low restarts the oscillator but bringing the pin back high completes the exit. Once the interrupt is serviced, the next instruction to be executed after RETI will be the one following the instruction that put the device into Power Down.

Design Consideration

- When the idle mode is terminated by a hardware reset, the device normally resumes program execution, from where it left off, up to two machine cycles before the internal rest algorithm takes control. On-chip hardware inhibits access to internal RAM in this event, but access to the port pins is not inhibited. To eliminate the possibility of an unexpected write when Idle is terminated by reset, the instruction following the one that invokes Idle should not be one that writes to a port pin or to external memory.
- The windowed parts must be covered with an opaque label to assure proper chip operation.

ONCE™ Mode

The ONCE ("On-Circuit Emulation") Mode facilitates testing and debugging of systems using the 8XC58 without the 8XC58 having to be removed from the circuit. The ONCE Mode is invoked by:

1. Pull ALE low while the device is in reset and $\overline{PSEN}$ is high;
2. Hold ALE low as RST is deactivated.

While the device is in ONCE Mode, the Port 0 pins go into a float state, and the other port pins and ALE and $\overline{PSEN}$ are weakly pulled high. The oscillator circuit remains active. While the 8XC58 is in this mode, an emulator or test CPU can be used to drive the circuit. Normal operation is restored when a normal reset is applied.

Table 2. External Pin Status During Idle and Power-Down Mode

MODE	PROGRAM MEMORY	ALE	$\overline{PSEN}$	PORT 0	PORT 1	PORT 2	PORT 3
Idle	Internal	1	1	Data	Data	Data	Data
Idle	External	1	1	Float	Data	Address	Data
Power-down	Internal	0	0	Data	Data	Data	Data
Power-down	External	0	0	Float	Data	Data	Data

Programmable Clock-Out

The 87C54/87C58 has a new feature. A 50% duty cycle clock can be programmed to come out on P1.0. This pin, besides being a regular I/O pin, has two alternate functions. It can be programmed (1) to input the external clock for Timer/Counter 2 or (2) to output a 50% duty cycle clock ranging from 61Hz to 4MHz at a 16MHz operating frequency.

To configure the Timer/Counter 2 as a clock generator, bit C/T2 (in T2CON) must be cleared and bit T20E in T2MOD must be set. Bit TR2 (T2CON.2) also must be set to start the timer.

The Clock-Out frequency depends on the oscillator frequency and the reload value of Timer 2 capture registers (RCAP2H, RCAP2L) as shown in this equation:

$$\frac{\text{OscillatorFrequency}}{4 \times (65536 - \text{RCAP2H, RCAP2L})}$$

In the Clock-Out mode Timer 2 roll-overs will not generate an interrupt. This is similar to when it is used as a baud-rate generator. It is possible to use Timer 2 as a baud-rate generator and a clock generator simultaneously. Note, however, that the baud-rate and the Clock-Out frequency will be the same.

Enhanced UART

The UART operates in all of the usual modes that are described in the first section of this book for the 80C51. In addition the UART can perform framing error detect by looking for missing stop bits, and automatic address recognition. The 87C54/87C58 UART also fully supports multiprocessor communication as does the standard 80C51 UART.

When used for framing error detect the UART looks for missing stop bits in the communication. A missing bit will set the FE bit in the SCON register. The FE bit shares the SCON.7 bit with SM0 and the function of SCON.7 is determined by PCON.6 (SMOD0) (see Figure 1). If SMOD0 is set then SCON.7 functions as FE. SCON.7 functions as SM0 when SMOD0 is cleared. When used as FE SCON.7 can only be cleared by software. Refer to Figure 2.

Automatic Address Recognition

Automatic Address Recognition is a feature which allows the UART to recognize certain addresses in the serial bit stream by using hardware to make the comparisons. This feature saves a great deal of software overhead by eliminating the need for the software to examine every serial address which passes by the serial port. This feature is enabled by setting the SM2 bit in SCON. In the 9 bit UART modes, mode 2 and mode 3, the Receive Interrupt flag (RI) will be automatically set when the received byte contains either the “Given” address or the “Broadcast” address. The 9 bit mode requires that the 9th information bit is a 1 to indicate that the received information is an address and not data. Automatic address recognition is shown in Figure 3.

The 8 bit mode is called Mode 1. In this mode the RI flag will be set if SM2 is enabled and the information received has a valid stop bit following the 8 address bits and the information is either a Given or Broadcast address.

Mode 0 is the Shift Register mode and SM2 is ignored.

Using the Automatic Address Recognition feature allows a master to selectively communicate with one or more slaves by invoking the Given slave address or addresses. All of the slaves may be contacted by using the Broadcast address. Two special Function Registers are used to define the slave’s address, SADDR, and the address mask, SADEN. SADEN is used to define which bits in the SADDR are to b used and which bits are “don’t care”. The SADEN mask can be logically ANDed with the SADDR to create the “|Given” address which the master will use for addressing each of the slaves. Use of the Given address allows multiple slaves to be recognized while excluding others. The following examples will help to show the versatility of this scheme:

Slave 0	SADDR	=	1100 0000
	SADEN	=	1111 1101
	Given	=	1100 00X0
Slave 1	SADDR	=	1100 0000
	SADEN	=	1111 1110
	Given	=	1100 000X

In the above example SADDR is the same and the SADEN data is used to differentiate between the two slaves. Slave 0 requires a 0 in bit 0 and it ignores bit 1. Slave 1 requires a 0 in bit 1 and bit 0 is ignored. A unique address for Slave 0 would be 1100 0010 since slave 1 requires a 0 in bit 1. A unique address for slave 1 would be 1100 0001 since a 1 in bit 0 will exclude slave 0. Both slaves can be selected at the same time by an address which has bit 0 = 0 (for slave 0) and bit 1 = 0 (for slave 1). Thus, both could be addressed with 1100 0000.

In a more complex system the following could be used to select slaves 1 and 2 while excluding slave 0:

Slave 0	SADDR	=	1100 0000
	SADEN	=	1111 1001
	Given	=	1100 0XX0
Slave 1	SADDR	=	1110 0000
	SADEN	=	1111 1010
	Given	=	1110 0X0X
Slave 2	SADDR	=	1110 0000
	SADEN	=	1111 1100
	Given	=	1110 00XX

In the above example the differentiation among the 3 slaves is in the lower 3 address bits. Slave 0 requires that bit 0 = 0 and it can be uniquely addressed by 1110 0110. Slave 1 requires that bit 1 = 0 and it can be uniquely addressed by 1110 and 0101. Slave 2 requires that bit 2 = 0 and its unique address is 1110 0011. To select Slaves 0 and 1 and exclude Slave 2 use address 1110 0100, since it is necessary t make bit 2 = 1 to exclude slave 2.

The Broadcast Address for each slave is created by taking the logical OR of SADDR and SADEN. Zeros in this result are teated as don’t-cares. In most cases, interpreting the don’t-cares as ones, the broadcast address will be FF hexadecimal.

Upon reset SADDR (SFR address 0A9H) and SADEN (SFR address 0B9H) are loaded with 0s. This produces a given address of all “don’t cares” as well as a Broadcast address of all “don’t cares”. this effectively disables the Automatic Addressing mode and allows the microcontroller to use standard 80C51 type UART drivers which do not make use of this feature.

Reduced EMI Mode

The AO bit (AUXR.0) in the AUXR register, when set, disables the ALE output.

8XC58 Reduced EMI Mode

AUXR (0X8E)

7	6	5	4	3	2	1	0
–	–	–	–	–	–	–	AO

AO: Turns off ALE output.

Interrupt Priority Structure

The 87C54/87C58 has a 6-source two-level interrupt structure. There are 3 SFRs associated with the interrupts. They are the IE and IP which are identical in function to those on the 80C51.

The priority scheme for servicing the interrupts is the same as that for the 80C51. An interrupt will be serviced as long as an interrupt of equal or higher priority is not already being serviced. If an interrupt of equal or higher level priority is being serviced, the new interrupt will wait until it is finished before being serviced. If a lower priority level interrupt is being serviced, it will be stopped and the new interrupt serviced. When the new interrupt is finished, the lower priority level interrupt that was stopped will be completed.

Table 3. Interrupt Table

SOURCE	POLLING PRIORITY	REQUEST BITS	HARDWARE CLEAR?	VECTOR ADDRESS
X0	1	IE0	N (L) Y (T)	03H
T0	2	TP0	Y	0B
X1	3	IE1	N (L) Y (T)	13
T1	4	TF1	Y	1B
SP	5	R1, TI	N	23
T2	6	TF2, EXF2	N	2B

SCON Address = 98H Reset Value = 0000 0000B

Bit Addressable

	SM0/FE	SM1	SM2	REN	TB8	RB8	TI	RI
Bit:	7	6	5	4	3	2	1	0
	(SMOD0 = 0/1)*							

Symbol	Function
FE	Framing Error bit. This bit is set by the receiver when an invalid stop bit is detected. The FE bit is not cleared by valid frames but should be cleared by software. The SMOD0 bit must be set to enable access to the FE bit.
SM0	Serial Port Mode Bit 0, (SMOD0 must = 0 to access bit SM0)
SM1	Serial Port Mode Bit 1

SM0	SM1	Mode	Description	Baud Rate**
0	0	0	shift register	$f_{OSC}/12$
0	1	1	8-bit UART	variable
1	0	2	9-bit UART	$f_{OSC}/64$ or $f_{OSC}/32$
1	1	3	9-bit UART	variable

SM2	Enables the Automatic Address Recognition feature in Modes 2 or 3. If SM2 = 1 then RI will not be set unless the received 9th data bit (RB8) is 1, indicating an address, and the received byte is a Given or Broadcast Address. In Mode 1, if SM2 = 1 then RI will not be activated unless a valid stop bit was received, and the received byte is a Given or Broadcast Address. In Mode 0, SM2 should be 0.
REN	Enables serial reception. Set by software to enable reception. Clear by software to disable reception.
TB8	The 9th data bit that will be transmitted in Modes 2 and 3. Set or clear by software as desired.
RB8	In modes 2 and 3, the 9th data bit that was received. In Mode 1, if SM2 = 0, RB8 is the stop bit that was received. In Mode 0, RB8 is not used.
TI	Transmit interrupt flag. Set by hardware at the end of the 8th bit time in Mode 0, or at the beginning of the stop bit in the other modes, in any serial transmission. Must be cleared by software.
RI	Receive interrupt flag. Set by hardware at the end of the 8th bit time in Mode 0, or halfway through the stop bit time in the other modes, in any serial reception (except see SM2). Must be cleared by software.

NOTE:
*SMOD0 is located at PCON6.
**f_{OSC} = oscillator frequency

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Figure 1. SCON: Serial Port Control Register

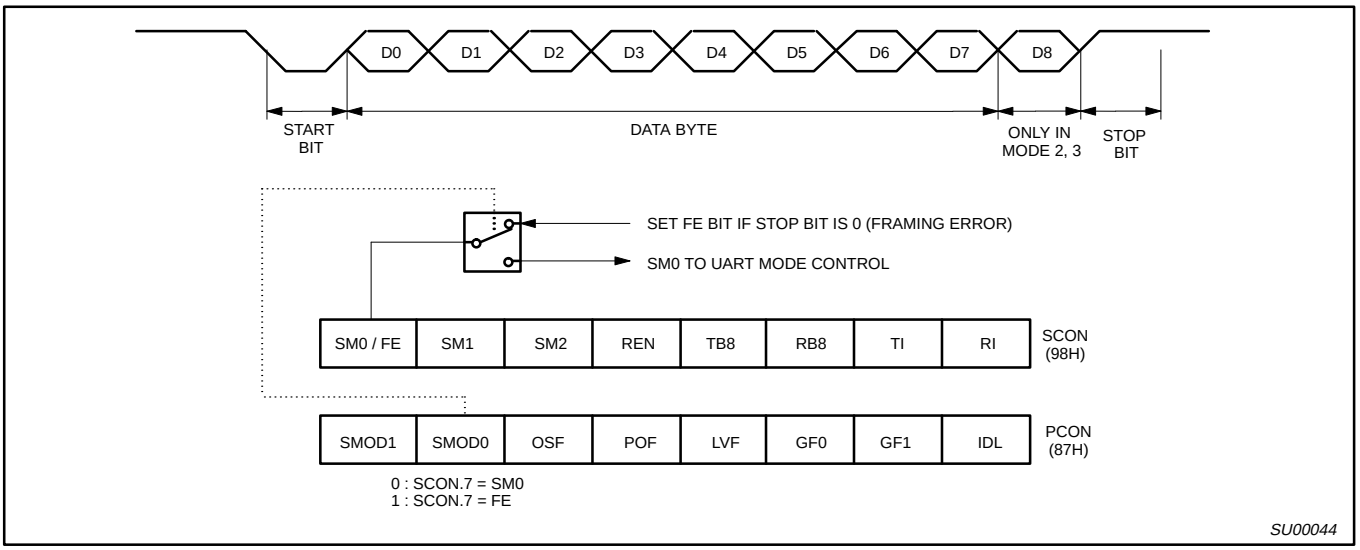


Figure 2. UART Framing Error Detection

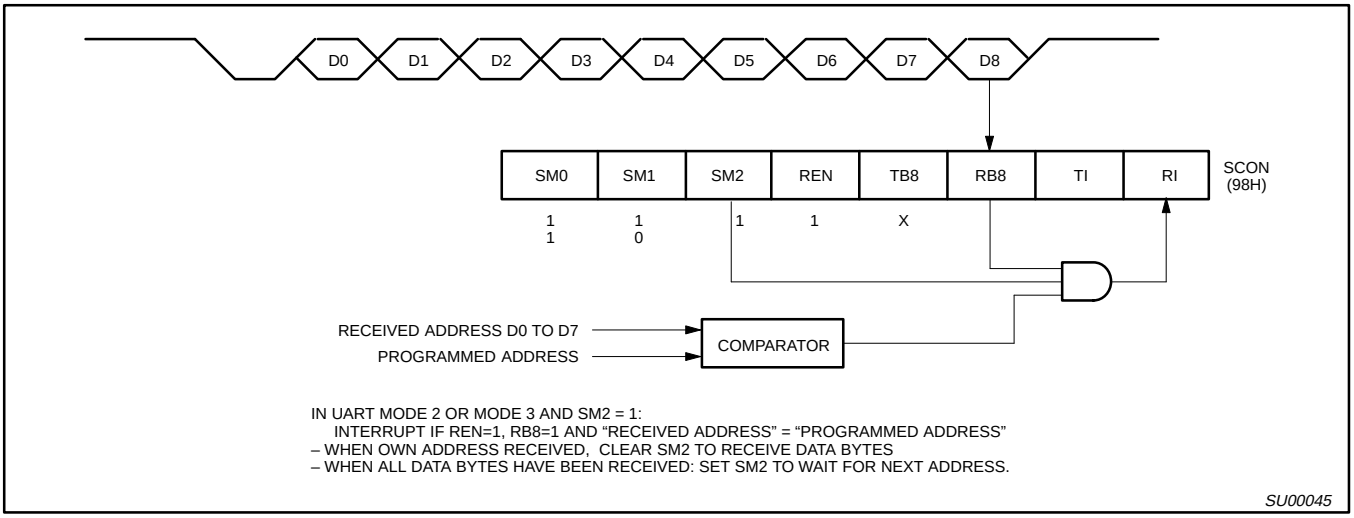


Figure 3. UART Multiprocessor Communication, Automatic Address Recognition

ABSOLUTE MAXIMUM RATINGS[1, 2, 3]

PARAMETER	RATING	UNIT
Operating temperature under bias	0 to +70 or –40 to +85	°C
Storage temperature range	–65 to +150	°C
Voltage on $\overline{EA}/V_{PP}$ pin to V_{SS}	0 to +13.0	V
Voltage on any other pin to V_{SS}	–0.5 to +6.5	V
Maximum I_{OL} per I/O pin	15	mA
Power dissipation (based on package heat transfer limitations, not device power consumption)	1.5	W

NOTES:

1. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any conditions other than those described in the AC and DC Electrical Characteristics section of this specification is not implied.
2. This product includes circuitry specifically designed for the protection of its internal devices from the damaging effects of excessive static charge. Nonetheless, it is suggested that conventional precautions be taken to avoid applying greater than the rated maxima.
3. Parameters are valid over operating temperature range unless otherwise specified. All voltages are with respect to V_{SS} unless otherwise noted.

DC ELECTRICAL CHARACTERISTICS

T_{amb} = 0°C to +70°C, V_{CC} = 5V ±10%, V_{SS} = 0V

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP[1]	MAX	
V_{IL}	Input low voltage, except $\overline{EA}$		–0.5		$0.2V_{CC}$–0.1	V
V_{IL1}	Input low voltage to $\overline{EA}$		0		$0.2V_{CC}$–0.3	V
V_{IH1}	Input high voltage, XTAL1, RST		$0.7V_{CC}$		V_{CC}+0.5	V
V_{OL}	Output low voltage, ports 1, 2, 3[7]	I_{OL} = 1.6mA[2]			0.45	V
V_{OL1}	Output low voltage, port 0, ALE, $\overline{PSEN}$[7]	I_{OL} = 3.2mA[2]			0.45	V
V_{OH}	Output high voltage, ports 1, 2, 3 [3]	I_{OH} = –30µA	V_{CC} – 0.7			V
V_{OH1}	Output high voltage (port 0 in external bus mode), ALE[8], $\overline{PSEN}$[3]	I_{OH} = –3.2mA	V_{CC} – 0.7			V
I_{IL}	Logical 0 input current, ports 1, 2, 3	V_{IN} = 0.4V			–50	µA
I_{TL}	Logical 1-to-0 transition current, ports 1, 2, 3[5]	See note 4			–650	µA
I_{LI}	Input leakage current, port 0	0.45 V_{IN} < V_{CC} – 0.3			±10	µA
I_{CC}	Power supply current (See Figure 11):	See note 10				
	Active mode @ 16MHz			15	32	mA
	Idle mode @ 16MHz			3	5	mA
	Power-down mode T_{amb} = 0 to +70°C			10	75	µA
	T_{amb} = –40 to +85°C				100	µA
R_{RST}	Internal reset pull-down resistor		40		225	kΩ
C_{IO}	Pin capacitance[9] (except $\overline{EA}$)				15	pF

NOTES:

1. Typical ratings are not guaranteed. The values listed are at room temperature, 5V.
2. Capacitive loading on ports 0 and 2 may cause spurious noise to be superimposed on the V_{OL}s of ALE and ports 1 and 3. The noise is due to external bus capacitance discharging into the port 0 and port 2 pins when these pins make 1-to-0 transitions during bus operations. In the worst cases (capacitive loading > 100pF), the noise pulse on the ALE pin may exceed 0.8V. In such cases, it may be desirable to qualify ALE with a Schmitt Trigger, or use an address latch with a Schmitt Trigger STROBE input. I_{OL} can exceed these conditions provided that no single output sinks more than 5mA and no more than two outputs exceed the test conditions.
3. Capacitive loading on ports 0 and 2 may cause the V_{OH} on ALE and $\overline{PSEN}$ to momentarily fall below the $0.9V_{CC}$ specification when the address bits are stabilizing.
4. Pins of ports 1, 2 and 3 source a transition current when they are being externally driven from 1 to 0. The transition current reaches its maximum value when V_{IN} is approximately 2V.
5. This value applies to T_{amb} = 0°C to +70°C. For T_{amb} = –40°C to 85°C, I_{TL} = –750µA.
6. Load capacitance for port 0, ALE, and $\overline{PSEN}$ = 100pF, load capacitance for all other outputs = 80pF.
7. Under steady state (non-transient) conditions, I_{OL} must be externally limited as follows:
   Maximum I_{OL} per port pin: 15mA
   Maximum I_{OL} per 8-bit port: 26mA
   Maximum total I_{OL} for all outputs: 71mA
   If I_{OL} exceeds the test condition, V_{OL} may exceed the related specification. Pins are not guaranteed to sink current greater than the listed test conditions.
8. ALE is tested to V_{OH1}, except when ALE is off then V_{OH} is the voltage specification.
9. Pin capacitance is characterized but not tested. Pin capacitance is less than 25pF. Pin capacitance of ceramic package is less than 15pF (except $\overline{EA}$ it is 25pF).
10. See Figures 12 through 15 for I_{CC} test condition.

AC ELECTRICAL CHARACTERISTICS

T_{amb} = 0°C to +70°C or –40°C to +85°C, V_{CC} = 5V ±10%, V_{SS} = 0V[1, 2, 3]

SYMBOL	FIGURE	PARAMETER	16MHz CLOCK		VARIABLE CLOCK		UNIT
			MIN	MAX	MIN	MAX	
$1/t_{CLCL}$	4	Oscillator frequency Speed versions : E			3.5	16	MHz
t_{LHLL}	4	ALE pulse width	85		$2t_{CLCL}$–40		ns
t_{AVLL}	4	Address valid to ALE low	22		t_{CLCL}–40		ns
t_{LLAX}	4	Address hold after ALE low	32		t_{CLCL}–30		ns
t_{LLIV}	4	ALE low to valid instruction in		150		$4t_{CLCL}$–100	ns
t_{LLPL}	4	ALE low to $\overline{PSEN}$ low	32		t_{CLCL}–30		ns
t_{PLPH}	4	$\overline{PSEN}$ pulse width	142		$3t_{CLCL}$–45		ns
t_{PLIV}	4	$\overline{PSEN}$ low to valid instruction in		82		$3t_{CLCL}$–105	ns
t_{PXIX}	4	Input instruction hold after $\overline{PSEN}$	0		0		ns
t_{PXIZ}	4	Input instruction float after $\overline{PSEN}$		37		t_{CLCL}–25	ns
t_{AVIV}	4	Address to valid instruction in		207		$5t_{CLCL}$–105	ns
t_{PLAZ}	4	$\overline{PSEN}$ low to address float		10		10	ns
Data Memory							
t_{RLRH}	5, 6	$\overline{RD}$ pulse width	275		$6t_{CLCL}$–100		ns
t_{WLWH}	5, 6	$\overline{WR}$ pulse width	275		$6t_{CLCL}$–100		ns
t_{RLDV}	5, 6	$\overline{RD}$ low to valid data in		147		$5t_{CLCL}$–165	ns
t_{RHDX}	5, 6	Data hold after $\overline{RD}$	0		0		ns
t_{RHDZ}	5, 6	Data float after $\overline{RD}$		65		$2t_{CLCL}$–60	ns
t_{LLDV}	5, 6	ALE low to valid data in		350		$8t_{CLCL}$–150	ns
t_{AVDV}	5, 6	Address to valid data in		397		$9t_{CLCL}$–165	ns
t_{LLWL}	5, 6	ALE low to $\overline{RD}$ or $\overline{WR}$ low	137	239	$3t_{CLCL}$–50	$3t_{CLCL}$+50	ns
t_{AVWL}	5, 6	Address valid to $\overline{WR}$ low or $\overline{RD}$ low	122		$4t_{CLCL}$–130		ns
t_{QVWX}	5, 6	Data valid to $\overline{WR}$ transition	13		t_{CLCL}–50		ns
t_{WHQX}	5, 6	Data hold after $\overline{WR}$	13		t_{CLCL}–50		ns
t_{QVWH}	6	Data valid to $\overline{WR}$ high	287		$7t_{CLCL}$–150		ns
t_{RLAZ}	5, 6	$\overline{RD}$ low to address float		0		0	ns
t_{WHLH}	5, 6	$\overline{RD}$ or $\overline{WR}$ high to ALE high	23	103	t_{CLCL}–40	t_{CLCL}+40	ns
External Clock							
t_{CHCX}	8	High time	20		20	$t_{CLCL}+t_{CLCX}$	ns
t_{CLCX}	8	Low time	20		20	$t_{CLCL}+t_{CHCX}$	ns
t_{CLCH}	8	Rise time		20		20	ns
t_{CHCL}	8	Fall time		20		20	ns
Shift Register							
t_{XLXL}	7	Serial port clock cycle time	750		$12t_{CLCL}$		ns
t_{QVXH}	7	Output data setup to clock rising edge	492		$10t_{CLCL}$–133		ns
t_{XHQX}	7	Output data hold after clock rising edge	8		$2t_{CLCL}$–117		ns
t_{XHDX}	7	Input data hold after clock rising edge	0		0		ns
t_{XHDV}	7	Clock rising edge to input data valid		492		$10t_{CLCL}$–133	ns

NOTES:
1. Parameters are valid over operating temperature range unless otherwise specified.
2. Load capacitance for port 0, ALE, and $\overline{PSEN}$ = 100pF, load capacitance for all other outputs = 80pF.
3. Interfacing the 8XC58 to devices with float times up to 45ns is permitted. This limited bus contention will not cause damage to Port 0 drivers.

AC ELECTRICAL CHARACTERISTICS

T_{amb} = 0°C to +70°C or –40°C to +85°C, V_{CC} = 5V ±10%, V_{SS} = 0V[1, 2, 3]

SYMBOL	FIGURE	PARAMETER	24MHz CLOCK		VARIABLE CLOCK[4]		UNIT
			MIN	MAX	MIN	MAX	
$1/t_{CLCL}$	4	Oscillator frequency Speed versions : I			3.5	24	MHz
t_{LHLL}	4	ALE pulse width	43		$2t_{CLCL}$–40		ns
t_{AVLL}	4	Address valid to ALE low	17		t_{CLCL}–25		ns
t_{LLAX}	4	Address hold after ALE low	17		t_{CLCL}–25		ns
t_{LLIV}	4	ALE low to valid instruction in		102		$4t_{CLCL}$–65	ns
t_{LLPL}	4	ALE low to $\overline{PSEN}$ low	17		t_{CLCL}–25		ns
t_{PLPH}	4	$\overline{PSEN}$ pulse width	80		$3t_{CLCL}$–45		ns
t_{PLIV}	4	$\overline{PSEN}$ low to valid instruction in		65		$3t_{CLCL}$–60	ns
t_{PXIX}	4	Input instruction hold after $\overline{PSEN}$	0		0		ns
t_{PXIZ}	4	Input instruction float after $\overline{PSEN}$		17		t_{CLCL}–25	ns
t_{AVIV}	4	Address to valid instruction in		128		$5t_{CLCL}$–80	ns
t_{PLAZ}	4	$\overline{PSEN}$ low to address float		10		10	ns
Data Memory							
t_{RLRH}	5, 6	$\overline{RD}$ pulse width	150		$6t_{CLCL}$–100		ns
t_{WLWH}	5, 6	$\overline{WR}$ pulse width	150		$6t_{CLCL}$–100		ns
t_{RLDV}	5, 6	$\overline{RD}$ low to valid data in		118		$5t_{CLCL}$–90	ns
t_{RHDX}	5, 6	Data hold after $\overline{RD}$	0		0		ns
t_{RHDZ}	5, 6	Data float after $\overline{RD}$		55		$2t_{CLCL}$–28	ns
t_{LLDV}	5, 6	ALE low to valid data in		183		$8t_{CLCL}$–150	ns
t_{AVDV}	5, 6	Address to valid data in		210		$9t_{CLCL}$–165	ns
t_{LLWL}	5, 6	ALE low to $\overline{RD}$ or $\overline{WR}$ low	75	175	$3t_{CLCL}$–50	$3t_{CLCL}$+50	ns
t_{AVWL}	5, 6	Address valid to $\overline{WR}$ low or $\overline{RD}$ low	92		$4t_{CLCL}$–75		ns
t_{QVWX}	5, 6	Data valid to $\overline{WR}$ transition	12		t_{CLCL}–30		ns
t_{WHQX}	5, 6	Data hold after $\overline{WR}$	17		t_{CLCL}–25		ns
t_{QVWH}	6	Data valid to $\overline{WR}$ high	162		$7t_{CLCL}$–130		ns
t_{RLAZ}	5, 6	$\overline{RD}$ low to address float		0		0	ns
t_{WHLH}	5, 6	$\overline{RD}$ or $\overline{WR}$ high to ALE high	17	67	t_{CLCL}–25	t_{CLCL}+25	ns
External Clock							
t_{CHCX}	8	High time	17		17	t_{CLCL}–t_{CLCX}	ns
t_{CLCX}	8	Low time	17		17	t_{CLCL}–t_{CHCX}	ns
t_{CLCH}	8	Rise time		5		5	ns
t_{CHCL}	8	Fall time		5		5	ns
Shift Register							
t_{XLXL}	7	Serial port clock cycle time	505		$12t_{CLCL}$		ns
t_{QVXH}	7	Output data setup to clock rising edge	283		$10t_{CLCL}$–133		ns
t_{XHQX}	7	Output data hold after clock rising edge	3		$2t_{CLCL}$–80		ns
t_{XHDX}	7	Input data hold after clock rising edge	0		0		ns
t_{XHDV}	7	Clock rising edge to input data valid		283		$10t_{CLCL}$–133	ns

NOTES:
1. Parameters are valid over operating temperature range unless otherwise specified.
2. Load capacitance for port 0, ALE, and $\overline{PSEN}$ = 100pF, load capacitance for all other outputs = 80pF.
3. Interfacing the 87C58 to devices with float times up to 45ns is permitted. This limited bus contention will not cause damage to Port 0 drivers.
4. Variable clock is specified for oscillator frequencies greater than 16MHz to 24MHz. For frequencies equal or less than 16MHz, see 16MHz "AC Electrial Characteristics", page 3-226.

EXPLANATION OF THE AC SYMBOLS

Each timing symbol has five characters. The first character is always 't' (= time). The other characters, depending on their positions, indicate the name of a signal or the logical status of that signal. The designations are:

A – Address
C – Clock
D – Input data
H – Logic level high
I – Instruction (program memory contents)
L – Logic level low, or ALE
P – $\overline{PSEN}$
Q – Output data
R – $\overline{RD}$ signal
t – Time
V – Valid
W – $\overline{WR}$ signal
X – No longer a valid logic level
Z – Float

Examples: t_{AVLL} = Time for address valid to ALE low.
t_{LLPL} =Time for ALE low to $\overline{PSEN}$ low.

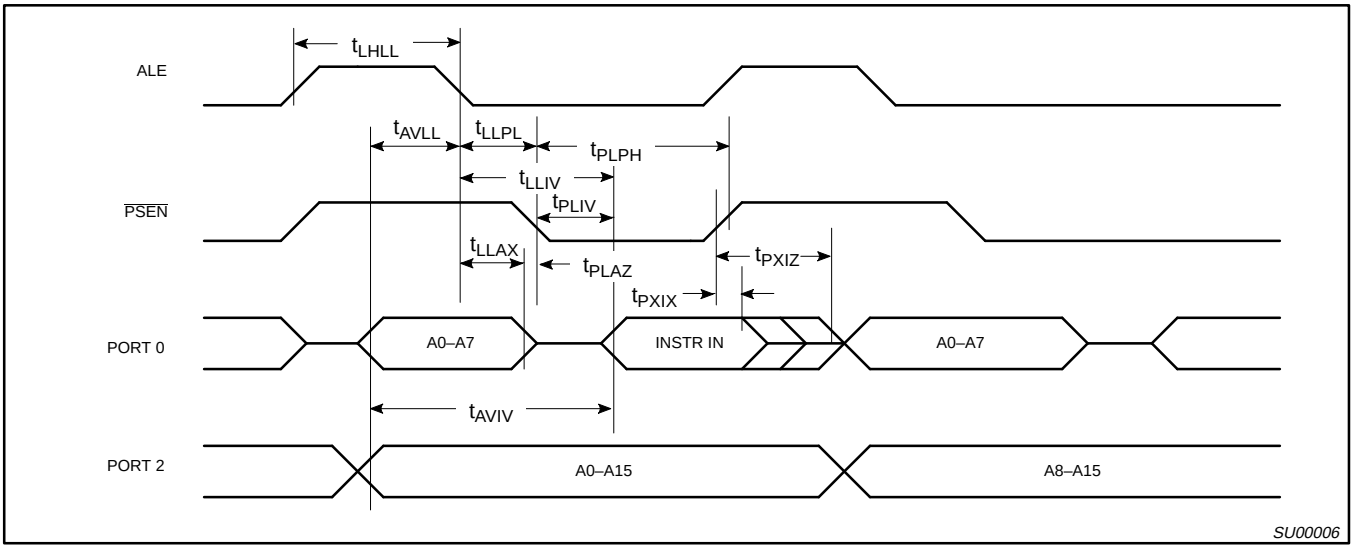


Figure 4. External Program Memory Read Cycle

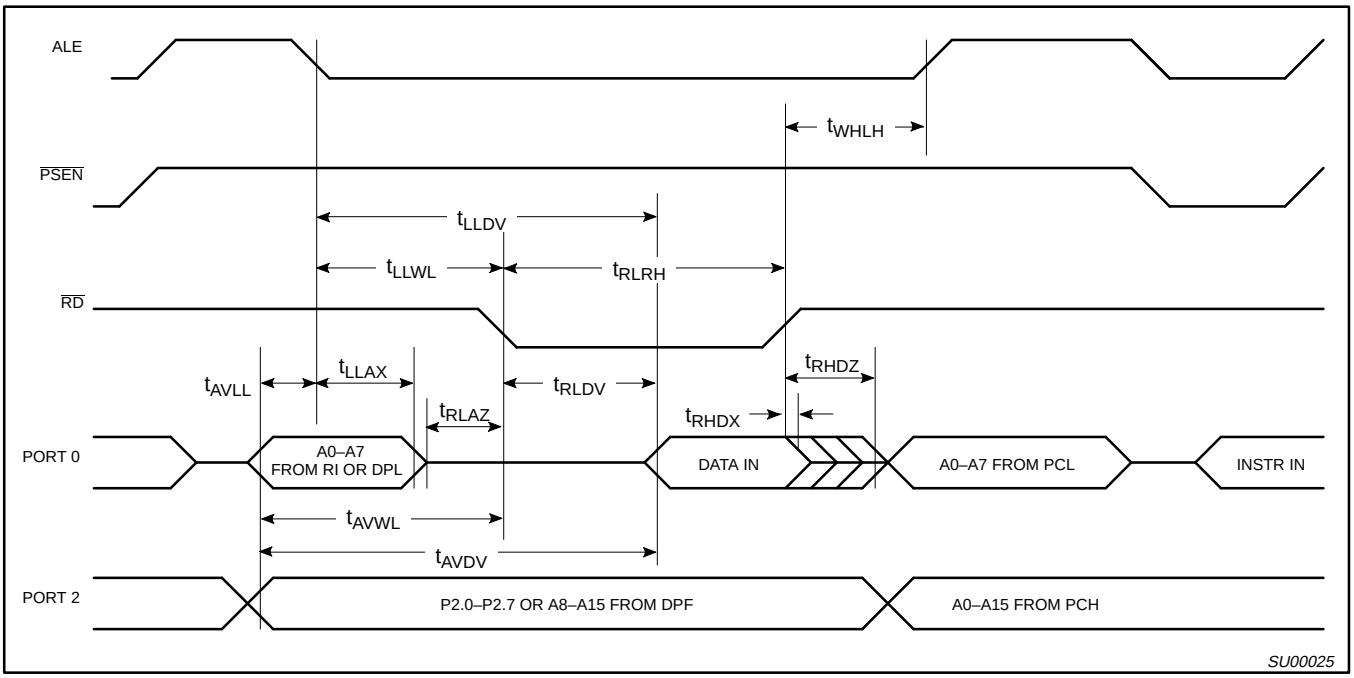


Figure 5. External Data Memory Read Cycle

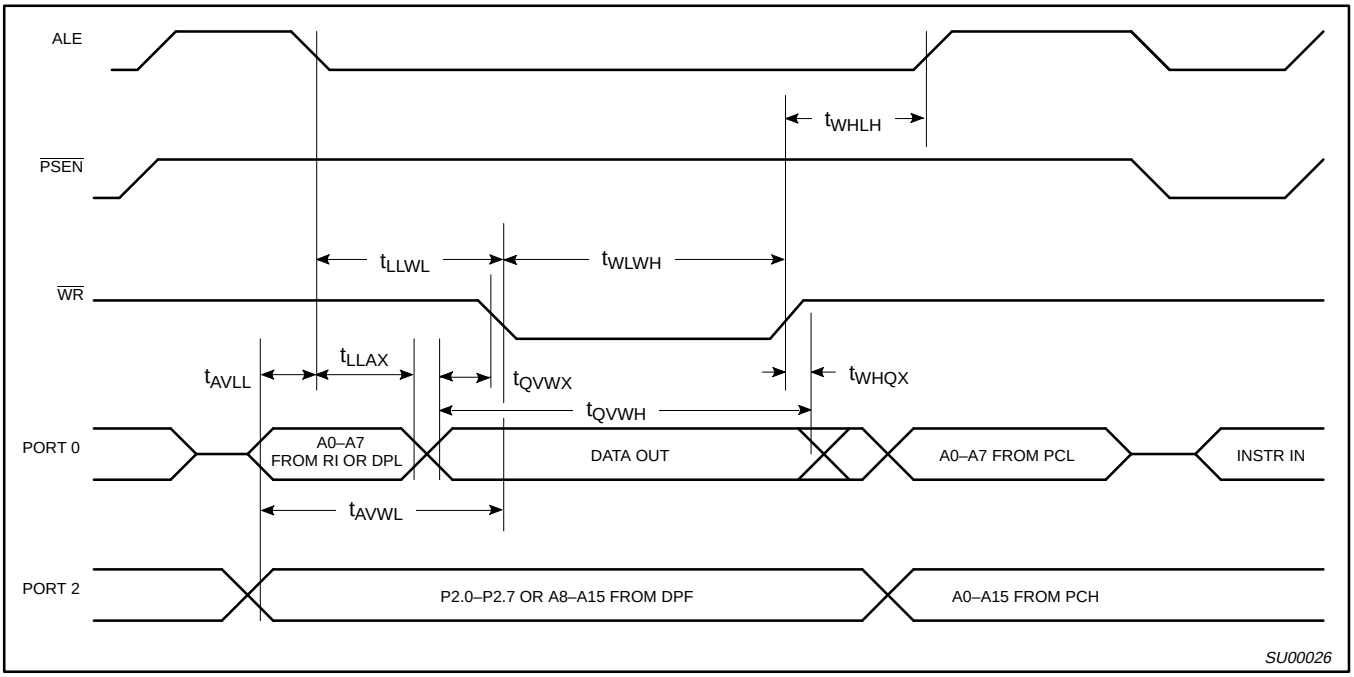


Figure 6. External Data Memory Write Cycle

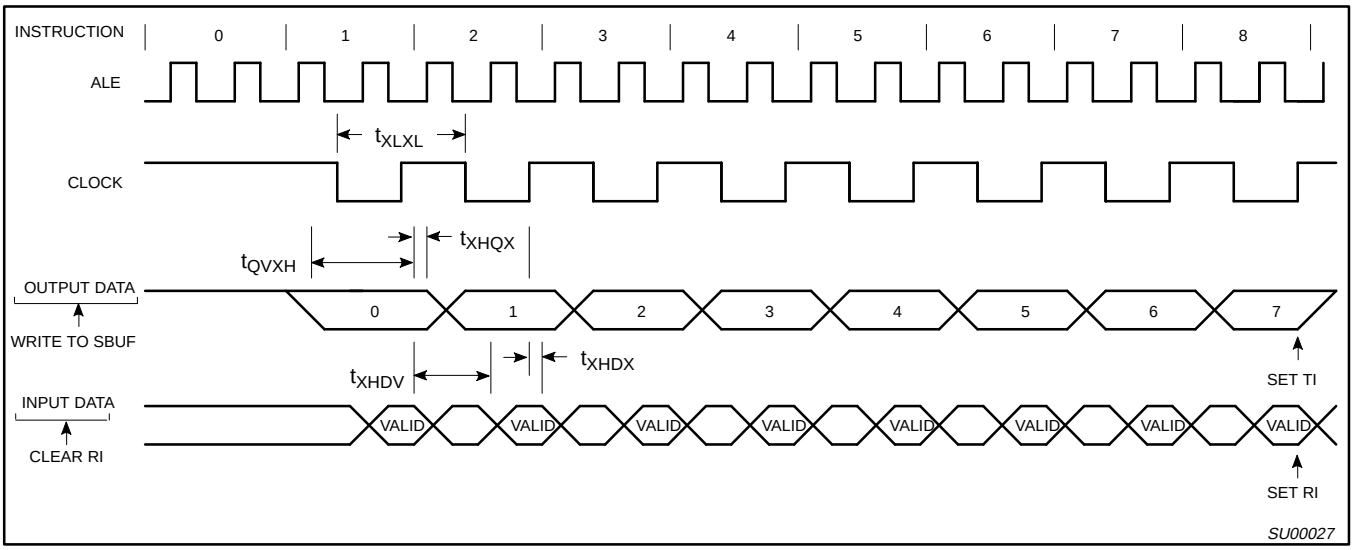


Figure 7. Shift Register Mode Timing

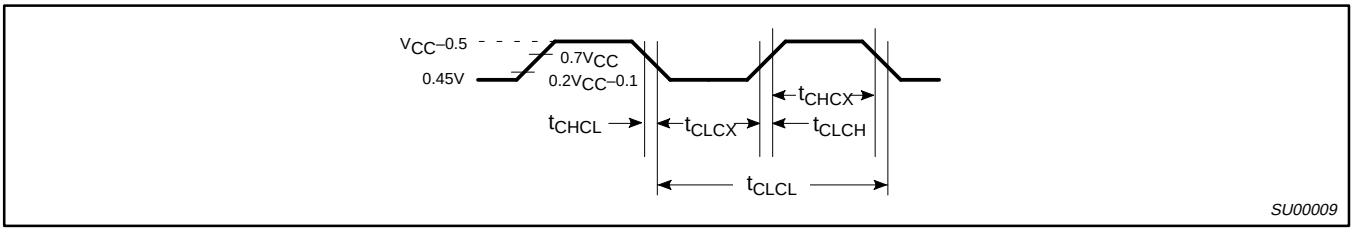
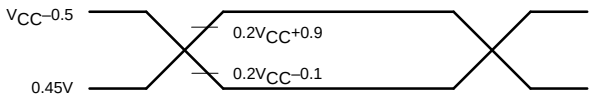


Figure 8. External Clock Drive



NOTE:
AC inputs during testing are driven at V_{CC} –0.5 for a logic '1' and 0.45V for a logic '0'. Timing measurements are made at V_{IH} min for a logic '1' and V_{IL} max for a logic '0'.

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Figure 9. AC Testing Input/Output

NOTE:
For timing purposes, a port is no longer floating when a 100mV change from load voltage occurs, and begins to float when a 100mV change from the loaded V_{OH}/V_{OL} level occurs. $I_{OH}/I_{OL} \geq \pm 20$mA.

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Figure 10. Float Waveform

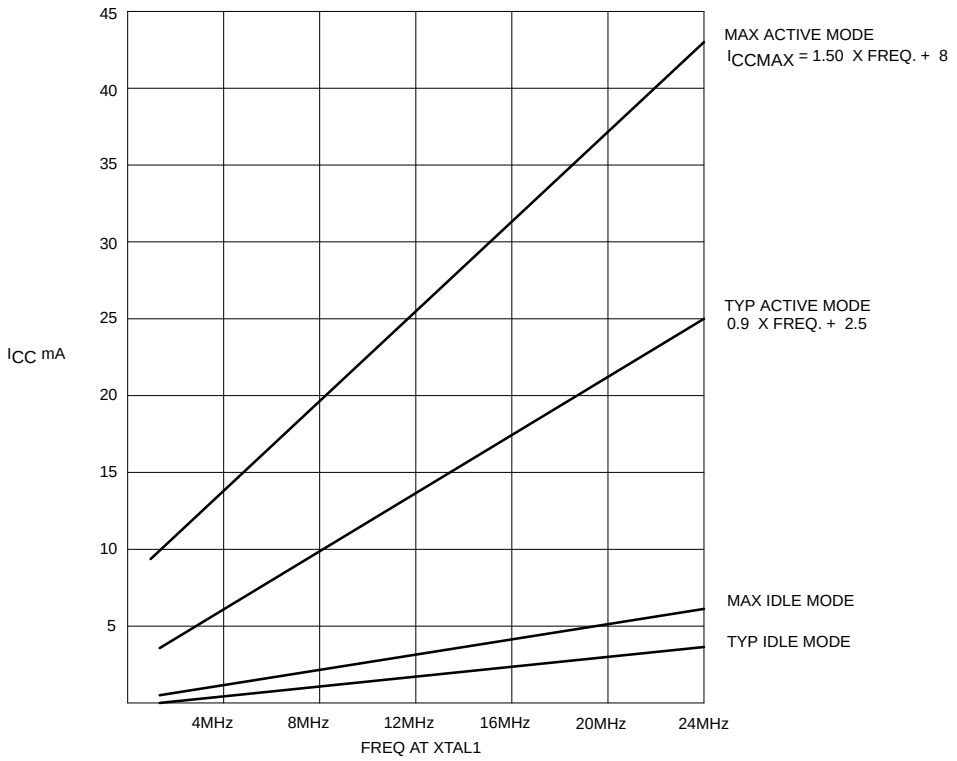

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Figure 11. I_{CC} vs. Frequency

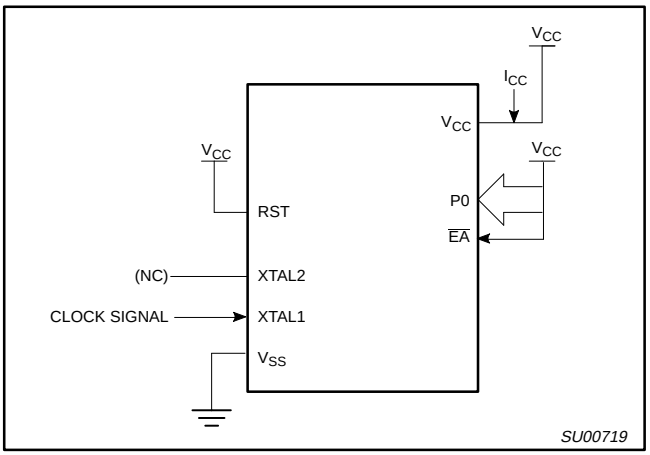

Figure 12. I_{CC} Test Condition, Active Mode
All other pins are disconnected

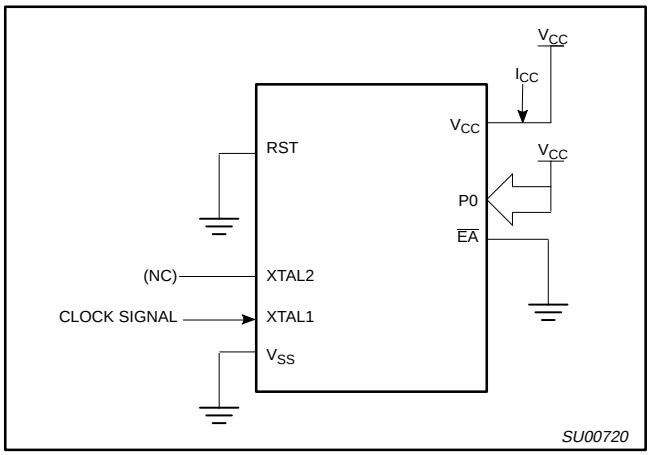

Figure 13. I_{CC} Test Condition, Idle Mode
All other pins are disconnected

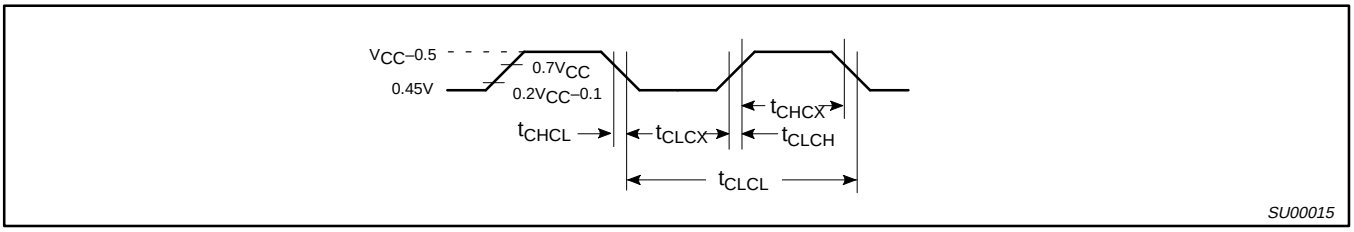

Figure 14. Clock Signal Waveform for I_{CC} Tests in Active and Idle Modes
$t_{CLCH} = t_{CHCL} = 5ns$

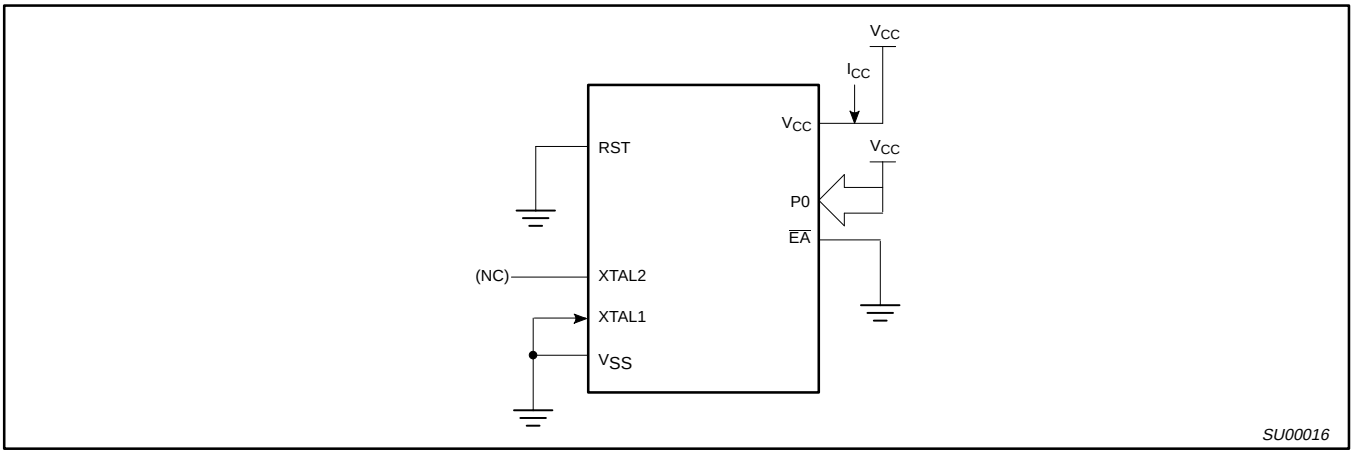

Figure 15. I_{CC} Test Condition, Power Down Mode
All other pins are disconnected. V_{CC} = 2V to 5.5V

EPROM CHARACTERISTICS

The 87C58 is programmed by using a modified Improved Quick-Pulse Programming™ algorithm. It differs from older methods in the value used for V_{PP} (programming supply voltage) and in the width and number of the ALE/$\overline{PROG}$ pulses.

The 87C58 contains two signature bytes that can be read and used by an EPROM programming system to identify the device. The signature bytes identify the device as an 87C58 manufactured by Philips.

Table 4 shows the logic levels for reading the signature byte, and for programming the program memory, the encryption table, and the security bits. The circuit configuration and waveforms for quick-pulse programming are shown in Figures 16 and 17. Figure 18 shows the circuit configuration for normal program memory verification.

Quick-Pulse Programming

The setup for microcontroller quick-pulse programming is shown in Figure 16. Note that the 87C58 is running with a 4 to 6MHz oscillator. The reason the oscillator needs to be running is that the device is executing internal address and program data transfers.

The address of the EPROM location to be programmed is applied to ports 1 and 2, as shown in Figure 16. The code byte to be programmed into that location is applied to port 0. RST, $\overline{PSEN}$ and pins of ports 2 and 3 specified in Table 4 are held at the 'Program Code Data' levels indicated in Table 4. The ALE/$\overline{PROG}$ is pulsed low 5 times as shown in Figure 17.

To program the encryption table, repeat the 25 pulse programming sequence for addresses 0 through 1FH, using the 'Pgm Encryption Table' levels. Do not forget that after the encryption table is programmed, verification cycles will produce only encrypted data.

To program the security bits, repeat the 25 pulse programming sequence using the 'Pgm Security Bit' levels. After one security bit is programmed, further programming of the code memory and encryption table is disabled. However, the other security bit can still be programmed.

Note that the $\overline{EA}$/V_{PP} pin must not be allowed to go above the maximum specified V_{PP} level for any amount of time. Even a narrow glitch above that voltage can cause permanent damage to the device. The V_{PP} source should be well regulated and free of glitches and overshoot.

Program Verification

If security bit 2 has not been programmed, the on-chip program memory can be read out for program verification. The address of the program memory locations to be read is applied to ports 1 and 2 as shown in Figure 18. The other pins are held at the 'Verify Code Data' levels indicated in Table 4. The contents of the address location will be emitted on port 0. External pull-ups are required on port 0 for this operation.

If the 32 byte encryption table has been programmed, the data presented at port 0 will be the exclusive NOR of the program byte with one of the encryption bytes. The user will have to know the encryption table contents in order to correctly decode the verification data. The encryption table itself cannot be read out.

Program/Verify Algorithms

Any algorithm in agreement with the conditions listed in Table 4, and which satisfies the timing specifications, is suitable.

Erasure Characteristics

Erasure of the EPROM begins to occur when the chip is exposed to light with wavelengths shorter than approximately 4,000 angstroms. Since sunlight and fluorescent lighting have wavelengths in this range, exposure to these light sources over an extended time (about 1 week in sunlight, or 3 years in room level fluorescent lighting) could cause inadvertent erasure. **For this and secondary effects, it is recommended that an opaque label be placed over the window.** For elevated temperature or environments where solvents are being used, apply Kapton tape Fluorglas part number 2345–5, or equivalent.

The recommended erasure procedure is exposure to ultraviolet light (at 2537 angstroms) to an integrated dose of at least 15W-s/cm^2. Exposing the EPROM to an ultraviolet lamp of 12,000µW/cm^2 rating for 20 to 39 minutes, at a distance of about 1 inch, should be sufficient.

Erasure leaves the array in an all 1s state.

Security Bits

With none of the security bits programmed the code in the program memory can be verified. If the encryption table is programmed, the code will be encrypted when verified. When only security bit 1 (see Table 5) is programmed, MOVC instructions executed from external program memory are disabled from fetching code bytes from the internal memory, EA is latched on Reset and all further programming of the EPROM is disabled. When security bits 1 and 2 are programmed, in addition to the above, verify mode is disabled. When all three security bits are programmed, all of the conditions above apply and all external program memory execution is disabled.

Encryption Array

32 bytes of encryption array are initially unprogrammed (all 1s).

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Table 4. EPROM Programming Modes

MODE	RST	$\overline{PSEN}$	ALE/$\overline{PROG}$	$\overline{EA}$/V_{PP}	P2.7	P2.6	P3.7	P3.6	P3.3
Read signature	1	0	1	1	0	0	0	0	0
Program code data	1	0	0*	V_{PP}	1	0	1	1	1
Verify code data	1	0	1	1	0	0	1	1	0
Pgm encryption table	1	0	0*	V_{PP}	1	0	1	0	1
Pgm security bit 1	1	0	0*	V_{PP}	1	1	1	1	1
Pgm security bit 2	1	0	0*	V_{PP}	1	1	0	0	1

NOTES:
1. ‘0’ = Valid low for that pin, ‘1’ = valid high for that pin.
2. V_{PP} = 12.75V ±0.25V.
3. V_{CC} = 5V±10% during programming and verification.

* ALE/$\overline{PROG}$ receives 5 programming pulses (only for user array; 25 pulses for encryption or security bits) while V_{PP} is held at 12.75V. Each programming pulse is low for 100µs (±10µs) and high for a minimum of 10µs.

Table 5. Program Security Bits

PROGRAM LOCK BITS[1, 2]			
	SB1	SB2	PROTECTION DESCRIPTION
1	U	U	No Program Security features enabled. (Code verify will still be encrypted by the Encryption Array if programmed.)
2	P	U	MOVC instructions executed from external program memory are disabled from fetching code bytes from internal memory, $\overline{EA}$ is sampled and latched on Reset, and further programming of the EPROM is disabled.
3	P	P	Same as 2, also verify is disabled.

NOTES:
1. P – programmed. U – unprogrammed.
2. Any other combination of the security bits is not defined.

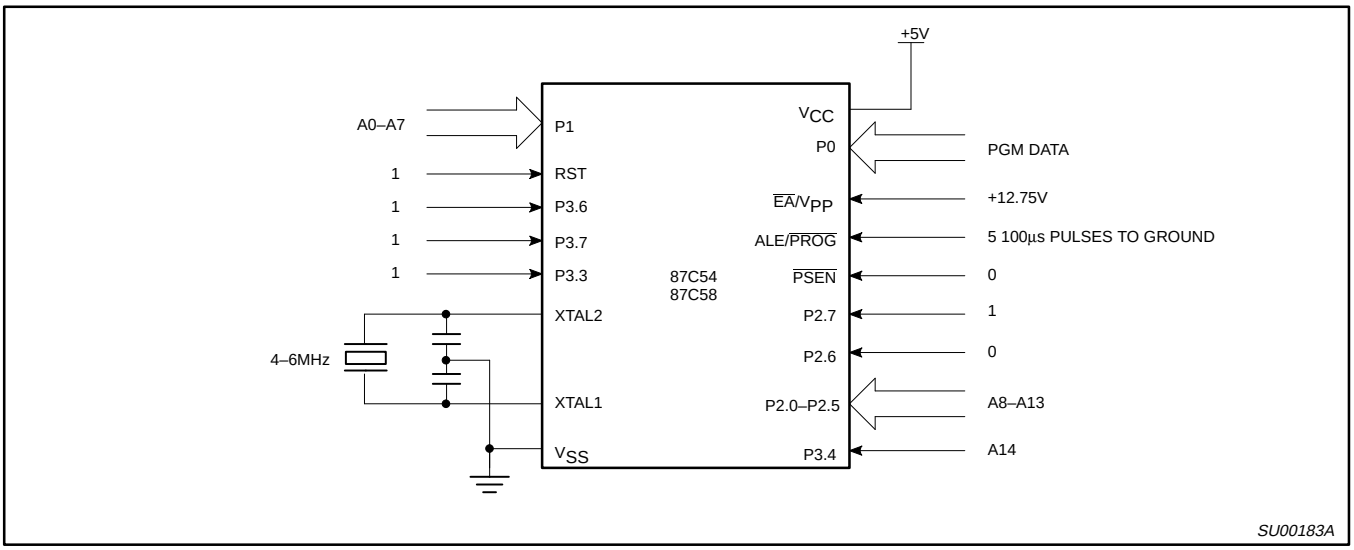


Figure 16. Programming Configuration

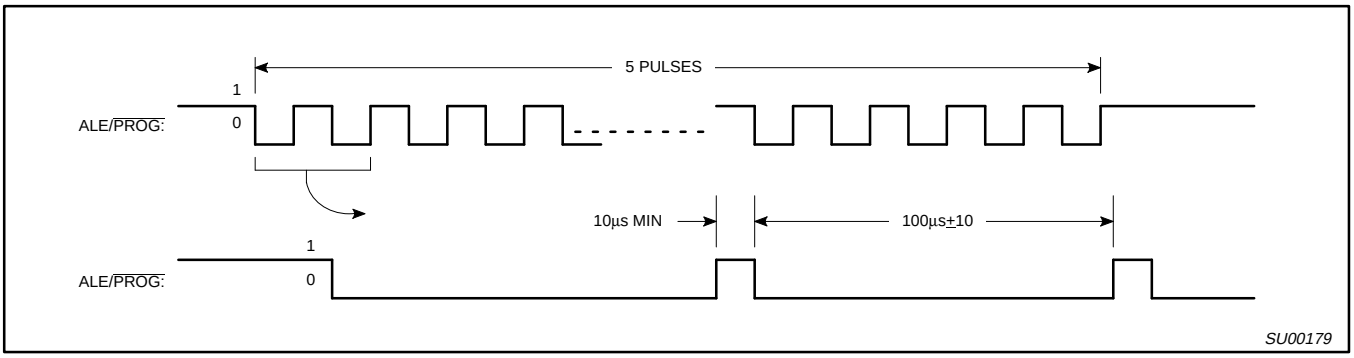


Figure 17. $\overline{\text{PROG}}$ Waveform

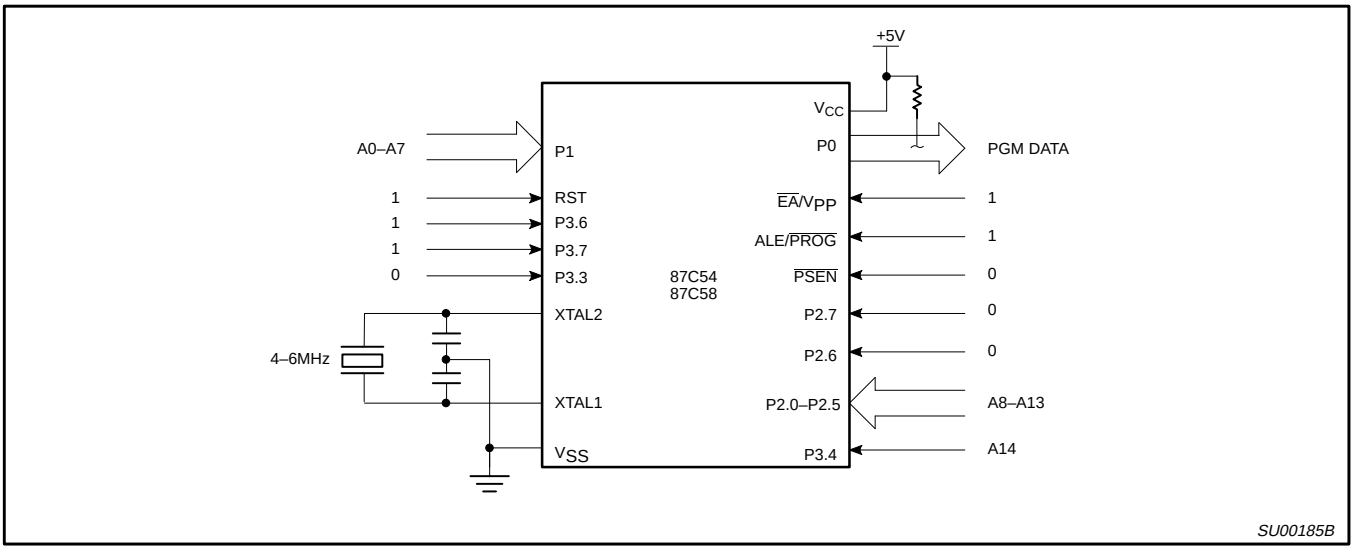


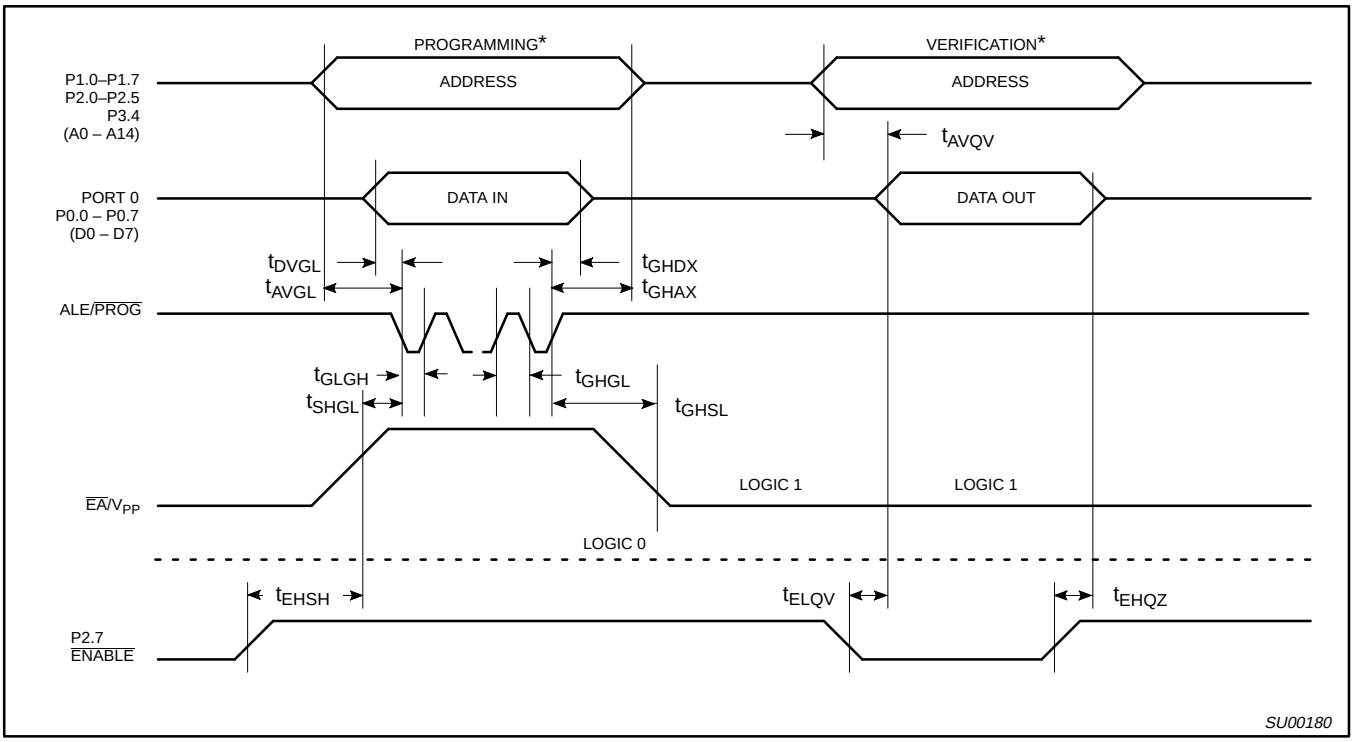
Figure 18. Program Verification

EPROM PROGRAMMING AND VERIFICATION CHARACTERISTICS

T_{amb} = 21°C to +27°C, V_{CC} = 5V±10%, V_{SS} = 0V (See Figure 19)

SYMBOL	PARAMETER	MIN	MAX	UNIT
V_{PP}	Programming supply voltage	12.5	13.0	V
I_{PP}	Programming supply current		50 [1]	mA
$1/t_{CLCL}$	Oscillator frequency	4	6	MHz
t_{AVGL}	Address setup to $\overline{PROG}$ low	$48t_{CLCL}$		
t_{GHAX}	Address hold after $\overline{PROG}$	$48t_{CLCL}$		
t_{DVGL}	Data setup to $\overline{PROG}$ low	$48t_{CLCL}$		
t_{GHDX}	Data hold after $\overline{PROG}$	$48t_{CLCL}$		
t_{EHSH}	P2.7 ($\overline{ENABLE}$) high to V_{PP}	$48t_{CLCL}$		
t_{SHGL}	V_{PP} setup to $\overline{PROG}$ low	10		µs
t_{GHSL}	V_{PP} hold after $\overline{PROG}$	10		µs
t_{GLGH}	$\overline{PROG}$ width	90	110	µs
t_{AVQV}	Address to data valid		$48t_{CLCL}$	
t_{ELQZ}	$\overline{ENABLE}$ low to data valid		$48t_{CLCL}$	
t_{EHQZ}	Data float after $\overline{ENABLE}$	0	$48t_{CLCL}$	
t_{GHGL}	$\overline{PROG}$ high to $\overline{PROG}$ low	10		µs

NOTE:
1. Not tested.



* FOR PROGRAMMING VERIFICATION SEE FIGURE 16.
FOR VERIFICATION CONDITIONS SEE FIGURE 18.

Figure 19. EPROM Programming and Verification