

HFBR-7934Z and HFBR-7934EZ/HZ/EHZ

Four-Channel Pluggable Parallel Fiber Optic Transceiver



Data Sheet

Description

The HFBR-7934Z transceiver is a high performance fiber optic module for parallel optical data communication applications. It incorporates 8 independent data channels (4 for transmit and 4 for receive) operating from 1 to 3.125 Gb/s 8B/10B encoded per channel providing a cost effective solution for very short reach applications requiring 12.5 Gb/s aggregate bandwidth. The module is designed to operate on multimode fiber systems at a nominal wavelength of 850 nm. It incorporates high performance, highly reliable, short wavelength optical devices coupled with proven circuit technology to provide long life and consistent service.

The HFBR-7934Z transceiver module incorporates a 4 channel VCSEL (Vertical Cavity Surface Emitting Laser) array together with a custom 4 channel laser driver integrated circuit providing IEC-825 and CDRH Class 1M laser eye safety. It also contains a 4 channel PIN photodiode array coupled with a custom preamplifier / post amplifier integrated circuit.

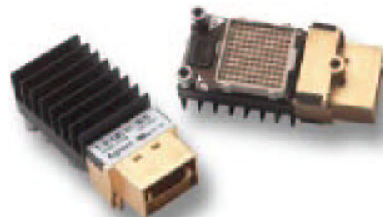
Operating on 3.3 V power supply this module provides LVTTTL/LVCMOS control interfaces and CML compatible high speed data lines which simplify external circuitry. The transceiver is housed in MTP®/MPO receptacle package with integral finned heatsink. Electrical connections to the device are achieved by means of a pluggable 10x10 connector array.

Features

- RoHS Compliant
- Four Transmit and Four Receive Channels; 1 to 3.125 Gb/s 8B/10B encoded per channel
- Compatible with SONET scrambled and 8B10B encoded data formats
- 850 nm VCSEL array source
- Conforms to "POP4" Four-Channel Pluggable Optical Transceiver Multisource Agreement
- 50/125 μ m multimode fiber operation
 - Distance up to 150 m with 500 MHz.km fiber at 3.125 Gb/s
 - Distance up to 350 m with 2000 MHz.km fiber at 3.125 Gb/s
- Pluggable package
- Outputs (Tx & Rx) are squelched for loss of signal
- Control I/O is compatible with LVTTTL and LVCMOS
- Standard MTP® MPO ribbon fiber connector interface
- Integrated heat sink
- Manufactured in an ISO 9002 certified facility
- Rx Signal Detect

Applications

- Telecom and Datacom Switch/Router Rack-to-Rack Connections
- Computer Cluster Interconnects



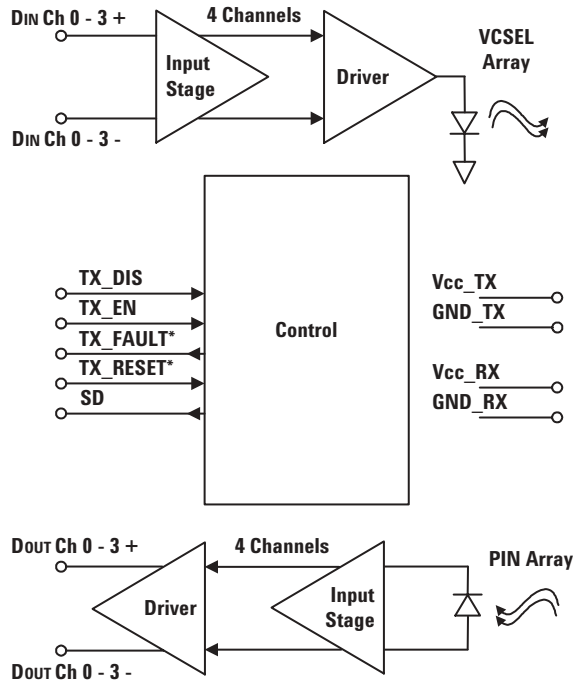


Figure 1 Block Diagram (dimensions in mm)

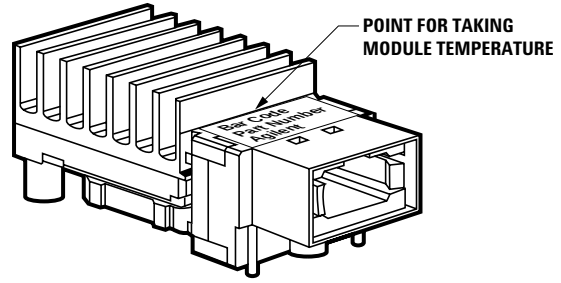


Figure 2 - Case temperature measurement

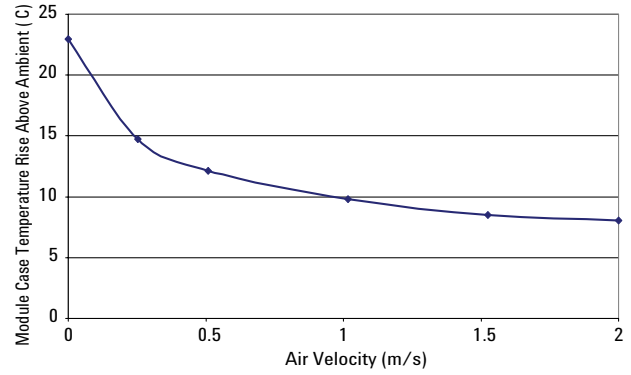
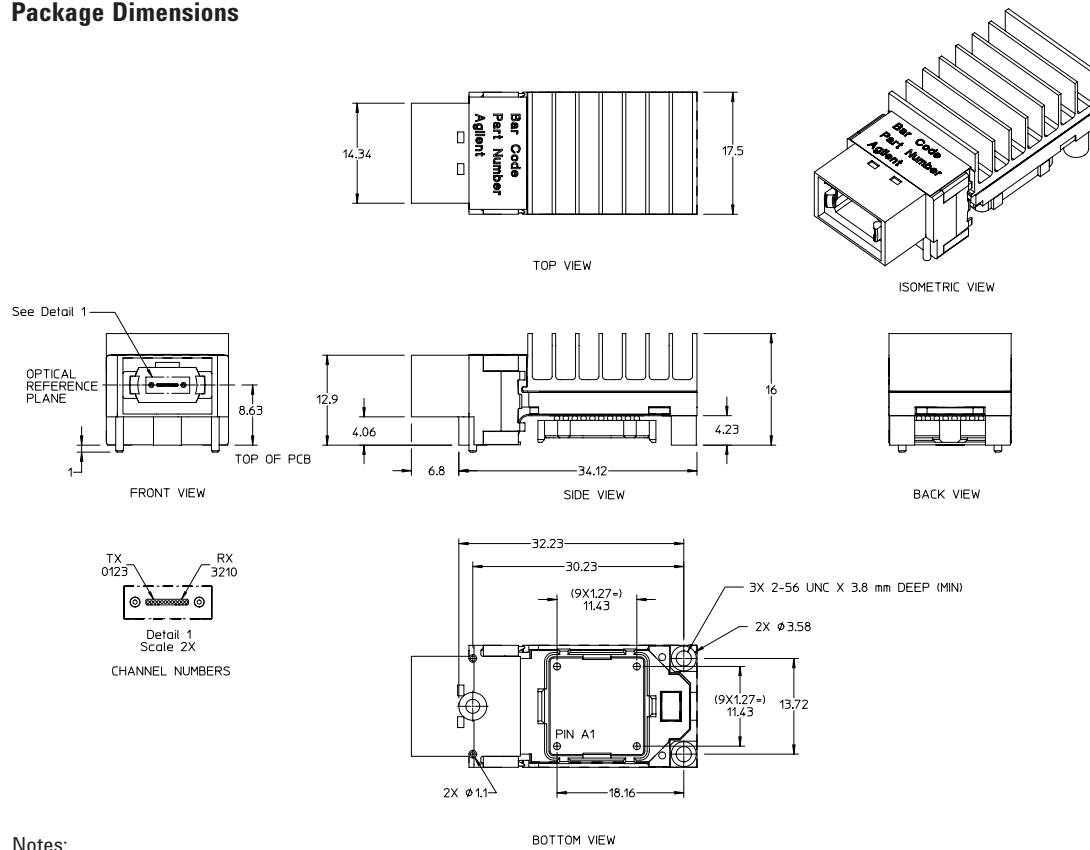


Figure 3 - Ambient air temperature and air flow for $T_c = +80^\circ\text{C}$

Package Dimensions



Notes:

1. Module mass approximately 20 grams.

Figure 4A - HFBR-7934Z Package dimensions (dimensions in mm)

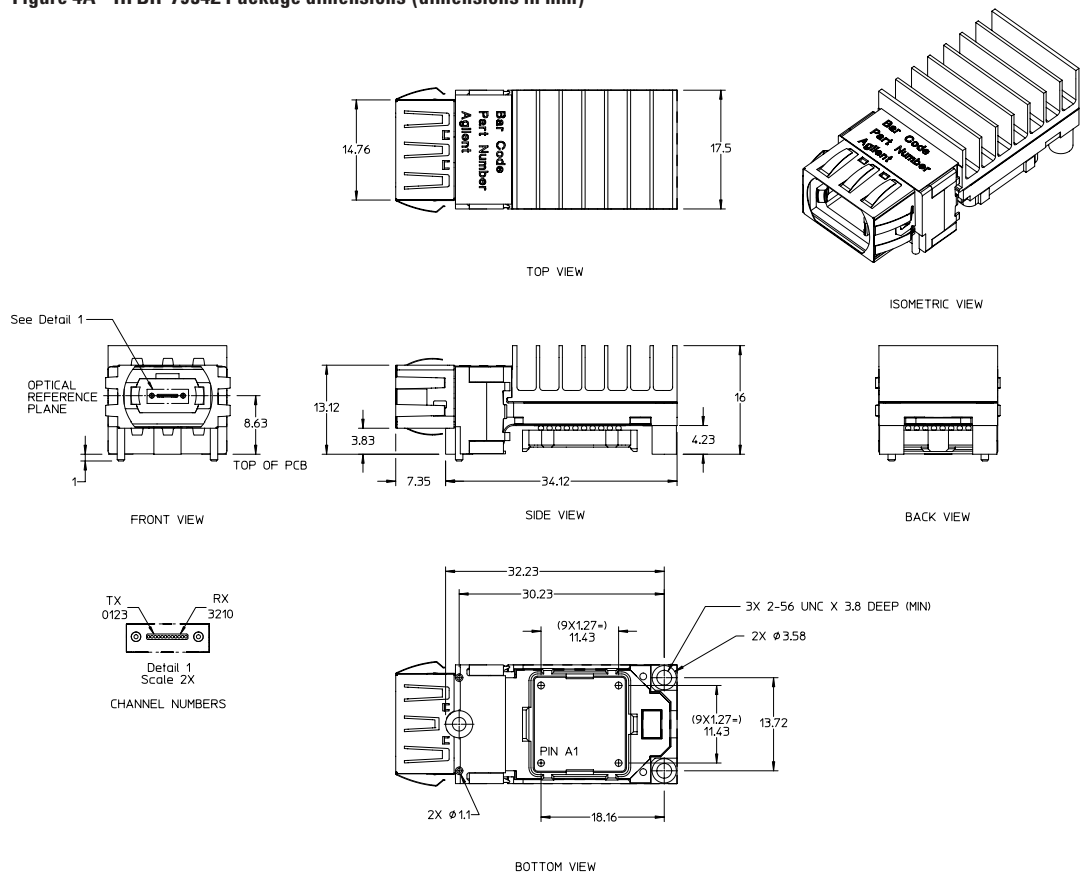


Figure 4B - HFBR-7934EZ Package dimensions (dimensions in mm)

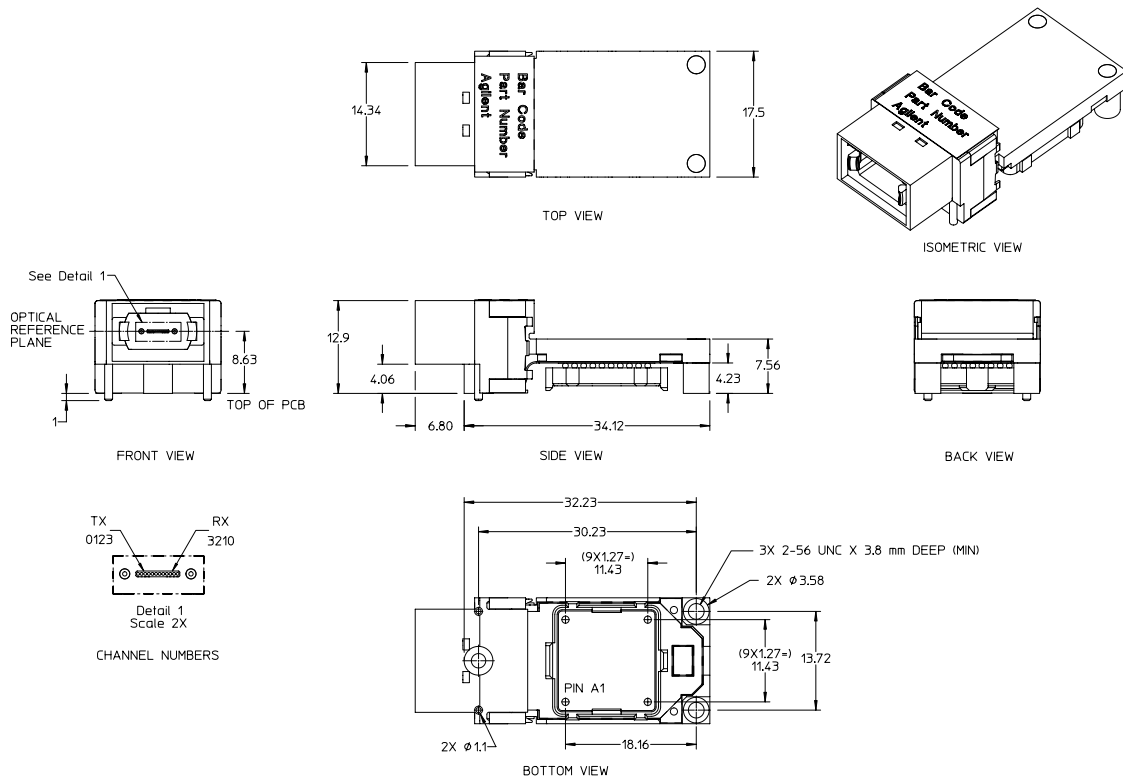


Figure 5A - HFBR-7934HZ Package Dimensions (dimensions in mm)

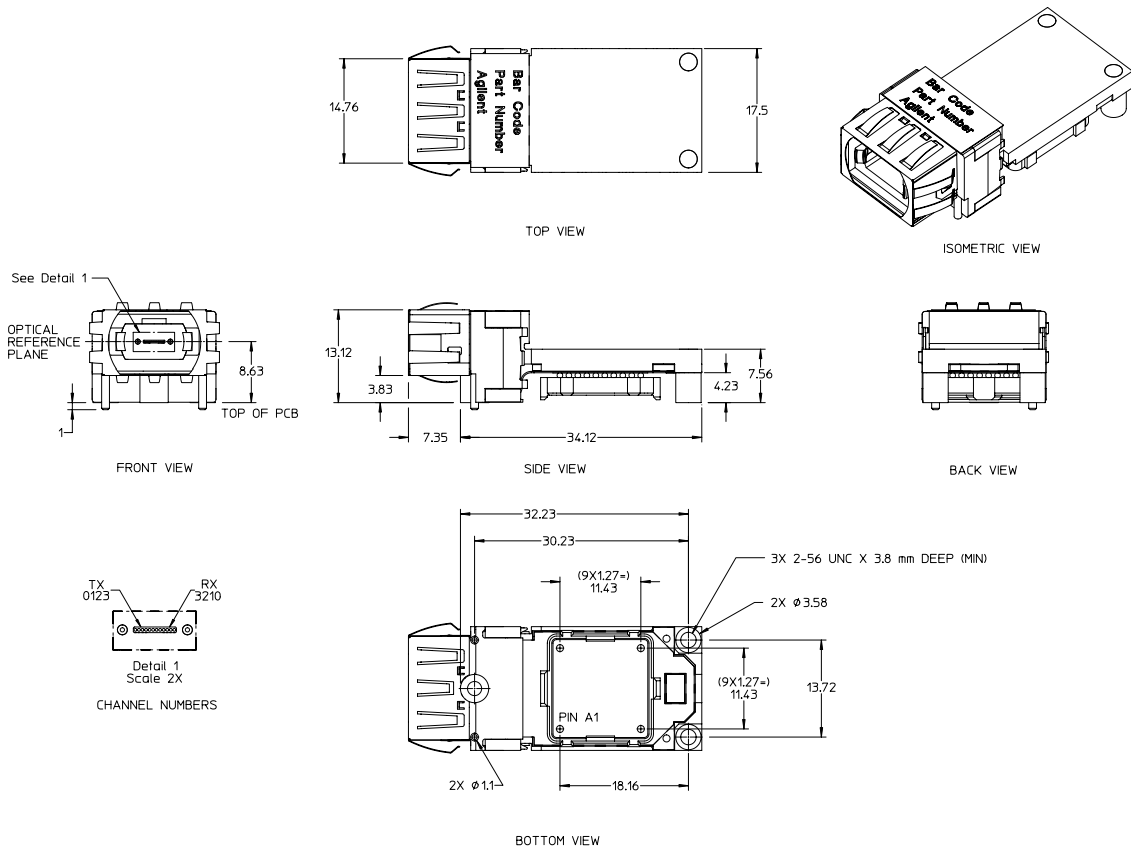
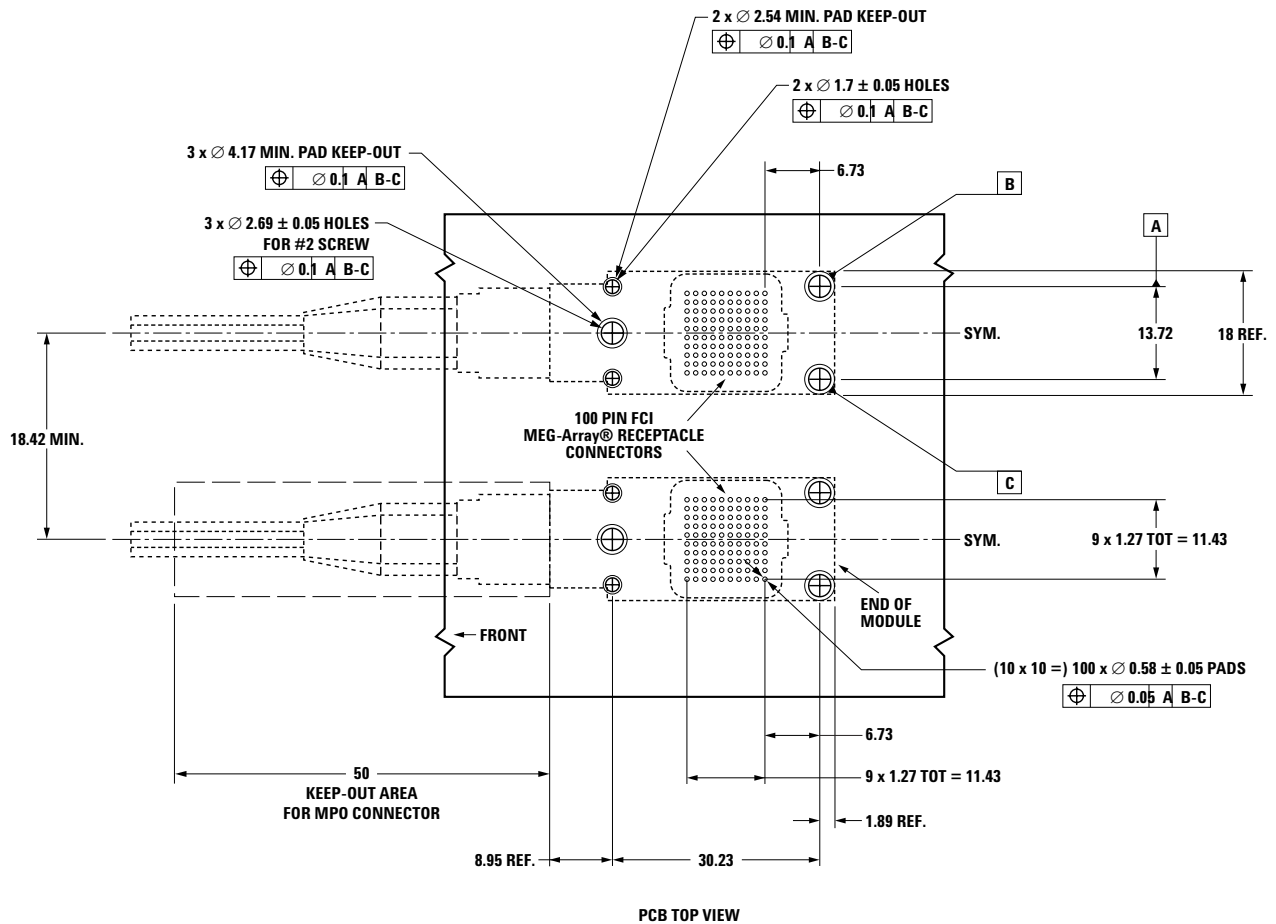


Figure 5B - HFBR-7934EHZ Package Dimensions (dimensions in mm)



NOTE: The host electrical connector attached to the PCB must be a 100-position FCI Meg-Array[®] plug (FCI PN: 84512-102) or equivalent.

Figure 6 - Package Board Footprint (dimensions in mm)

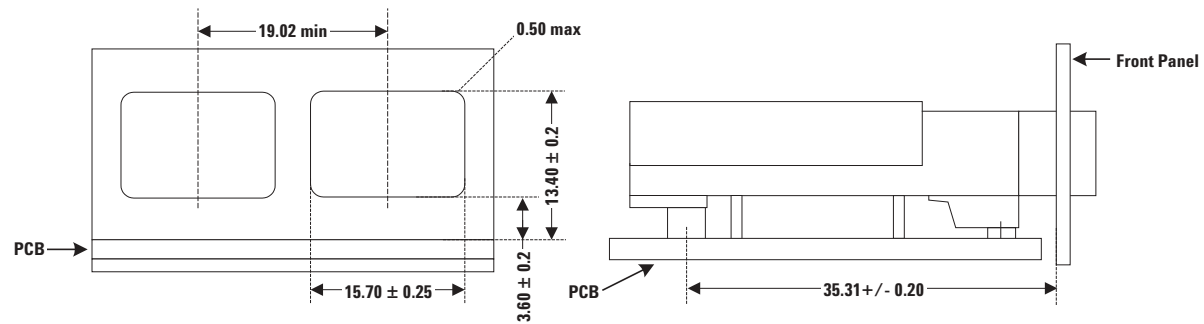


Figure 7 - Host Frontplate Layout (dimensions in mm)

Absolute Maximum Ratings

Stresses in excess of the absolute maximum ratings can cause catastrophic damage to the device. Limits apply to each parameter in isolation, all other parameters having values within the recommended operating conditions. It should not be assumed that limiting values of more than one parameter can be applied to the product at the same time. Exposure to the absolute maximum ratings for extended periods can adversely affect device reliability.

Parameter	Symbol	Minimum	Maximum	Unit	Reference
Storage Temperature	T_s	-40	+100	°C	
Supply Voltage	V_{CC}	-0.5	4.6	V	
Data/Control Signal Input Voltage	V_I	-0.5	$V_{CC} + 0.5$	V	
Transmitter Differential Input Voltage	$ V_D $		2	V	1
Output Current (dc)	I_O		25	mA	
Relative Humidity (Non Condensing)	RH	5	95	%	

Recommended Operating Conditions

Recommended Operating Conditions specify conditions for which the optical and electrical characteristics hold. Optical and electrical characteristics are not specified for operation beyond the Recommended Operating Conditions, reliability is not implied and damage to the device may occur for such operation over an extended time period.

Parameter	Symbol	Minimum	Typical	Maximum	Unit	Reference
Case Temperature	T_C	0		+80	°C	2, Figures 2,
Supply Voltage	V_{CC}	3.135	3.3	3.465	V	Figure 8
Signaling Rate/Channel		1		3.125	GBd	6
Data Input Differential Peak-to-Peak Voltage Swing	ΔV_{DINP-P}	175		1600	mV _{P-P}	3, Figures 11,12
Data Input Rise & Fall Time (20-80%)	t_r, t_f			160	ps	
Control Input Voltage High	V_{IH}	2.0		V_{CC}	V	
Control Input Voltage Low	V_{IL}	V_{EE}		0.8	V	
Power Supply Noise	N_P			200	mV _{P-P}	4, Figure 8
Data I/O Coupling Capacitors	C_{AC}		0.1		μF	5, Figure 9
Receiver Differential Data Output Load	R_{DL}		100		Ω	Figure 9
Transmitter Input Electrical Deterministic Jitter	DJ			0.15 48	UI ps	
Transmitter Input Electrical Total Jitter	TJ			0.33 106	UI ps	

Notes:

1. This is the maximum voltage that can be applied across the Transmitter Differential Data Inputs without damaging the input circuit.
2. Case Temperature is measured as indicated in Figure 2.
3. Data inputs are CML compatible. Coupling capacitors are required to block dc. $\Delta V_{DINP-P} = \Delta V_{DINH} - \Delta V_{DINL}$, where ΔV_{DINH} = High State Differential Data Input Voltage and ΔV_{DINL} = Low State Differential Data Input Voltage.
4. Power Supply Noise is defined at the supply side of the recommended filter for all V_{CC} supplies over the frequency range from 500 Hz to 2700 MHz with the recommended power supply filter in place.
5. For data patterns with restricted run lengths, e.g. 8B10B encoded data, smaller value capacitors may provide acceptable results.
6. 8B/10B encoded

Transmitter Electrical Characteristics

(Over recommended operating conditions: $T_c = 0^\circ\text{C}$ to $+80^\circ\text{C}$, $V_{CC} = 3.3\text{V} \pm 5\%$)

Parameter	Symbol	Minimum	Typical	Maximum	Unit	Reference
Differential Input Impedance	Z_{in}	80	100	120	Ω	1, Figure 9
FAULT* Assert time	T_{OFF}			100	μs	Figure 13
RESET* Assert time	T_{OFF}			7.5	μs	Figure 14
RESET* De-assert time	T_{ON}			18	ms	Figure 14
Transmit Enable (TX_EN) Assert time	T_{ON}			18	ms	Figure 15
Transmit Enable (TX_EN) De-assert time	T_{OFF}			7.5	μs	Figure 15
Transmit Disable (TX_DIS) Assert time	T_{OFF}			7.5	μs	Figure 15
Transmit Disable (TX_DIS) De-assert time	T_{ON}			18	ms	Figure 15
Power-On Initiation Time			21		ms	Figure 17
Control I/Os	Input Current High	$ I_{IH} $		0.5	mA	$2.0\text{ V} \leq V_{IH} \leq V_{CC}$
TX_DIS, TX_EN,	Input Current Low	$ I_{IL} $		0.5	mA	$V_{EE} \leq V_{IH} \leq 0.8\text{ V}$
TX_FAULT*,	Output Voltage Low	V_{OL}	V_{EE}	0.4	V	$I_{OL} = 4.0\text{ mA}$
TX_RESET*	Output Voltage High	V_{OH}	2.4	V_{CC}	V	$I_{OH} = -0.5\text{ mA}$

Transmitter Optical Characteristics

(Over recommended operating conditions: $T_c = 0^\circ\text{C}$ to $+80^\circ\text{C}$, $V_{CC} = 3.3\text{V} \pm 5\%$)

Parameter	Symbol	Minimum	Typical	Maximum	Unit	Reference
Optical Modulation Amplitude	OMA	-7.22			dBm	
Center Wavelength	λ_c	830	850	860	nm	
Spectral Width - rms	σ			0.85	nm rms	
Rise, Fall Time	t_r, t_f		60	100	ps	2
Inter-channel Skew			50	100	ps	3
Relative Intensity Noise OMA	RIN_{12OMA}			-119.5	dB/Hz	
Jitter Contribution	Deterministic	DJ		60	ps	4
	Total	TJ		120	ps	5
Output Optical Power, 50/125 μm , Fiber NA =0.2	P_{OUT}			-2.0	dBm Avg.	6

Notes:

- Differential impedance is measured between D_{IN+} and D_{IN-} over the range 4 MHz to 2 GHz.
- These are unfiltered 20% - 80% values measured with a 550 MBd 101010 pattern.
- Inter-channel Skew is defined for the condition of equal amplitude, zero ps skew input signals.
- Deterministic Jitter (DJ) is defined as the combination of Duty Cycle Distortion (Pulse-Width Distortion) and Data Dependent Jitter. Deterministic Jitter is measured at the 50% signal threshold level using a 3.125 GBd Pseudo Random Bit Sequence of length $2^7 - 1$ (PBR7), or equivalent, test pattern with zero skew between the differential data input signals.
- Total Jitter (TJ) includes Deterministic Jitter and Random Jitter (RJ). Total Jitter is specified at a BER of 10^{-12} for the same 3.125 GBd test pattern as for DJ and is measured with all channels operating.
- The specified optical output power, measured at the output of a 2meter test cable, will be compliant with IEC 60825-1 Amendment 2, Class 1M Accessible Emission Limits, AEL Regulatory Compliance section.

Receiver Electrical Characteristics

(Over recommended operating conditions: $T_c = 0^\circ\text{C}$ to $+80^\circ\text{C}$, $V_{CC} = 3.3\text{V} \pm 5\%$)

Parameter	Symbol	Minimum	Typical	Maximum	Unit	Reference
Differential Output Impedance	Z_{OUT}		100		Ω	1, Figure 9
Data Output Differential Peak-to-Peak Voltage Swing	$\Delta V_{DOUTP-P}$	500	650	800	mV _{P-P}	2, Figure 10
Inter-channel Skew			50	100	ps	3
Data Output Rise, Fall Time	t_r, t_f		120	150	ps	4
Control I/O	Output Voltage Low	V_{OL}	V_{EE}	0.4	V	$I_{OL} = 4.0\text{ mA}$
Signal Detect	Output Voltage High	V_{OH}	2.4	V_{CC}	V	$I_{OH} = -0.5\text{ mA}$
LVTTL & LVCMOS	Assert Time (OFF-to-ON)	t_{SDA}	50		μs	5
Compatible	De-assert Time (ON-to-OFF)	t_{SDD}	50		μs	6
Optical Link Output Deterministic Jitter	DJ			0.4 128	UI ps	7
Optical Link Output Total Jitter	TJ			0.7 225	UI ps	7
Receiver Electrical Output Eye Opening		0.3 96			UI ps	7

Receiver Optical Characteristics

(Over recommended operating conditions: $T_c = 0^\circ\text{C}$ to $+80^\circ\text{C}$, $V_{CC} = 3.3\text{V} \pm 5\%$)

Parameter	Symbol	Minimum	Typical	Maximum	Unit	Reference
Input OMA - Sensitivity	P_{INMIN}	-14.22			dBm OMA	8
Input Optical Power - Saturation	P_{INMAX}	-2.0			dBm avg.	
Operating Center Wavelength	λ_c	830		860	nm	
Return Loss		12			dB	9
Signal Detect	Asserted	P_A	-21	-16	dBm	10
	Deasserted	P_D	-30	-26	dBm	
	Hysteresis	$P_A - P_D$	0.5	1.0	dB	
Contributed Deterministic Jitter	DJ			0.063 20	UI ps	
Contributed Total Jitter	TJ			0.214 68	UI ps	

Notes:

- Measured over the range 4 MHz to 2 GHz.
- $\Delta V_{DOUTP-P} = \Delta V_{DOUTH} - \Delta V_{DOUTL}$, where ΔV_{DOUTH} = High State Differential Data Output Voltage and ΔV_{DOUTL} = Low State Differential Data Output Voltage. ΔV_{DOUTH} and $\Delta V_{DOUTL} = V_{DOUT+} - V_{DOUT-}$, measured with a 100 Ω differential load connected with the recommended coupling capacitors and with a 2500 MBd, 101010 pattern.
- Inter-channel Skew is defined for the condition of equal amplitude, zero ps skew input signals.
- Rise and Fall Times are measured between the 20% and 80% levels using a 550 MHz square wave signal.
- The Signal Detect output will change from logic "0" (Low) to "1" (High) within the specified assert time for a step transition in optical input power from the deasserted condition to the specified asserted optical power level.
- The Signal Detect output will change from logic "1" (High) to "0" (Low) within the specified de-assert time for a step transition in optical input power from the specified asserted optical power level to the deasserted condition.
- Assumes a link where the transmitter is an HFBR-7934Z or equivalent operating per the recommended operating conditions and with maximum cable links.
- Sensitivity is defined as the maximum Input OMA necessary to produce a BER $< 10^{-12}$ at the center of the signal period. For this parameter, input OMA is equivalent to that provided by an ideal source, i.e. one with RIN and switching attributes that do not degrade the sensitivity measurement. All channels not under test are operating receiving data with an average input OMA of up to 6 dB above P_{INMIN} . Sensitivity for signal rates from 1 to 3.125 GBd is defined for 8B/10B encoded data.
- Return loss is defined as the ratio, in dB, of the received optical power to the optical power reflected back down the fiber.
- Signal Detect assertion requires all optical inputs to exhibit a minimum OMA of -16dBm. All channels not under test are operating with PRBS7 patterns, asynchronous with the channel under test, and average input power of up to 6 dB above the specified P_{INMIN} .

General/Control Electrical Characteristics

(Over recommended operating conditions: $T_c = 0^{\circ}\text{C}$ to $+80^{\circ}\text{C}$, $V_{CC} = 3.3\text{V} \pm 5\%$)

Parameter	Symbol	Minimum	Typical	Maximum	Unit	Reference
Supply Current	I_{CC}		300	420	mA	
Power Dissipation	P_{DIST}	1.0	1.46		W	

Regulatory Compliance

The overall equipment design will determine the certification level. The module performance is offered as a figure of merit to assist the designer in considering their use in equipment designs.

Electrostatic Discharge (ESD)

There are two design cases in which immunity to ESD damage is important.

The first case is during handling of the module prior to mounting it on the circuit board. It is important to use normal ESD handling precautions for ESD sensitive devices. These precautions include using grounded wrist straps, workbenches and floor mats in ESD controlled areas. The module performance has been shown to provide adequate performance in typical industry production environments.

The second case to consider is static discharges to the exterior of the equipment chassis containing the module parts. To the extent that the MT-based connector receptacle is exposed to the outside of the equipment chassis it may be subject to whatever system-level ESD test criteria that the equipment is intended to meet. The module performance exceeds typical industry equipment requirements of today.

Electromagnetic Interference (EMI)

Most equipment designs using these high-speed modules from Avago Technologies will be required to meet the requirements of FCC in the United States, CENELEC EN55022 (CISPR 22) in Europe and VCCI in Japan. These modules, with their shielded design, perform to the limits listed in Table 1 to assist the designer in the management of the overall equipment EMI performance.

Immunity

Equipment utilizing these modules will be subject to radio frequency electromagnetic fields in some environments. These modules have good immunity to such fields due to their shielded design.

Eye Safety

These 850 nm VCSEL-based transceiver modules provide eye safety by design.

The HFBR-7934Z has been registered with CDRH and certified by TUV as a Class 1M device under Amendment 2 of IEC 60825-1. See the Regulatory Compliance Table for further detail. If Class 1M exposure is possible, a safety-warning label should be placed on the product stating the following:

LASER RADIATION
DO NOT VIEW DIRECTLY WITH OPTICAL
INSTRUMENTS.
CLASS 1M LASER PRODUCT

MTP®(MPO) Optics Cleaning Statement

The optical port has recessed optics that are visible through the nose of the port. The port plug provided should be installed whenever a fiber cable is not connected. This ensures the optics remain clean and no cleaning should be necessary. In the event of the optics being contaminated, forced nitrogen or dry clean air at less than 20 psi is the recommended cleaning agent. The features of the optical port and guide pins preclude the use of any solid instrument. Liquids are not advised due to potential damage.

Application of wave soldering, reflow soldering and/or aqueous wash processes with the HFBR-7934Z modules device on board is not recommended as damage may occur.

Normal handling precautions for electrostatic sensitive devices should be taken (see ESD section).

Table 1 - Regulatory Compliance

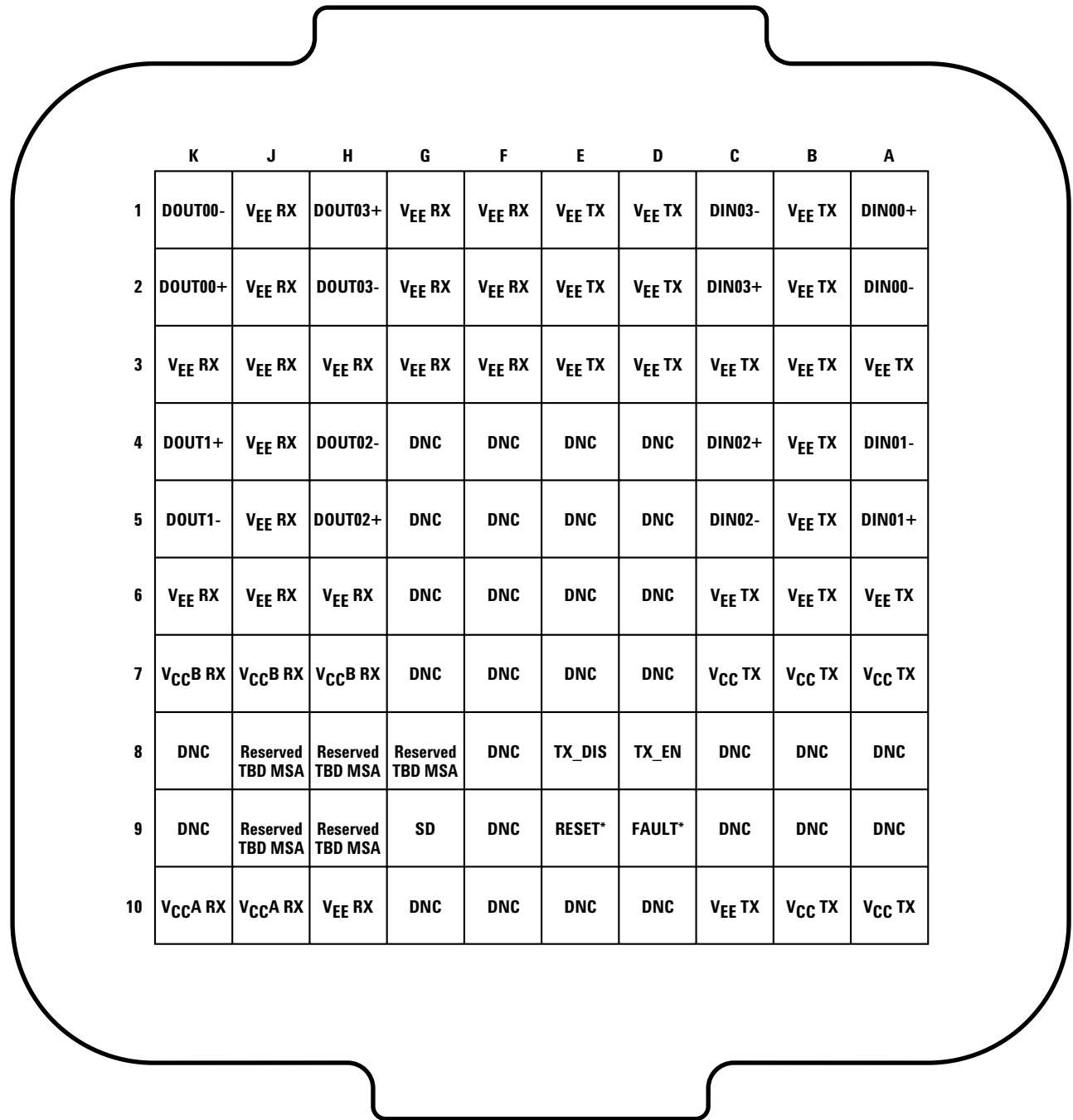
Feature	Test Method	Performance
Electrostatic Discharge (ESD to the Electrical Pads)	JEDEC Human Body (HBM) (JESD22-A114-B)	Module > 1000 V
	JEDEC Machine Model (MM)	Module > 50 V
Electrostatic Discharge (ESD to the Connector Receptacle)	Variation of IEC 61000-4-2	Typically withstand at least 6 kV (module biased) without damage when the connector receptacle is contacted by a Human Body Model probe
Electromagnetic Interference (EMI)	FCC Class B	Typically pass with 5 dB margin.
	CENELEC EN55022 Class B (CISPR 22A) VCCI Class 1	(See Notes 24 and 25)
Immunity	Variation of IEC 61000-4-3	Typically show no measurable effect from a 10 V/m field swept from 80 MHz to 1 GHz applied to the module without a chassis enclosure.
Laser Eye Safety and Equipment Type Testing	IEC 60825-1 Amendment 2	IEC AEL & US FDA CDRH Class 1M
	CFR 21 Section 1040	CDRH Accession Number: 9720151-22 TUV Bauart License: E2171095.04
Component Recognition	Underwriters Laboratories and Canadian Standards Association Joint Component Recognition for Information Technology Equipment Including Electrical Business Equipment.	UL File Number: E173874
RoHS Compliance		Less than 1000 ppm of cadmium, lead, mercury, hexavalent chromium, polybrominated biphenyls, and polybrominated biphenyl ethers.

Notes:

24. EMI performance only refers to shielded version (HFBR-7934EZ and HFBR-7934HEZ).

25. EMI performance could be improved by connecting the following pads to electrical ground : C9, G7 and H9.

4+4 Transceiver Module Pad Assignment - HFBR-7934Z



TOP VIEW (PCB LAYOUT)
(10 x 10 ARRAY)

Table 2. Transceiver Module Pad Description

Symbol	Functional Description
Din Ch 0 - 3 +/- through Din Ch 0 - 3 +/-	Transmitter differential data inputs for channels 0 through 3: Data inputs are CML compatible.
TX_DIS	Transmitter Disable: LVCMOS Input (Internal pull down). Control input used to turn off the transmitter optical outputs. High Active. VCSEL array is off when High. Normal operation is enabled when Low.
TX_EN	Transmitter Enable: LVCMOS Input (Internal pull up). Control input used to enable the transmitter optical outputs. High Active. VCSEL array is off when Low. Normal operation is enabled when High.
TX_FAULT*	Transmitter Fault: LVCMOS Output. Transmitter status output indicating an eye-safety over-current condition for any VCSEL, an out of temperature range condition and/or a calibration data corruption detection. High output state indicates normal operation. Low output state indicates the fault condition. An asserted FAULT* condition disables the VCSEL array and is cleared by TX_RESET*.
TX_RESET*	Transmitter Reset: LVCMOS Input (Internal pull up). Control input used to reset the transmitter logic functions. Active Low. VCSEL array is off when Low. Normal operation is enabled when High.
V _{EE_TX}	Transmitter signal common. All transmitter voltages are referenced to this potential unless otherwise stated. Directly connect these pads to the PC board transmitter ground plane.
V _{CC_TX}	Transmitter power supply.
Dout Ch 0 - 3 +/- through Dout Ch 0 - 3 +/-	Receiver differential data outputs for channels 0 through 3: Data outputs are CML compatible. Data outputs are squelched for de-asserted Signal Detect.
SD	Receiver Signal Detect: LVCMOS Output. Receiver status output indicating valid signal in all channels. High output state (asserted) indicates valid optical inputs to each and every channel. Low output state (de-asserted) indicates loss of signal at any of the monitored receiver inputs. All channels are monitored.
DNC	Do NOT Connect. Do not connect to any electrical potential.
V _{EE_RX}	Receiver signal common. All receiver voltages are referenced to this potential unless otherwise stated. Directly connect these pads to the PC board receiver ground plane.
V _{CCA_RX}	Pin preamplifier power supply rail.
V _{CCB_RX}	Receiver quantizer power supply rail.
V _{CCA_RX} and V _{CCB_RX} can be connected to the same power supply. However, to insure maximum receiver sensitivity and minimize the impact of noise from the power supply, it is recommended to keep the power supplies separate and to use the recommended power supply filtering network on V _{CCA_RX} (see Figure 8).	
Module Case	Transceiver Case Common. Transceiver Case Common incorporates all exposed conductive surfaces and is electrically isolated from Transmitter Signal Common and Receiver Signal Common.

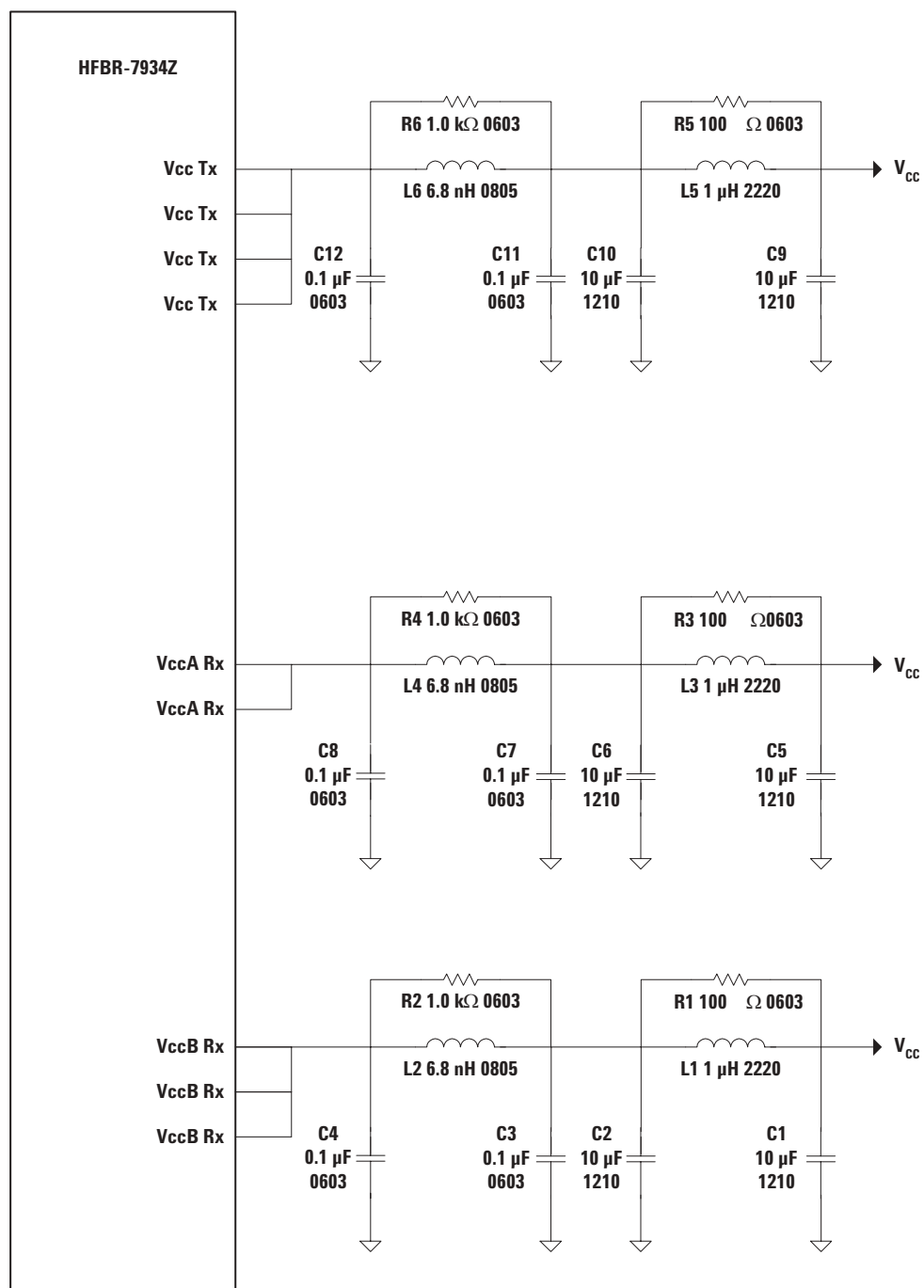
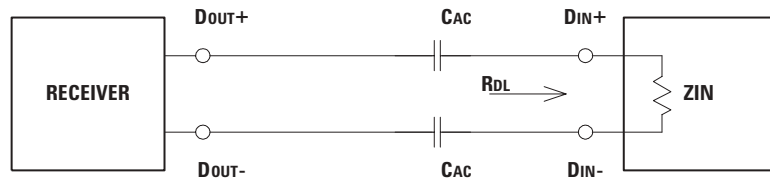


Figure 8 - Recommended power supply filter



AC COUPLING CAPACITORS (DC BLOCKING CAPACITORS) SHOULD BE USED TO CONNECT DATA OUTPUTS TO THE LOAD. THE DIFFERENTIAL DATA PAIR SHOULD BE TERMINATED WITH A DIFFERENTIAL LOAD, R_{DL} , OF $100\ \Omega$ USING EITHER AN INTERNAL LOAD, Z_{IN} , AS SHOWN ABOVE, OR AN EXTERNAL LOAD, IF NECESSARY.

Figure 9 - Recommended AC coupling and data signal termination

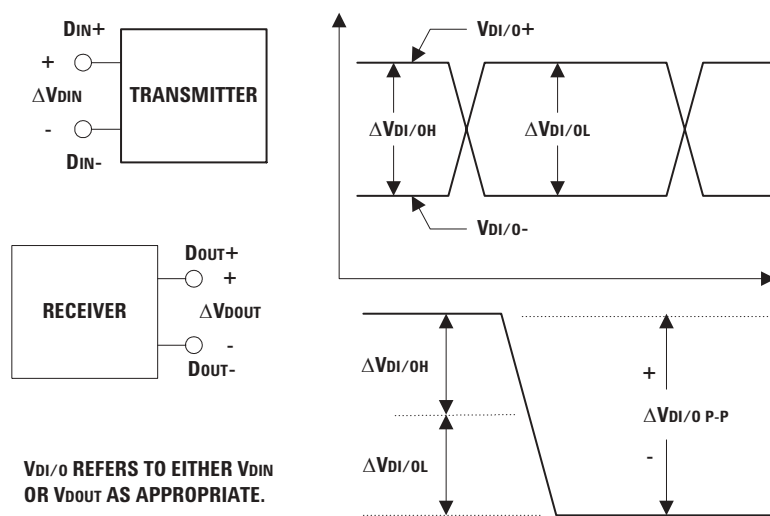


Figure 10 - Differential signals

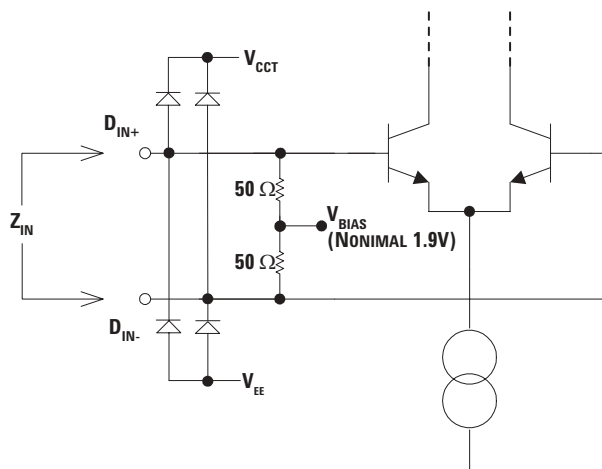


Figure 11 - Transmitter data input equivalent circuit

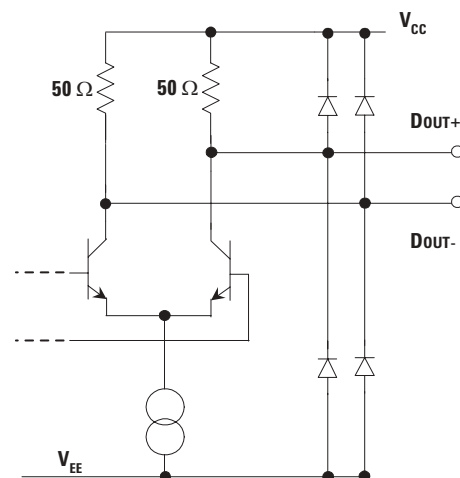


Figure 12 - Receiver data output equivalent circuit.

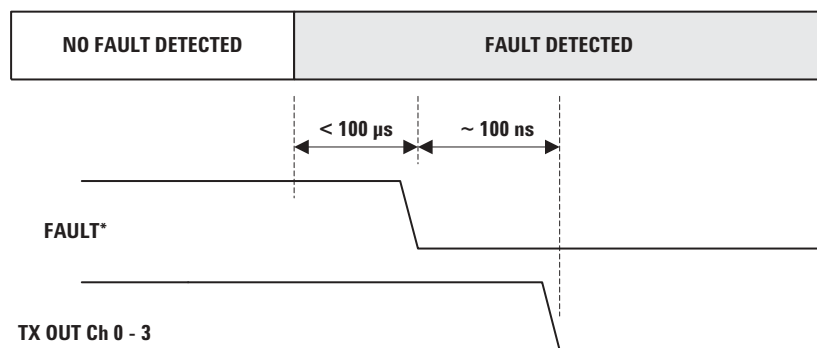


Figure 13 - Transmitter FAULT* signal timing diagram

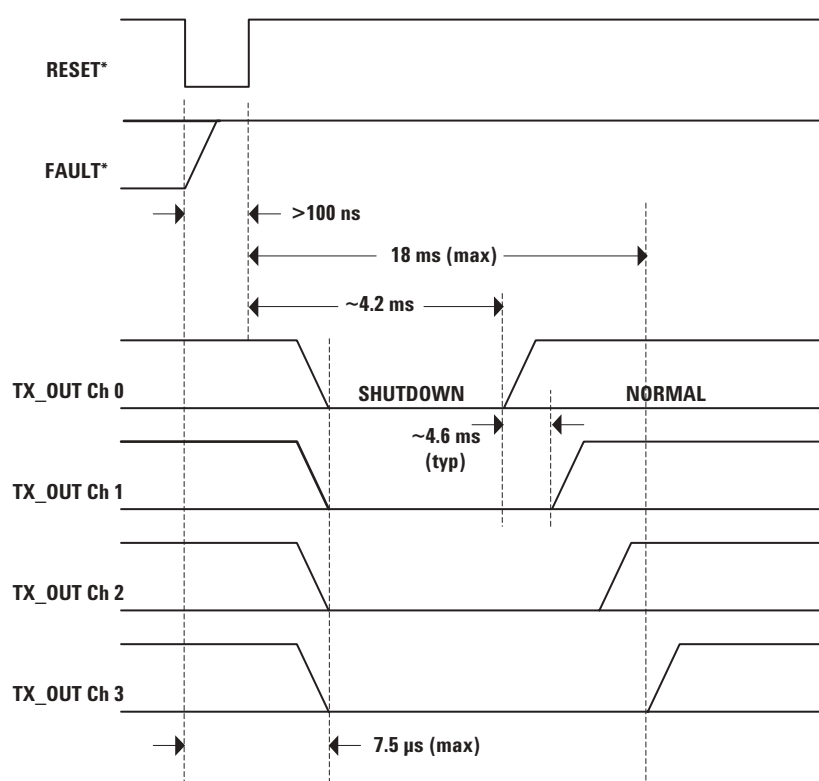


Figure 14 - Transmitter RESET* timing diagram

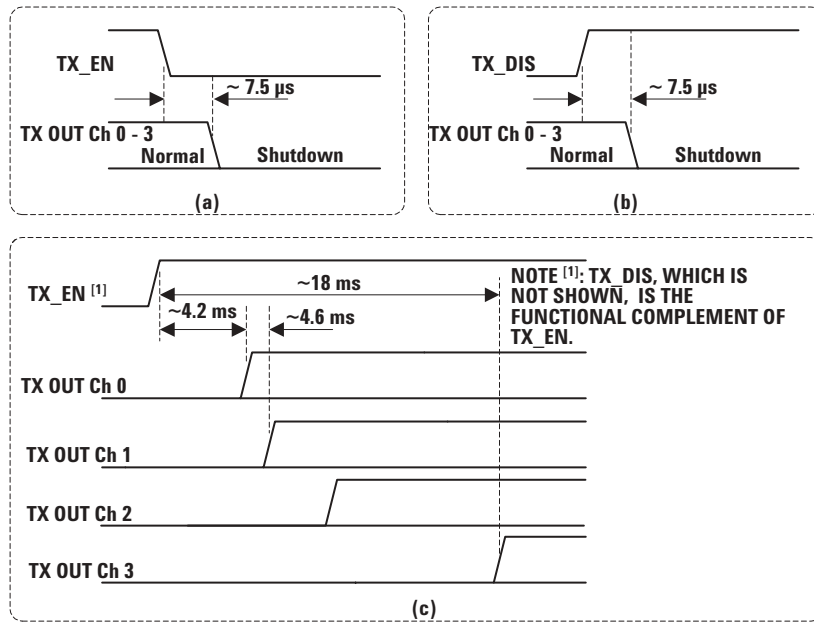
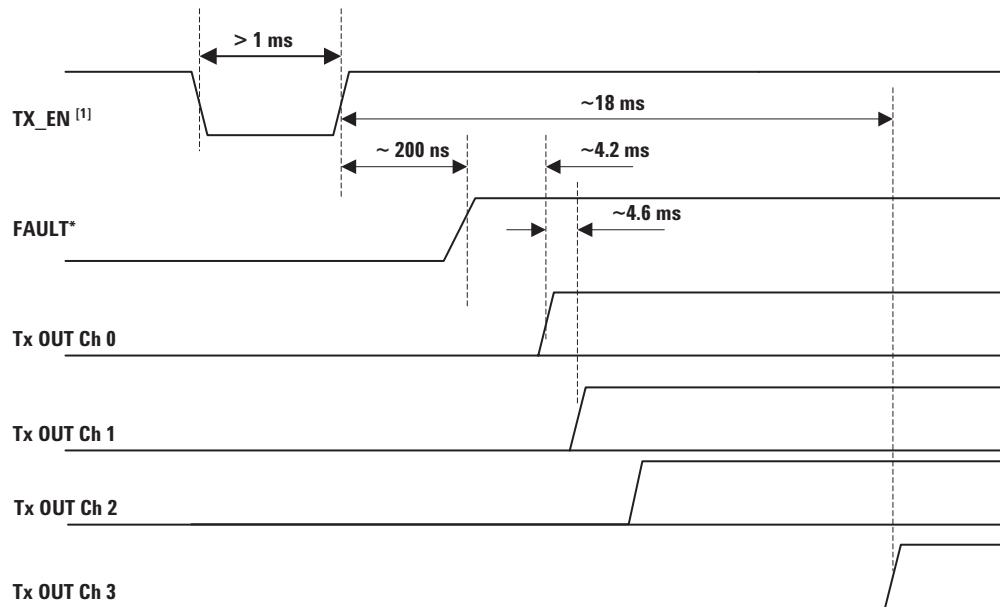


Figure 15 - Transmitter TX_EN and TX_DIS timing diagram



NOTE ^[1]. TX_DIS, WHICH IS NOT SHOWN, IS THE FUNCTIONAL COMPLEMENT OF TX_EN.

Figure 16 - Transmitter fault recovery via TX_EN timing diagram

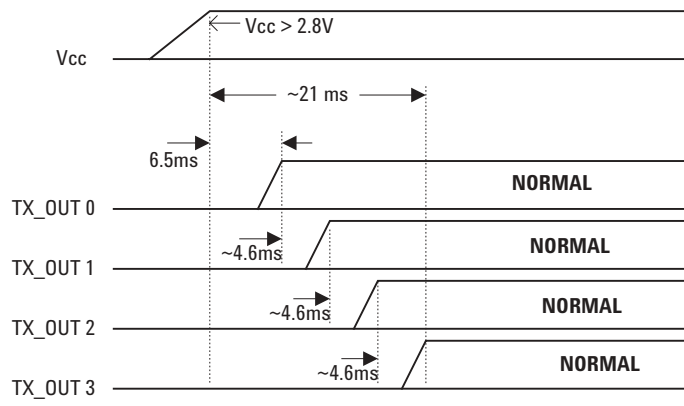


Figure 17. Typical Transmitter Power-Up Sequence

Ordering Information

The HFBR-7934Z product is available for production orders through the Avago Technologies Component Field Sales Office.

HFBR-7934Z	No EMI Nose Shield, with heatsink
HFBR-7934EZ	with EMI Nose Shield, with heatsink
HFBR-7934HZ	No heatsink, No EMI Nose Shield
HFBR-7934EHZ	No heatsink, with EMI Nose Shield

For product information and a complete list of distributors, please go to our web site: www.avagotech.com

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