DM632

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16-CHANNEL CONSTANT CURRENT LED DRIVER
WITH PROGRAMMABLE PWM OUTPUTS

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DM632

16-CHANNEL CONSTANT CURRENT LED DRIVER WITH PROGRAMMABLE PWM OUTPUTS

General Description

DM632 is a 16-channel constant current sink LED driver. Each channel has adjustable 16-bits (65536 steps) grayscale PWM control current outputs. It incorporates shift registers, data latches, constant current circuitry with current value set by an external resistor, selectable oscillator source for PWM functioning, and built-in LED open detection circuit to detect error status. It is specifically designed for LED display or lighting applications.

Features

- Constant-current outputs: 5mA to 90mA adjustable by one external resistor
- 16-bit linear PWM control current outputs for each channel
- Maximum output voltage: 17V
- Maximum clock frequency: 25MHz
- Selectable internal/external PWM reference clock
- PWM free-running capability (refresh rate (~ 275Hz) with internal oscillator (~ 18 MHz))
- Build-in real-time open detection
- Package and pin assignment (except QFN32) compatible to pure LED driver series (ST2221C, DM134/5/6, DM13C)
- Power supply voltage: 3.3V to 5.5V

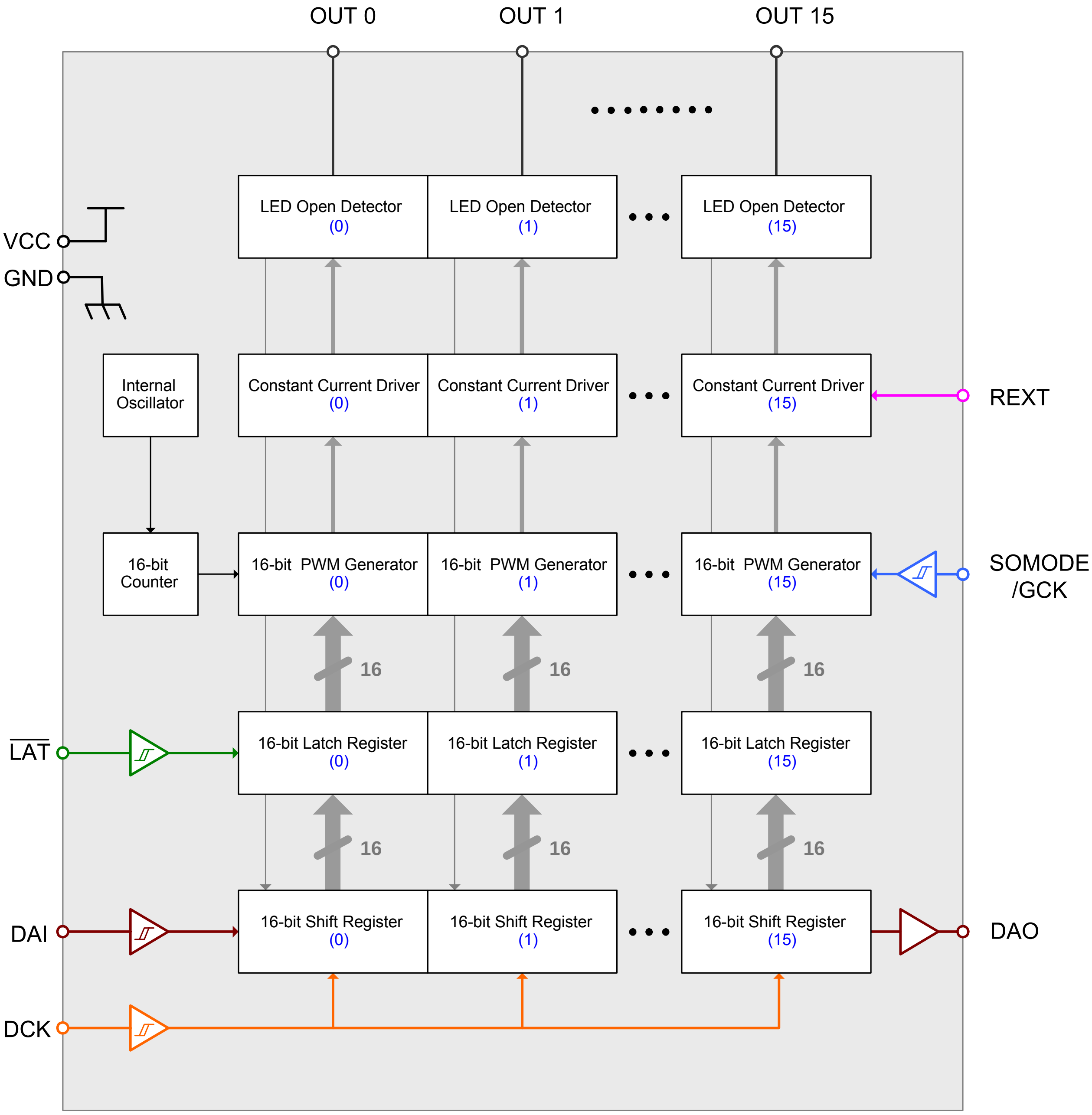
Applications

- Indoor/Outdoor LED Video Display
- LED Variable Message Signs (VMS) System
- LED Decorative Lighting

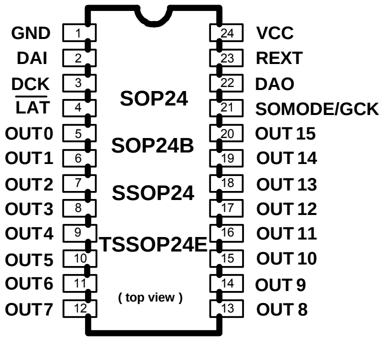
Package Types

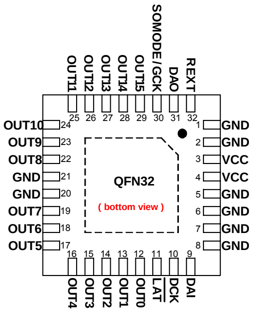
- SOP24, SOP24B, SSOP24, TSSOP24E (with exposed pad), QFN32 (with exposed pad)

Block Diagram


OUT 0
OUT 1
OUT 15
VCC
GND
LED Open Detector (0)
LED Open Detector (1)
LED Open Detector (15)
Internal Oscillator
Constant Current Driver (0)
Constant Current Driver (1)
Constant Current Driver (15)
REXT
16-bit Counter
16-bit PWM Generator (0)
16-bit PWM Generator (1)
16-bit PWM Generator (15)
SOMODE /GCK
16
LAT
16-bit Latch Register (0)
16-bit Latch Register (1)
16-bit Latch Register (15)
16
DAI
16-bit Shift Register (0)
16-bit Shift Register (1)
16-bit Shift Register (15)
DAO
DCK

Pin Connection


GND 1
DAI 2
DCK 3
$\overline{\text{LAT}}$ 4
OUT0 5
OUT1 6
OUT2 7
OUT3 8
OUT4 9
OUT5 10
OUT6 11
OUT7 12
24 VCC
23 REXT
22 DAO
21 SOMODE/GCK
20 OUT 15
19 OUT 14
18 OUT 13
17 OUT 12
16 OUT 11
15 OUT 10
14 OUT 9
13 OUT 8
SOP24
SOP24B
SSOP24
TSSOP24E
(top view)

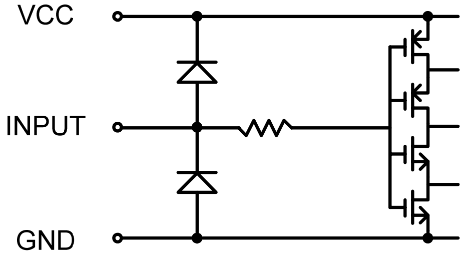

OUT11 25
OUT12 26
OUT13 27
OUT14 28
OUT15 29
SOMODE / GCK 30
DAO 31
REXT 32
1 GND
2 GND
3 VCC
4 VCC
5 GND
6 GND
7 GND
8 GND
9 DAI
10 DCK
11 $\overline{\text{LAT}}$
12 OUT0
13 OUT1
14 OUT2
15 OUT3
16 OUT4
17 OUT5
18 OUT6
19 OUT7
20 GND
21 GND
22 OUT8
23 OUT9
24 OUT10
QFN32
(bottom view)

Pin Description

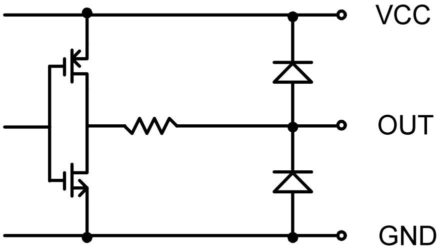
PIN No.	PIN NAME	FUNCTION
SOP24/SOP24B/SSOP24/TSSOP24E: 1 TSSOP24E, QFN32: exposed pad QFN32: 1, 2, 5, 6, 7, 8, 20,21	GND	Ground terminal.
SOP24/SOP24B/SSOP24/TSSOP24E: 2 QFN32: 9	DAI	Serial data input terminal.
SOP24/SOP24B/SSOP24/TSSOP24E: 3 QFN32: 10	DCK	Synchronous clock input terminal for serial data transfer. Data is sampled at the rising edge of DCK.
SOP24/SOP24B/SSOP24/TSSOP24E: 4 QFN32: 11	$\overline{\text{LAT}}$	Input terminal of data strobe: ‘**H**’ means data on shift register goes through latch (level trigger), ‘**L**’ means data is latched.
SOP24/SOP24B/SSOP24/TSSOP24E: 5~20 QFN32: 12~19, 22~29	OUT0~15	Sink constant-current outputs (open-drain).
SOP24/SOP24B/SSOP24/TSSOP24E: 21 QFN32: 30	SOMODE /GCK	Serial Out Mode Selection(SOMODE) : **‘H’**: DAO is shifted out and synchronized to falling edge of DCK, **‘L’** : DAO is shifted out and synchronized to rising edge of DCK. Gray Scale Clock(GCK) : Input terminal for PWM operation.
SOP24/SOP24B/SSOP24/TSSOP24E: 22 QFN32: 31	DAO	Serial data output terminal.
SOP24/SOP24B/SSOP24/TSSOP24E: 23 QFN32: 32	REXT	External resistors connected between REXT and GND for output current value setting.
SOP24/SOP24B/SSOP24/TSSOP24E: 24 QFN32: 3, 4	VCC	Supply voltage terminal.

Equivalent Circuit of Inputs and Outputs

1. DCK, DAI, $\overline{\text{LAT}}$, SOMODE/GCK terminals



2. DAO terminals



PCB Layout Consideration

To connect an external resistor to REXT pin and ground can determine the maximum output current. If there is any disturbance occurred to REXT pin, the constant current output may be unstable or noisy. Since REXT (pin23), DAO (pin22), and SOMODE/GCK (pin21) are next to each other, the most possible interference is caused by DAO or SOMODE/GCK signal. Accordingly, it is recommended that adding some shielding area within the above pins in PCB layout, or laying the signal line of above pins on different PCB layer will prevent the noise problems effectively.

Maximum Ratings (Ta=25°C, Tj(max) = 150°C)

CHARACTERISTIC	SYMBOL	RATING	UNIT
Supply Voltage	VCC	-0.3 ~ 7.0	V
Input Voltage	VIN	-0.3 ~ VCC+0.3	V
Output Current	IOUT	100	mA
Output Voltage	VOUT	-0.3 ~ 17	V
Input Clock Frequency	FDCK	25	MHz
GND Terminal Current	IGND	1600	mA
Power Dissipation (4 layer PCB, at Ta=25℃)	PD	4.46 (QFN32)	W
		4.17 (TSSOP24E exposed pad)	
		2.45 (SOP24)	
		2.19 (SOP24B)	
		1.79 (SSOP24)	
Thermal Resistance (4 layer PCB, at Ta=25℃)	Rth(j-a)	28 (QFN32)	°C/W
		30 (TSSOP24E exposed pad)	
		51 (SOP24)	
		57 (SOP24B)	
		70 (SSOP24)	
Operating Temperature	Top	-40 ~ 85	°C
Storage Temperature	Tstg	-55 ~ 150	°C

Recommended Operating Condition

CHARACTERISTIC	SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT
Supply Voltage	VCC	—	3.3	5.0	5.5	V
Output Voltage	VOUT	Driver On[*1]	1.0	—	0.5VCC	V
Output Voltage	VOUT	Driver Off[*2]	—	—	17	
Output Current	IO	OUTn	5	—	90	mA
	IOH	VOH = VCC – 0.4 V	-0.8	—	-2	
	IOL	VOL = 0.2 V	+0.8	—	+2	
Input Voltage	VIH	VCC = 3.3 V ~ 5.5V	0.8VCC	—	VCC	V
	VIL		0.0	—	0.2VCC	
Input Clock Frequency	FDCK	Single Chip Operation	—	—	25	MHz
Input PWM Frequency	FGCK	3.3V~5.5V	—	—	25	
$\overline{\text{LAT}}$ Pulse Width	Tw $\overline{\text{LAT}}$	VCC = 5.0V	15	—	—	ns
DCK Pulse Width	Tw DCK		15	—	—	
Set-up Time for DAI	tsetup(D)		10	—	—	
Hold Time for DAI	thold(D)		10	—	—	
Set-up Time for $\overline{\text{LAT}}$	tsetup(L)		10	—	—	
Hold Time for $\overline{\text{LAT}}$	thold(L)		10	—	—	
Internal Oscillator Frequency	FOSC		14.4	18	21.6	MHz

[*1] Notice that the power dissipation is limited to its package and ambient temperature.
[*2] The driver output voltage including any overshoot stress has to be compliant with the maximum voltage (17V).

Electrical Characteristics (VCC = 5.0 V, Ta = 25°C unless otherwise noted)

CHARACTERISTIC	SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT
Input Voltage "H" Level	VIH	CMOS logic level	0.8VCC	—	VCC	V
Input Voltage "L" Level	VIL	CMOS logic level	GND	—	0.2VCC	
Output Leakage Current	IOL	VOH = 17 V	—	—	±1.0	uA
Output Voltage (S-OUT)	VOL	IOL = 1.25 mA	—	—	0.2	V
	VOH	IOH= 1.2 mA	VCC-0.4	—	—	
Output Current Skew (Channel-to-Channel)[*1]	IOL1	VOUT = 1.0 V Rrext = 2.2 KΩ	—	—	±3	%
Output Current Skew (Chip-to-Chip)[*2]	IOL2		25.79	—	29.08	mA
Output Voltage Regulation	% / VOUT	Rrext = 2.2 KΩ VOUT = 1 V ~ 3 V	—	±0.1	±0.5	% / V
Supply Voltage Regulation	% / VCC	Rrext = 2.2 KΩ	—	±1	±4	
LED Open Detection Threshold	V(od)	all outputs turn on	—	0.3	—	V
Supply Current[*3]	$I_{DD(off)}$	power on all pins are open unless VCC and GND (fee-running mode)	—	5.39	6.5	mA
	$I_{DD(off)}$	power on all pins are open unless VCC and GND (external GCK mode)	—	4.57	—	
	$I_{DD(on)}$	input signal is static Rrext = 12.4 KΩ all outputs turn off	—	5.91	—	
	$I_{DD(on)}$	input signal is static Rrext = 2.2 KΩ all outputs turn off	—	8.10	—	
	$I_{DD(on)}$	input signal is static Rrext = 560 Ω all outputs turn off	—	17.11	—	

[*1] Channel-to-channel skew is defined as the ratio between (any Iout – average Iout) and average Iout, where average Iout = (Imax + Imin) / 2.

[*2] Chip-to-Chip skew is defined as the range into which any output current of any IC falls.

[*3] IO excluded.

Electrical Characteristics (VCC = 3.3 V, Ta = 25°C unless otherwise noted)

CHARACTERISTIC	SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT
Input Voltage “H” Level	VIH	CMOS logic level	0.8VCC	—	VCC	V
Input Voltage “L” Level	VIL	CMOS logic level	GND	—	0.2VCC	
Output Leakage Current	IOL	VOH = 17 V	—	—	±1.0	uA
Output Voltage (S-OUT)	VOL	IOL = 1.25 mA	—	—	0.2	V
	VOH	IOH= 1.2 mA	VCC-0.4	—	—	
Output Current Skew (Channel-to-Channel)[*1]	IOL1	VOUT = 1.0 V Rrext = 2.2 KΩ	—	—	±3	%
Output Current Skew (Chip-to-Chip)[*2]	IOL2		25.79	—	29.08	mA
Output Voltage Regulation	% / VOUT	Rrext = 2.2 KΩ VOUT = 1 V ~ 3 V	—	±0.1	±0.5	% / V
Supply Voltage Regulation	% / VCC	Rrext = 2.2 KΩ	—	±1	±4	
LED Open Detection Threshold	V(od)	all outputs turn on	—	0.3	—	V
Supply Current[*3]	$I_{DD(off)}$	power on all pins are open unless VCC and GND (fee-running mode)	—	3.8	—	mA
	$I_{DD(off)}$	power on all pins are open unless VCC and GND (external GCK mode)	—	3.39	—	
	$I_{DD(on)}$	input signal is static Rrext = 12.4 KΩ all outputs turn off	—	4.33	—	
	$I_{DD(on)}$	input signal is static Rrext = 2.2 KΩ all outputs turn off	—	6.54	—	
	$I_{DD(on)}$	input signal is static Rrext = 560 Ω all outputs turn off	—	15.10	—	

[*1] Channel-to-channel skew is defined as the ratio between (any Iout – average Iout) and average Iout, where average Iout = (Imax + Imin) / 2.

[*2] Chip-to-Chip skew is defined as the range into which any output current of any IC falls.

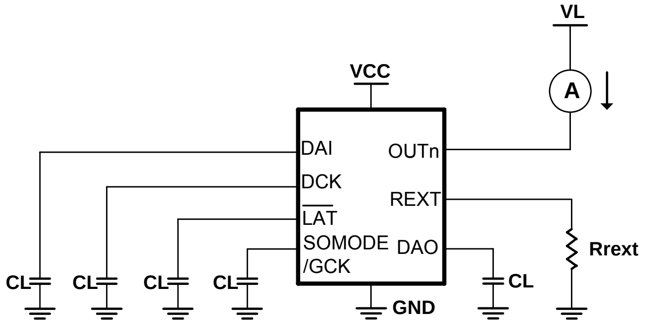
[*3] IO excluded.

Switching Characteristics (VCC = 5.0V, Ta = 25°C unless otherwise noted)

CHARACTERISTIC		SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT
Propagation Delay (‘L’ to ‘H’)	GCK-to-OUT	tpLH	VIH = VCC VIL = GND Rrext = 2.2 KΩ VL = 5.0 V CL = 13 pF	—	45.74	—	ns
	DCK-to-DAO			—	37.16	—	
Propagation Delay (‘H’ to ‘L’)	GCK-to-OUT	tpHL		—	23.76	—	
	DCK-to-DAO			—	27.82	—	
Output Current Rise Time		tor		—	18	—	
Output Current Fall Time		tof		—	6.96	—	
Output to output Delay Time Unit		td		—	33	—	
Output Current (Propagation Delay after $\overline{LAT}$ trigger)		top[*1]		—	—	4.6	ms

Switching Characteristics (VCC = 3.3V, Ta = 25°C unless otherwise noted)

CHARACTERISTIC		SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT
Propagation Delay (‘L’ to ‘H’)	GCK-to-OUT	tpLH	VIH = VCC VIL = GND Rrext = 2.2 KΩ VL = 3.3 V CL = 13 pF	—	48.8	—	ns
	DCK-to-DAO			—	21.2	—	
Propagation Delay (‘H’ to ‘L’)	GCK-to-OUT	tpHL		—	29.6	—	
	DCK-to-DAO			—	17.6	—	
Output Current Rise Time		tor		—	20	—	
Output Current Fall Time		tof		—	8.25	—	
Output to output Delay Time Unit		td		—	34	—	
Output Current (Propagation Delay after $\overline{LAT}$ trigger)		top[*1]		—	—	4.6	ms



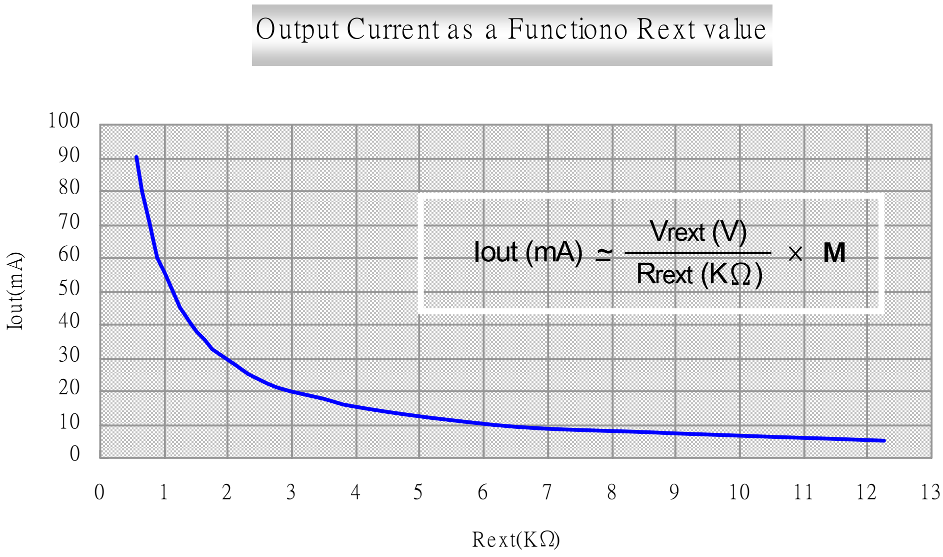
Switching Characteristics Test Circuit

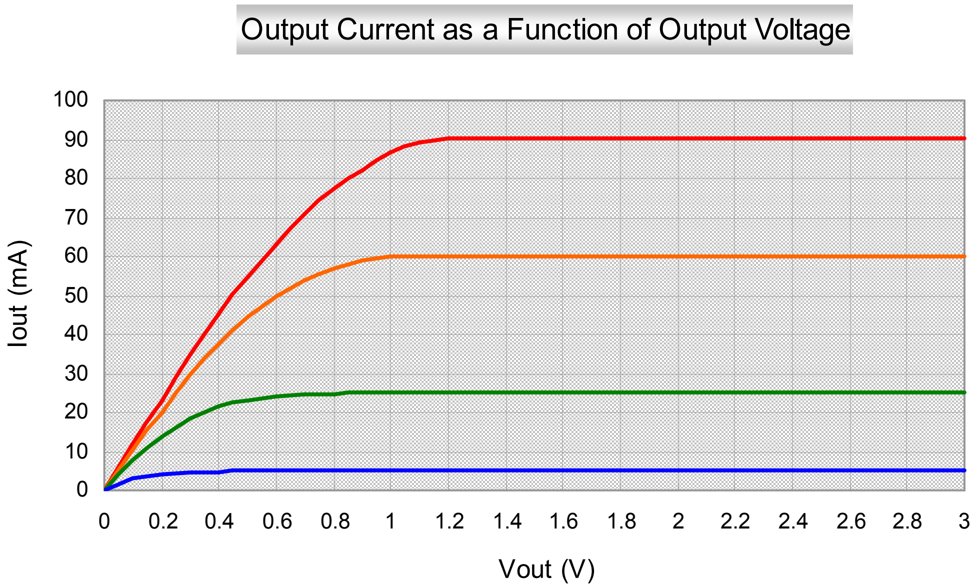
[*1] Reload the new PWM data at the end of the last PWM frame.

Constant-Current Output

Constant-current value (Iout[*1])of each output channel is set by an external resistor connected between the REXT pin and GND. The current scale ranging can be adjusted from 5mA to 90mA by varying the resistor value. The reference voltage of REXT terminal (Vrext) is approximately 1.23V. The output current value is calculated by the following equation:

Iout(mA)	5	10	20	30	40	50	60	70	80	90
M	50.86	48.60	48.39	47.66	46.97	46.13	44.74	43.94	43.20	42.24





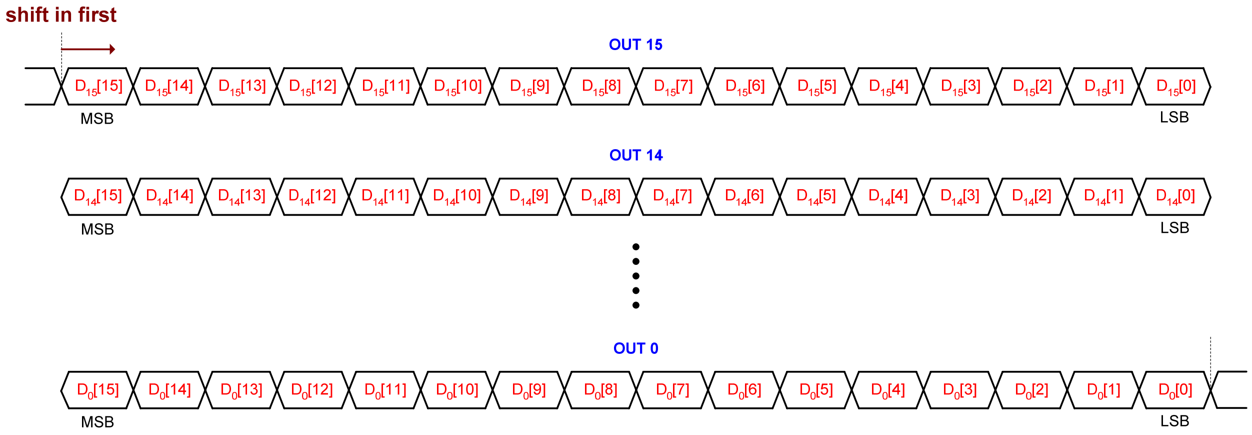
In order to obtain a good performance of constant-current output, a suitable output voltage is necessary. Users can get related information about the minimum output voltage above.

[*1] Iout is typical current value setting under 100% PWM duty cycle.

Serial Data Interface

The serial-in data (DAI) will be clocked into 16 × 16 bit shift registers synchronized on the rising edge of the clock (DCK). The data will be transferred into the 16 × 16 bit latch registers when the strobe signal ($\overline{LAT}$) is kept at high level (level trigger); otherwise, the data will be held. The latch pulse should be sent after the falling edge of the last clock within a frame data. The trigger timing of the serial-out data (DAO) will be shifted out on synchronization to the rising edge of the clock if serial out selection (SOMODE) is kept at low level. And if serial out selection (SOMODE) is kept at high level, the serial-out data (DAO) will be shifted out on synchronization to the falling edge of the clock (DCK).

Input Data Format

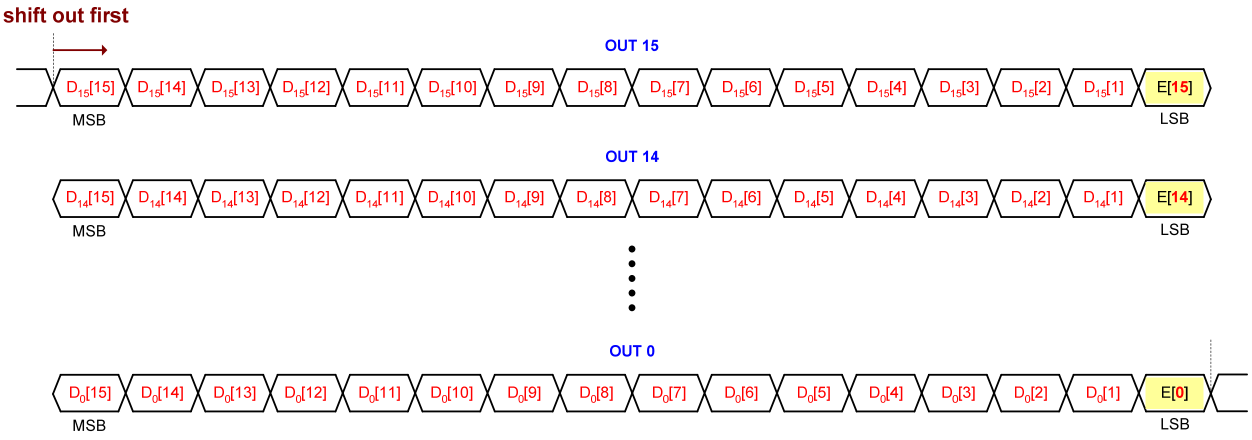

shift in first
OUT 15
D15[15] D15[14] D15[13] D15[12] D15[11] D15[10] D15[9] D15[8] D15[7] D15[6] D15[5] D15[4] D15[3] D15[2] D15[1] D15[0]
MSB
LSB
OUT 14
D14[15] D14[14] D14[13] D14[12] D14[11] D14[10] D14[9] D14[8] D14[7] D14[6] D14[5] D14[4] D14[3] D14[2] D14[1] D14[0]
MSB
LSB
OUT 0
D0[15] D0[14] D0[13] D0[12] D0[11] D0[10] D0[9] D0[8] D0[7] D0[6] D0[5] D0[4] D0[3] D0[2] D0[1] D0[0]
MSB
LSB

$$\text{Active width per frame(\%)} = \frac{D[15]\times2^{15}+D[14]\times2^{14}+D[13]\times2^{13}+D[12]\times2^{12}+D[11]\times2^{11}+D[10]\times2^{10}+D[9]\times2^{9}+D[8]\times2^{8}+D[7]\times2^{7}+D[6]\times2^{6}+D[5]\times2^{5}+D[4]\times2^{4}+D[3]\times2^{3}+D[2]\times2^{2}+D[1]\times2^{1}+D[0]\times2^{0}}{65536}$$

LED Open Detection

DM632 provides a real time monitor of LED open detection function without extra components or circuit design. It will be identified as a LED open failure when the output is turned on but the output voltage is below 0.3V. The test result of each channel will write to its correspondent shift register which is in LSB position ($D_{15}[0]$, $D_{14}[0]$, …., $D_0[0]$) while strobe signal is active. User can refer to timing diagram on page13. Detecting report could be retrieved from serial-out (DAO) data. If the system reads ‘1’ back, that indicates LED is in normal status. But if ‘0’ was retrieved then LED open failure has occurred. In order to make sure LED open detection function is in well operating condition, it is recommended that all the luminance data are wrote to ‘1’ then almost turning on the outputs during detection process.

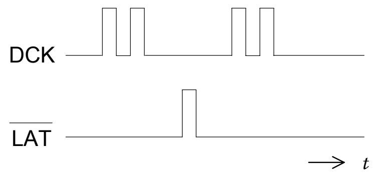
Serial-out Data Format


shift out first
OUT 15
D15[15] D15[14] D15[13] D15[12] D15[11] D15[10] D15[9] D15[8] D15[7] D15[6] D15[5] D15[4] D15[3] D15[2] D15[1] E[15]
MSB
LSB
OUT 14
D14[15] D14[14] D14[13] D14[12] D14[11] D14[10] D14[9] D14[8] D14[7] D14[6] D14[5] D14[4] D14[3] D14[2] D14[1] E[14]
MSB
LSB
OUT 0
D0[15] D0[14] D0[13] D0[12] D0[11] D0[10] D0[9] D0[8] D0[7] D0[6] D0[5] D0[4] D0[3] D0[2] D0[1] E[0]
MSB
LSB

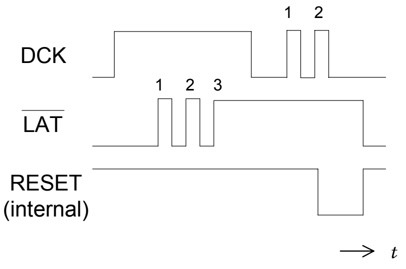
∗E[15], E[14], … , E[0] are Error Message of LED Open Detection. ‘1’ is normal, and ‘0’ is abnormal.

Selection of Internal/External PWM Frequency

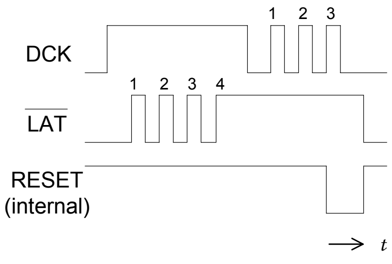
The default operation mode is the **free-running** PWM signal generated by internal oscillator after power-on. Users could switch internal to external PWM frequency source by following timing sequence. There are two alternative options could be selected. The option 1 shows three rising edge of latch pulses ($\overline{\text{LAT}}$) when the clock (DCK) kept at high level then two rising edge of clock (DCK) pulses when the latch pulse ($\overline{\text{LAT}}$) kept at high level. Then the SOMODE/GCK pin could input external frequency to operate PWM function. The option 2 shows four rising edge of latch pulses($\overline{\text{LAT}}$) when clock(DCK) kept at high level then sending three rising edge of clock (DCK) signal, while latch($\overline{\text{LAT}}$) signal kept high level at the same time. Meanwhile the GCK external mode can be set back to the free-running mode. Notice that when internal RESET at low level, all the shift registers in DM632 will be cleared (Kept at Low level) and all output current will be off immediately.



Normal Operation


1 2
DCK
1 2 3
LAT
RESET
(internal)
t

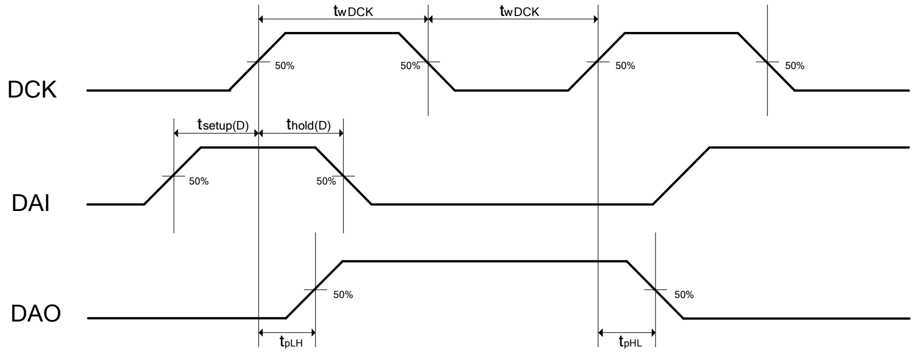
Option 1 : Timing Combination to set up
external GCK mode


1 2 3
DCK
1 2 3 4
LAT
RESET
(internal)
t

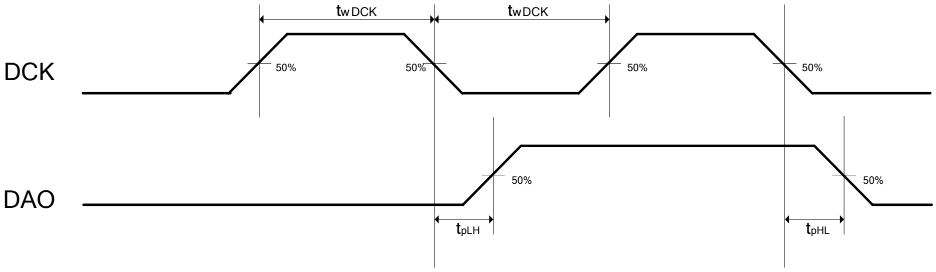
Option 2 : Timing Combination to set up
free-running mode

Timing Diagram

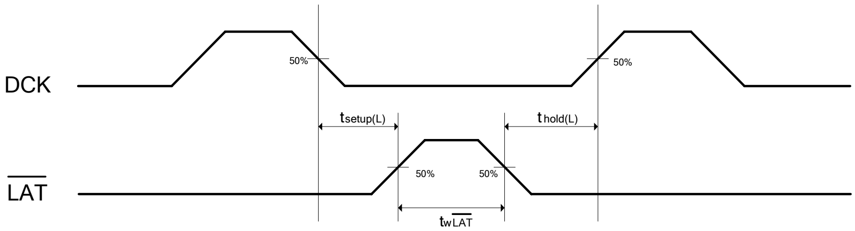
1. DCK-DAI, DAO (SOMODE = ”L” at free-running mode, or external GCK mode)


twDCK
twDCK
DCK
50%
50%
50%
50%
tsetup(D)
thold(D)
DAI
50%
50%
DAO
50%
50%
tpLH
tpHL

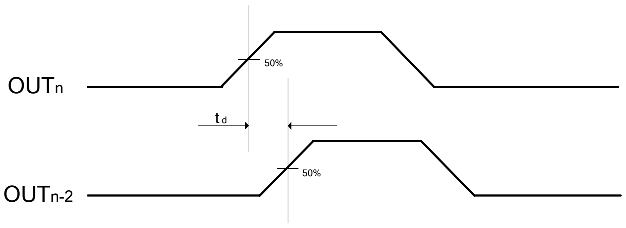
2. DCK, DAO (SOMODE = “H” at free-running mode)


twDCK
twDCK
DCK
50%
50%
50%
50%
DAO
50%
50%
tpLH
tpHL

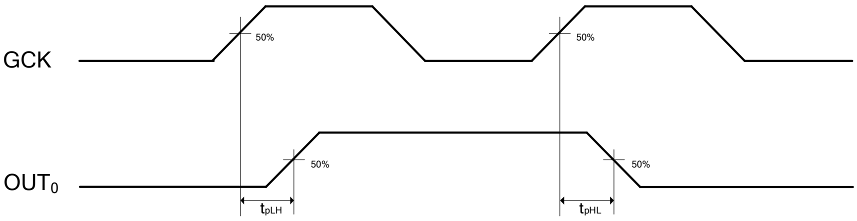
3. DCK-$\overline{\text{LAT}}$


DCK
50%
50%
tsetup(L)
thold(L)
LAT
50%
50%
twLAT

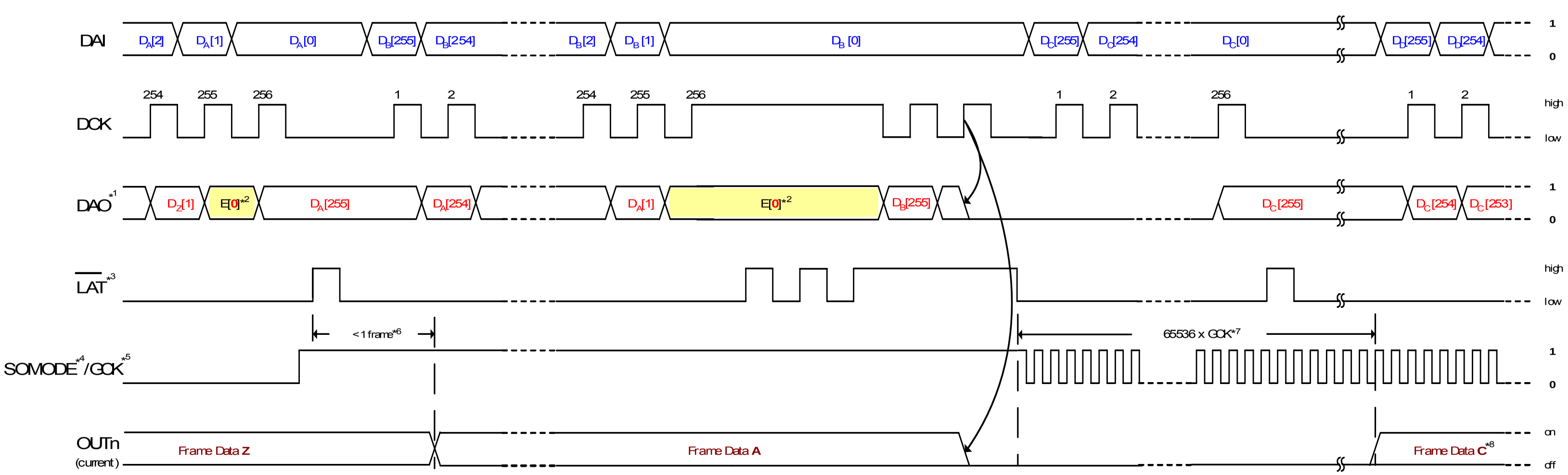
4. Output to Output Delay Time Unit (n=2,3,4,5,6,7, 10, 11, 12, 13, 14, 15)


OUTn
50%
td
OUTn-2
50%

5. GCK-OUT$_0$


GCK
50%
50%
OUT0
50%
50%
tpLH
tpHL

Timing Diagram (free-running mode switch to external GCK mode)


DAI
DA[2]
DA[1]
DA[0]
DB[255]
DB[254]
DB[2]
DB[1]
DB[0]
DC[255]
DC[254]
DC[0]
DD[255]
DD[254]
1
0
DCK
254
255
256
1
2
254
255
256
1
2
256
1
2
high
low
DAO*1
DZ[1]
E[0]*2
DA[255]
DA[254]
DA[1]
E[0]*2
DB[255]
DC[255]
DC[254]
DC[253]
1
0
LAT*3
high
low
SOMODE*4/GCK*5
< 1 frame*6
65536 x GCK*7
1
0
OUTn
(current)
Frame Data Z
Frame Data A
Frame Data C*8
on
off

*1 DAO is shifted out on synchronization to rising / falling edge of DCK according to SOMODE is ‘**L**’ / ‘**H**’ .

*2 E[0] is the error message of LED open detection.

*3 $\overline{\text{LAT}}$ is level trigger, not edge trigger.

*4 SOMODE function work in free-running mode.

*5 While switching to external GCK mode, all registers in DM632 will be reset simultaneously.

*6 Starting the new PWM frame after the last PWM period finish completely.

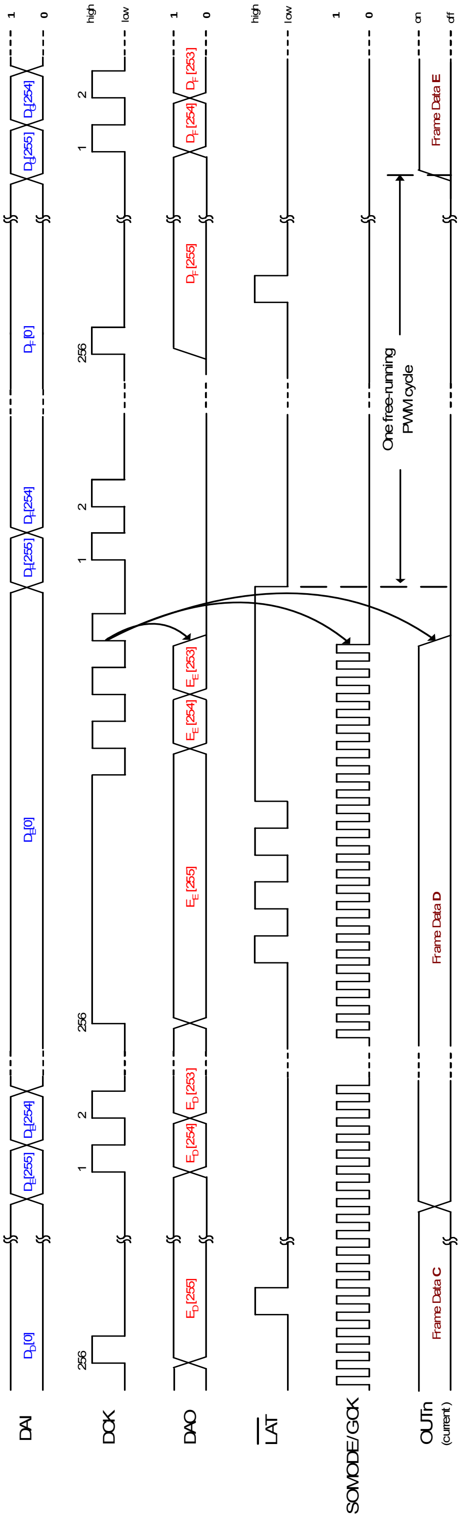
*7 While switching to external GCK mode, outputs will be active after 65536 GCK pulse.

*8 When using external frequency for PWM operation, the PWM refresh rate (frame rate) can be calculated by following equation:

$$\boxed{\text{Refresh Rate (Hz)} = \frac{\text{Input GCK Frequency (Hz)}}{\text{Total PWM resolution } (2^{16})}}$$

For example, if the refresh rate in display system is higher than 60Hz, the input GCK frequency must be higher than 4MHz.

Timing Diagram (external GCK mode switch to free-running mode)


DAI
DCK
DAO
LAT
SOMODE/GCK
OUTn
(current)
1
0
high
low
on
off
D_D[0]
D_E[255]
D_E[254]
D_E[0]
D_F[255]
D_F[254]
D_F[0]
D_G[255]
D_G[254]
E_D[255]
E_D[254]
E_D[253]
E_E[255]
E_E[254]
E_E[253]
D_F[255]
D_F[254]
D_F[253]
256
1
2
Frame Data C
Frame Data D
Frame Data E
One free-running PWM cycle

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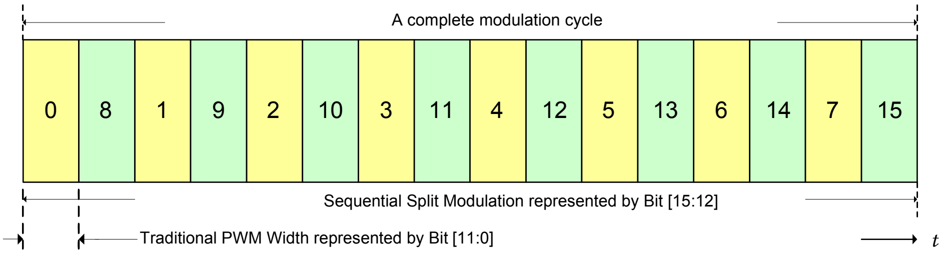
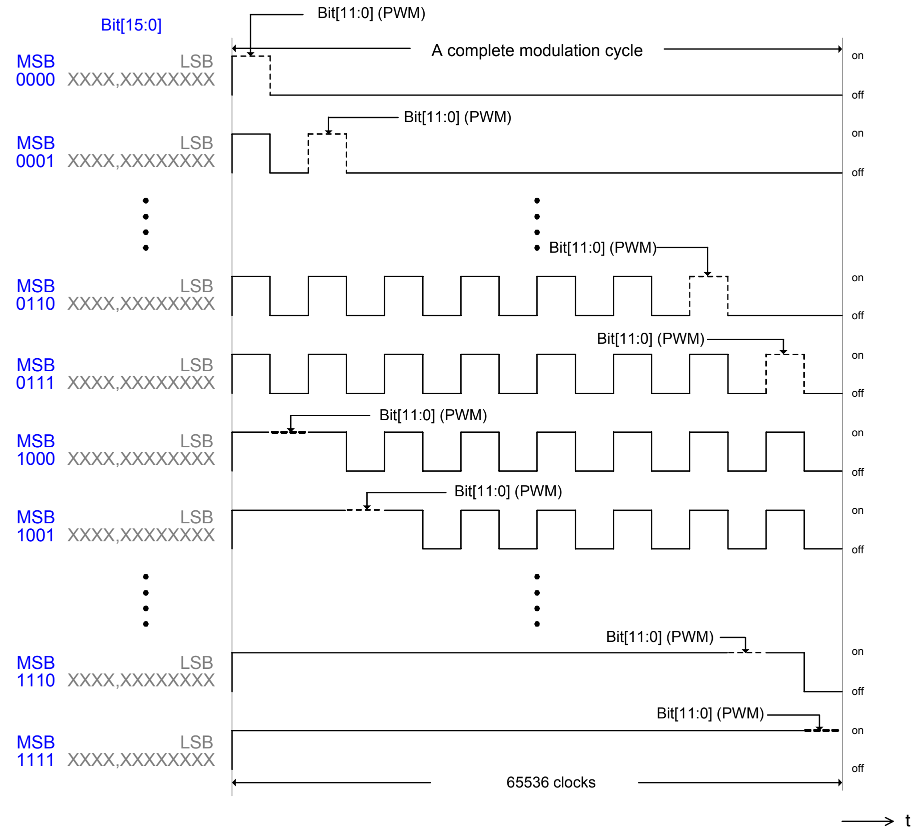
Output Modulation Technique

DM632 provides a new LED drive technique of output modulation. It mixes traditional Pulse Width Modulation (PWM) represented by LSB 12 bit with Sequential Split Modulation (SSM) represented by MSB 4 bit. The main benefits of SSM are to drive LED with an equivalent higher refresh rate (up to 380Hzn in DM632 when F_{GCK} = 25MHz) and change bit to next bit smoothly. The relationships between PWM and SSM in time domain can be refer to the diagram (not to scale) below:


A complete modulation cycle
0
8
1
9
2
10
3
11
4
12
5
13
6
14
7
15
Sequential Split Modulation represented by Bit [15:12]
Traditional PWM Width represented by Bit [11:0]
t

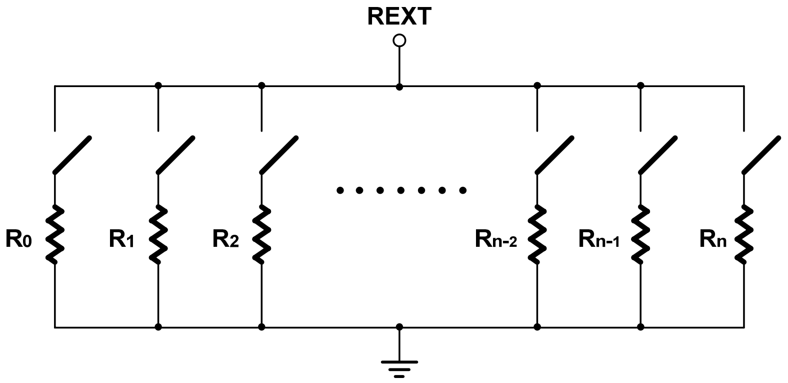

Bit[15:0]
Bit[11:0] (PWM)
A complete modulation cycle
MSB LSB
0000 XXXX,XXXXXXXX
MSB LSB
0001 XXXX,XXXXXXXX
MSB LSB
0110 XXXX,XXXXXXXX
MSB LSB
0111 XXXX,XXXXXXXX
MSB LSB
1000 XXXX,XXXXXXXX
MSB LSB
1001 XXXX,XXXXXXXX
MSB LSB
1110 XXXX,XXXXXXXX
MSB LSB
1111 XXXX,XXXXXXXX
on
off
65536 clocks
t

Ultra High Resolution Current Outputs

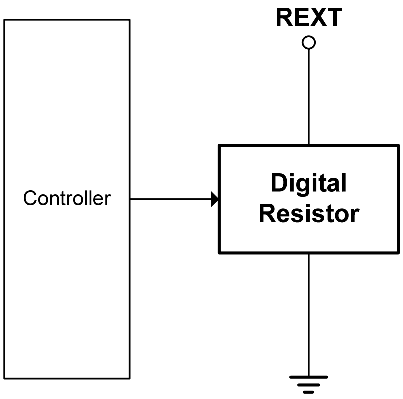
DM632 could provide 16-bit linear PWM control current outputs for each channel. There are two advantages for system design. One is DM632 has sufficient bit resolution (65536 steps), not only LED color information but additional data such as global brightness, dot correction, and gamma correction can be represented by the proper algorithms. The other is to reduce a lot of clock and data rate compared to conventional ON-OFF type LED drivers.

Global Brightness Control

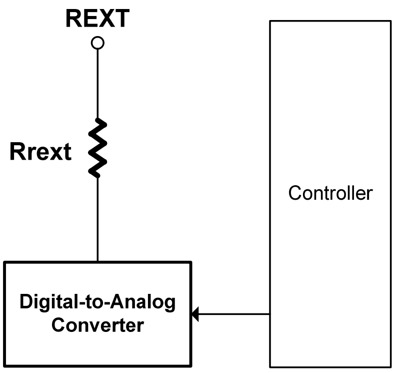
DM632 has no built-in global brightness control feature. In order to obtain a lower resolution of global brightness control effect, two methods could be utilized. Here show different ways to adjust the Rrext value or voltage drop across the external resistor. Please see the reference circuit below:



Global Brightness Control with Resistor Ladder



Global Brightness Control
with Digital Resistor



Global Brightness Control
with D/A converter

Output to Output Delay

DM632 has build-in output to output delay with a special arrangement. This arrangement help chip avoid noise cause by large current during channels switching. The arrangement details are shown as following table.

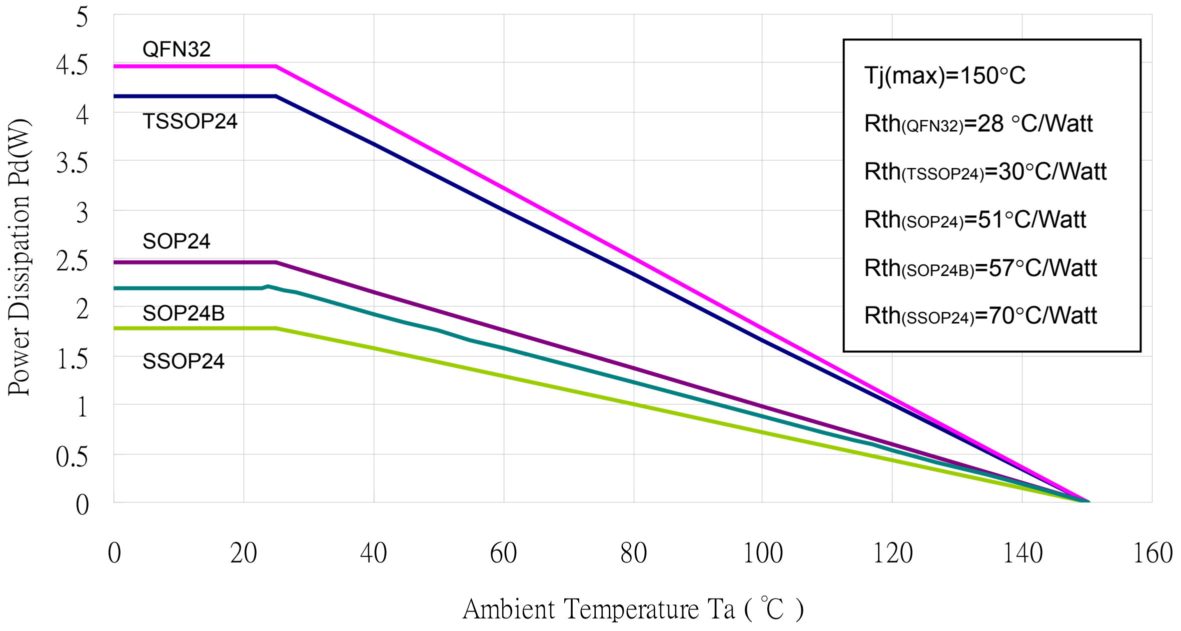
Channel	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
Delay units	0	4	1	5	2	6	3	7	3	7	2	6	1	5	0	4

Power Dissipation

The power dissipation of a semiconductor chip is limited to its package and ambient temperature, in which the device requires the maximum output current calculated for given operating conditions. The maximum allowable power consumption can be calculated by the following equation:

$$Pd(max)(Watt) = \frac{\text{Tj(junction temperature)(max)(℃)} - \text{Ta(ambient temperature)(℃)}}{\text{Rth(junction-to-air thermal resistance)(℃/Watt)}}$$

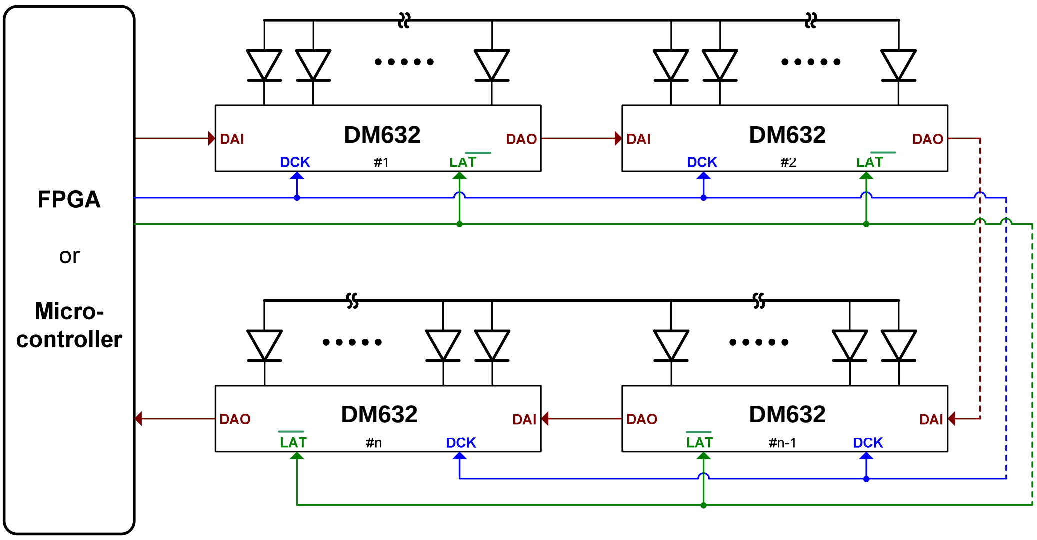
The relationship between power dissipation and operating temperature can be refer to the figure below:



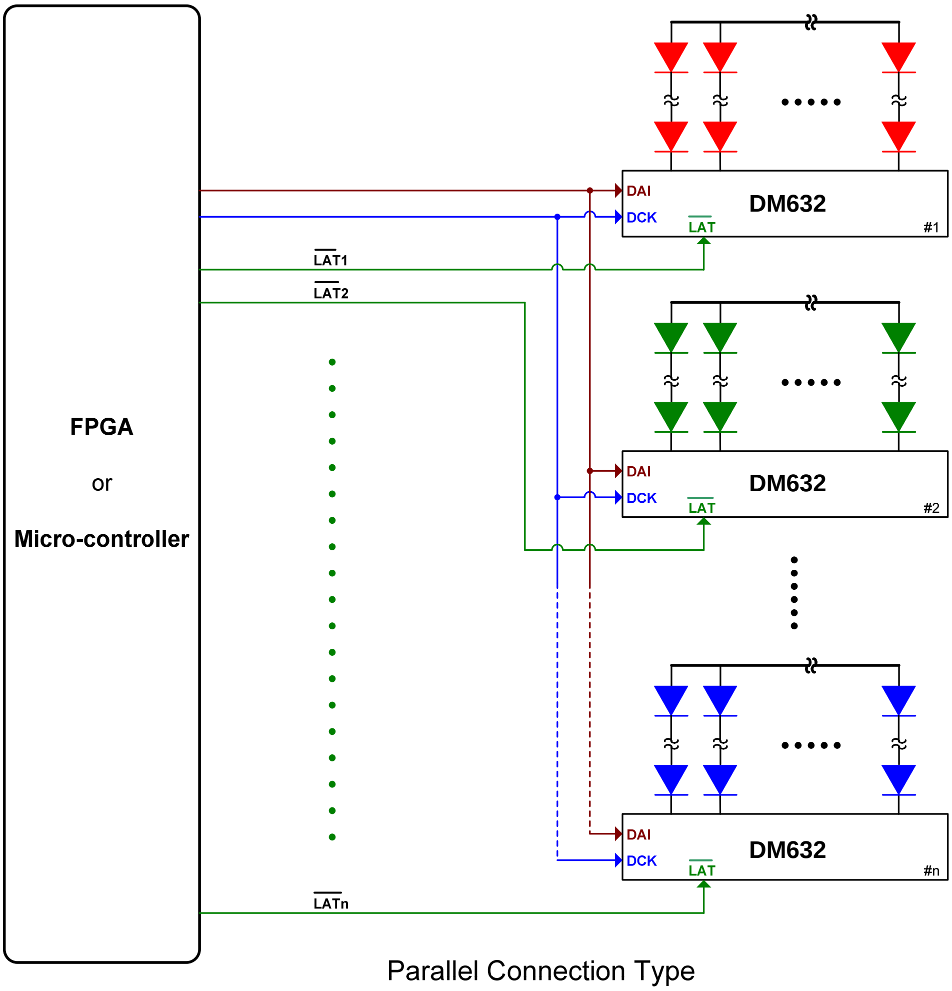
The power consumption of IC can be determined by the following equation and should be less than the maximum allowable power dissipation:

$$Pd(W) = V_{CC}(V) \times I_{DD}(A) + Vout0 \times Iout0 \times Duty0 + \cdots\cdots + Vout15 \times Iout15 \times Duty15 \leq Pd(max)(W)$$

Typical Application


FPGA
or
Micro-
controller
DAI
DM632
DAO
DCK
#1
LAT
DAI
DM632
DAO
DCK
#2
LAT
DAO
DM632
DAI
LAT
#n
DCK
DAO
DM632
DAI
LAT
#n-1
DCK

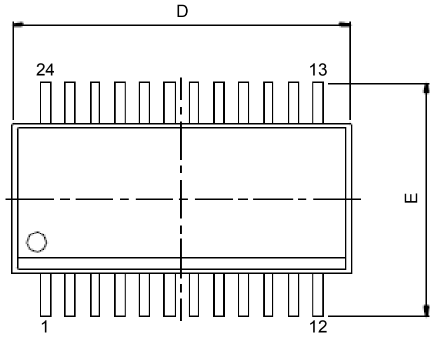
Serial Connection Type

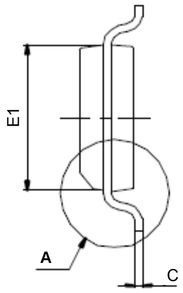

FPGA
or
Micro-controller
DAI
DCK
LAT
DM632
#1
LAT1
LAT2
DAI
DCK
LAT
DM632
#2
DAI
DCK
LAT
DM632
#n
LATn

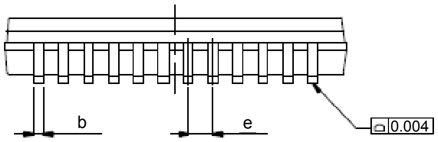
Parallel Connection Type

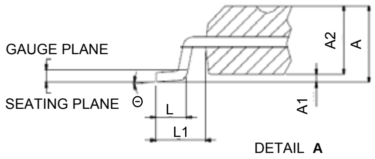
Package Outline Dimension

DM632-SSOP





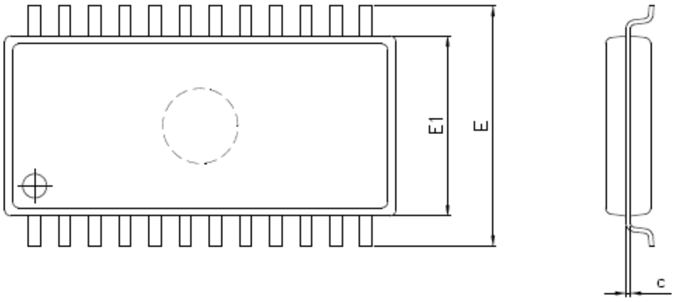


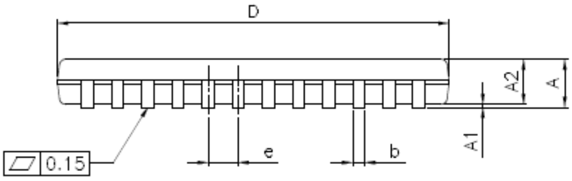

GAUGE PLANE
SEATING PLANE
Θ
L
L1
A2
A
A1
DETAIL A

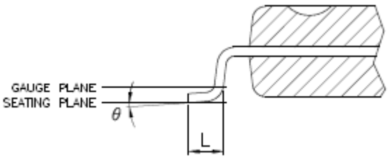
	DIMENSIONS IN INCH		DIMENSIONS IN MM	
SYMBOLS	MIN.	MAX.	MIN.	MAX.
A	0.053	0.069	1.346	1.753
A1	0.004	0.010	0.102	0.254
A2	-	0.059	-	1.499
b	0.008	0.012	0.203	0.305
C	0.007	0.010	0.178	0.254
D	0.337	0.344	8.560	8.738
E	0.228	0.244	5.791	6.198
E1	0.150	0.157	3.810	3.988
e	0.025 BSC.		0.635 BSC	
L	0.016	0.050	0.406	1.270
L1	0.041 BSC		1.041 BSC	
Θ	0°	8°	0°	8°

Package Outline Dimension

DM632-SOPB



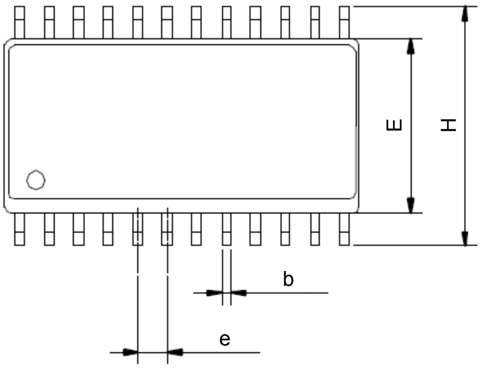


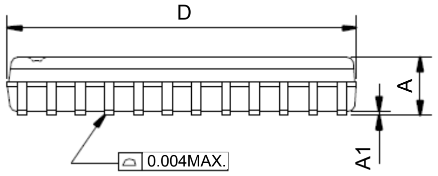


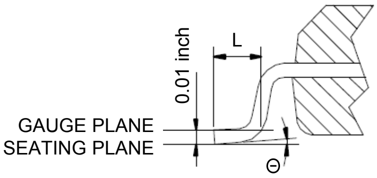
	DIMENSIONS IN INCH		DIMENSIONS IN MM	
SYMBOLS	MIN.	MAX.	MIN.	MAX.
A	-	0.075	-	1.900
A1	0.002	0.008	0.050	0.200
A2	0.051	0.067	1.300	1.700
b	0.012	0.020	0.300	0.500
c	0.004	0.010	0.100	0.250
D	0.504	0.520	12.800	13.200
E	0.303	0.327	7.700	8.300
e	0.0394 BSC		1.000 BSC	
E1	0.228	0.244	5.800	6.200
L	0.010	0.026	0.250	0.650
θ	0°	10°	0°	10°

Package Outline Dimension

DM632-SOP



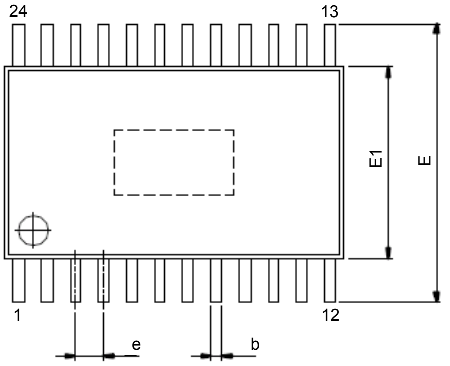

D
A
A1
0.004MAX.

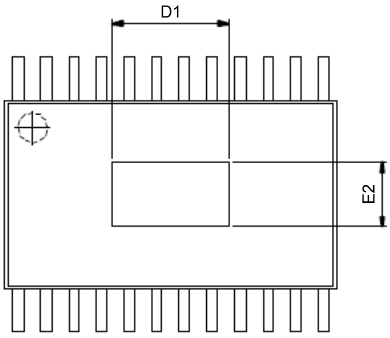

0.01 inch
L
GAUGE PLANE
SEATING PLANE
Θ

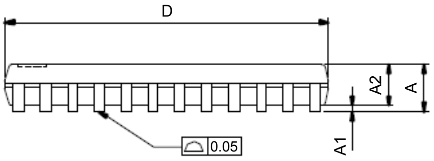
	DIMENSIONS IN INCH		DIMENSIONS IN MM	
SYMBOLS	MIN.	MAX.	MIN.	MAX.
A	-	0.104	-	2.642
A1	0.004	-	0.102	-
b	0.016 BSC		0.406 BSC	
D	0.612	0.624	15.545	15.850
E	0.292	0.299	7.417	7.595
e	0.050 BSC		1.270 BSC	
H	0.405	0.419	10.287	10.643
L	0.021	0.041	0.533	1.041
Θ	0°	8°	0°	8°

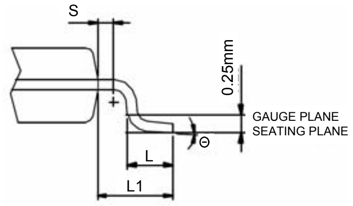
Package Outline Dimension

DM632-TSSOP (exposed pad)


24
13
E1
E
1
12
e
b



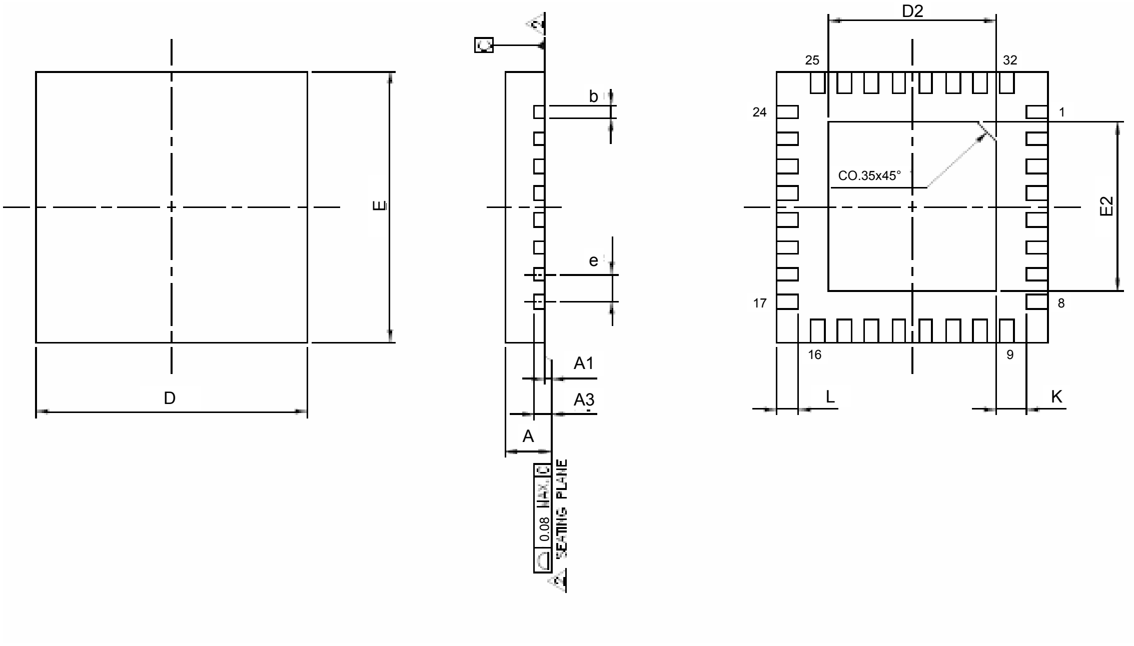



S
0.25mm
GAUGE PLANE
SEATING PLANE
L
Θ
L1

	DIMENSIONS IN INCH		DIMENSIONS IN MM	
SYMBOLS	MIN.	MAX.	MIN.	MAX.
A	-	0.047	-	1.20
A1	0.000	0.006	0.00	0.15
A2	0.031	0.041	0.80	1.05
b	0.007	0.012	0.19	0.30
D	0.303	0.311	7.70	7.90
E1	0.169	0.177	4.30	4.50
E	0.252 BSC		6.400 BSC	
e	0.026 BSC		0.650 BSC	
L1	0.039 REF		1.000 REF.	
L	0.018	0.030	0.45	0.75
S	0.008	-	0.20	-
Θ	0°	8°	0°	8°
E2	0.0898	0.1122	2.280	2.850
D1	0.146	1.819	3.700	4.620

Package Outline Dimension

DM632-QFN (exposed pad)



	DIMENSIONS IN INCH		DIMENSIONS IN MM	
SYMBOLS	MIN.	MAX.	MIN.	MAX.
A	0.028	0.031	0.70	0.80
A1	0	0.002	0	0.05
A3	0.008 REF.		0.203 REF.	
b	0.007	0.012	0.180	0.300
D	0.193	0.201	4.900	5.100
E	0.193	0.201	4.900	5.100
e	0.0197 BSC		0.500 BSC	
L	0.012	0.020	0.30	0.50
K	0.0079	-	0.2	-
D2	0.049	0.128	1.25	3.25
E2	0.049	0.128	1.25	3.25

Note: 1.DIMENSIONING AND TOLERANCING CONFORM TO ASME Y145.5M-1994.

2. REFER TO JEDEC STD. MO-220 WHHD-2 ISSUE A

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