

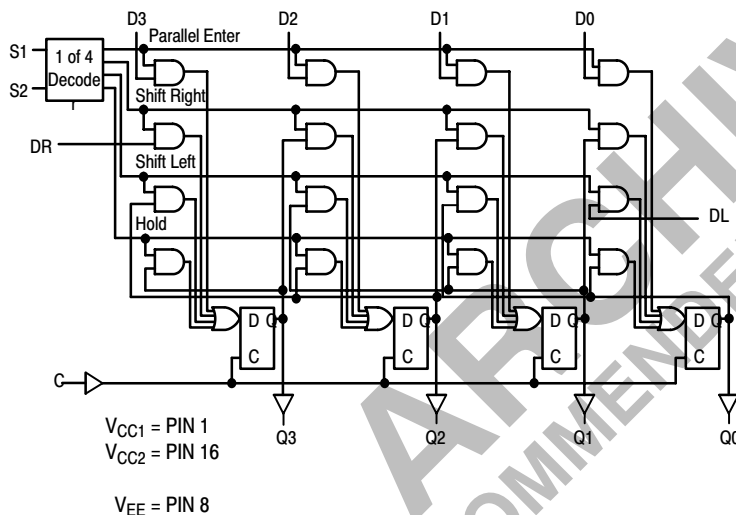
MC10141

Four Bit Universal Shift Register

The MC10141 is a four-bit universal shift register which performs shift left, or shift right, serial/parallel in, and serial/parallel out operations with no external gating. Inputs S1 and S2 control the four possible operations of the register without external gating of the clock. The flip-flops shift information on the positive edge of the clock. The four operations are stop shift, shift left, shift right, and parallel entry of data. The other six inputs are all data type inputs; four for parallel entry data, and one for shifting in from the left (DL) and one for shifting in from the right (DR).

- $P_D = 425 \text{ mW typ/pkg (No Load)}$
- $f_{\text{Shift}} = 200 \text{ MHz typ}$
- $t_r, t_f = 2.0 \text{ ns typ (20\%–80\%)}$

LOGIC DIAGRAM



TRUTH TABLE

SELECT		OPERATING MODE	OUTPUTS			
S1	S2		$Q0_{n+1}$	$Q1_{n+1}$	$Q2_{n+1}$	$Q3_{n+1}$
L	L	Parallel Entry	D0	D1	D2	D3
L	H	Shift Right*	$Q1_n$	$Q2_n$	$Q3_n$	DR
H	L	Shift Left*	DL	$Q0_n$	$Q1_n$	$Q2_n$
H	H	Stop Shift	$Q0_n$	$Q1_n$	$Q2_n$	$Q3_n$

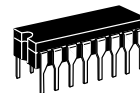
*Outputs as exist after pulse appears at "C" input with input conditions as shown. (Pulse = Positive transition of clock input).



ON Semiconductor

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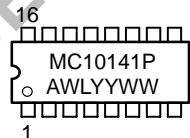
MARKING DIAGRAMS



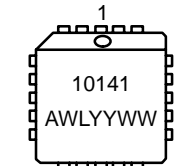
CDIP-16
L SUFFIX
CASE 620



PDIP-16
P SUFFIX
CASE 648

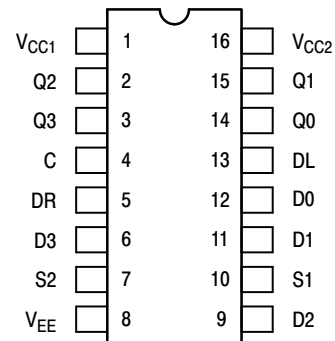


PLCC-20
FN SUFFIX
CASE 775



A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week

DIP PIN ASSIGNMENT



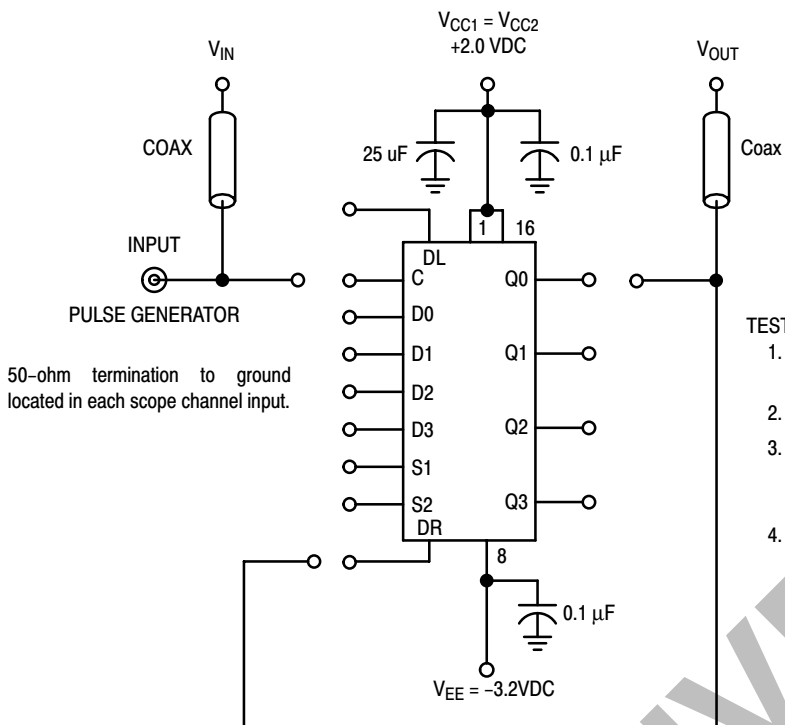
Pin assignment is for Dual-in-Line Package.
For PLCC pin assignment, see the Pin Conversion Tables on page 18 of the ON Semiconductor MECL Data Book (DL122/D).

ORDERING INFORMATION

Device	Package	Shipping
MC10141L	CDIP-16	25 Units / Rail
MC10141P	PDIP-16	25 Units / Rail
MC10141FN	PLCC-20	46 Units / Rail


MC10141

SHIFT FREQUENCY TEST CIRCUIT



All input and output cables to the scope are equal lengths of 50-ohm coaxial cable. Wire length should be < 1/4 inch from TP_{in} to input pin and TP_{out} to output pin.

TEST PROCEDURES:

1. SET D1, D2, D3 = +0.31 VDC (LOGIC L)
D0 = +1.11 VDC (LOGIC H)
2. APPLY CLOCK PULSE  TO SET Q0 HIGH.
3. MAINTAIN CLOCK LOW.
SET S1 = +0.31 VDC (LOGIC L)
S2 = +1.11 VDC (LOGIC H)
4. TEST SHIFT FREQUENCY

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	Pin Under Test	Test Limits							Unit
			−30°C		+25°C			+85°C		
			Min	Max	Min	Typ	Max	Min	Max	
Power Supply Drain Current	I _E	8		112		82	102		112	mAdc
Input Current	I _{inH}	5		350			220		220	μAdc
		6		350			220		220	
		7		390			245		245	
4			425			265		265		
	I _{inL}	12	0.5		0.5			0.3		μAdc
Output Voltage Logic 1	V _{OH}	3	−1.060	−0.890	−0.960		−0.810	−0.890	−0.700	Vdc
Output Voltage Logic 0	V _{OL}	3	−1.890	−1.675	−1.850		−1.650	−1.825	−1.615	Vdc
Threshold Voltage Logic 1	V _{OHA} (Note 1.)	3	−1.080		−0.980			−0.910		Vdc
		3	−1.080		−0.980			−0.910		
		3	−1.080		−0.980			−0.910		
		3	−1.080		−0.980			−0.910		
Threshold Voltage Logic 0	V _{OLA} (Note 1.)	3		−1.655			−1.630		−1.595	Vdc
		3		−1.655			−1.630		−1.595	
		3		−1.655			−1.630		−1.595	
		3		−1.655			−1.630		−1.595	
Switching Times (50Ω Load)										ns
Propagation Delay Setup Time (t _{setup})	t ₄₊₃₊	3	1.7	3.9	1.8	2.9	3.8	2.0	4.2	MHz
	t ₁₂₊₄₊	14	2.5		2.5			2.5		
	t ₁₀₊₄₊	14	5.5		5.0			5.5		
Hold Time (t _{hold})	t ₄₊₁₂₊	14	1.5		1.5			1.5		
Rise Time (20 to 80%)	t ₃₊	3	1.0	3.4	1.1	2.0	3.3	1.1	3.6	
Fall Time (20 to 80%)	t _{3−}	3	1.0	3.4	1.1	2.0	3.3	1.1	3.6	
Shift Frequency	f _{shift}		150		150	200		150		

1. These tests to be performed in sequence as shown.



2. See shift frequency test circuit for test procedures.
3. Reset to zero before performing test.
4. Reset to one before performing test.

ELECTRICAL CHARACTERISTICS (continued)

@ Test Temperature			TEST VOLTAGE VALUES (Volts)					P1	P2	P3	(V _{CC}) Gnd
			V _{IHmax}	V _{ILmin}	V _{IHAmin}	V _{ILAmx}	V _{EE}				
			−30°C	−0.890	−1.890	−1.205	−1.500	−5.2			
			+25°C	−0.810	−1.850	−1.105	−1.475	−5.2			
			+85°C	−0.700	−1.825	−1.035	−1.440	−5.2			
Characteristic	Symbol	Pin Under Test	TEST VOLTAGE APPLIED TO PINS LISTED BELOW					P1	P2	P3	(V _{CC}) Gnd
			V _{IHmax}	V _{ILmin}	V _{IHAmin}	V _{ILAmx}	V _{EE}				
Power Supply Drain Current	I _E	8					8				1, 16
Input Current	I _{inH}	5	5				8				1, 16
		6	6				8				1, 16
		7	7				8				1, 16
		4	4				8				1, 16
	I _{inL}	12	4,5,6,7,9, 10,11,13	12			8				1, 16
Output Voltage Logic 1	V _{OH}	3	6				8	4			1, 16
Output Voltage Logic 0	V _{OL}	3					8	4			1, 16
Threshold Voltage Logic 1	V _{OHA} (Note 1.)	3			6		8	4			1, 16
		3	6	Note 3.		7	8	4			1, 16
		3	6	Note 3.			8		4		1, 16
		3					8			4	1, 16
Threshold Voltage Logic 0	V _{OLA} (Note 1.)	3				6	8	4			1, 16
		3		Note 4.		7	8	4			1, 16
		3		Note 4.			8		4		1, 16
		3	6				8			4	1, 16
Switching Times (50Ω Load)							−3.2 V				+2.0 V
Propagation Delay	t ₄₊₃₊	3					8				1, 16
Setup Time (t _{setup})	t ₁₂₊₄₊	14					8				1, 16
	t ₁₀₊₄₊	14					8				1, 16
Hold Time (t _{hold})	t ₄₊₁₂₊	14					8				1, 16
Rise Time (20 to 80%)	t ₃₊	3					8				1, 16
Fall Time (20 to 80%)	t _{3−}	3					8				1, 16
Shift Frequency	f _{shift}		Note 2.				8				1, 16

- These tests to be performed in sequence as shown.

P1

P2

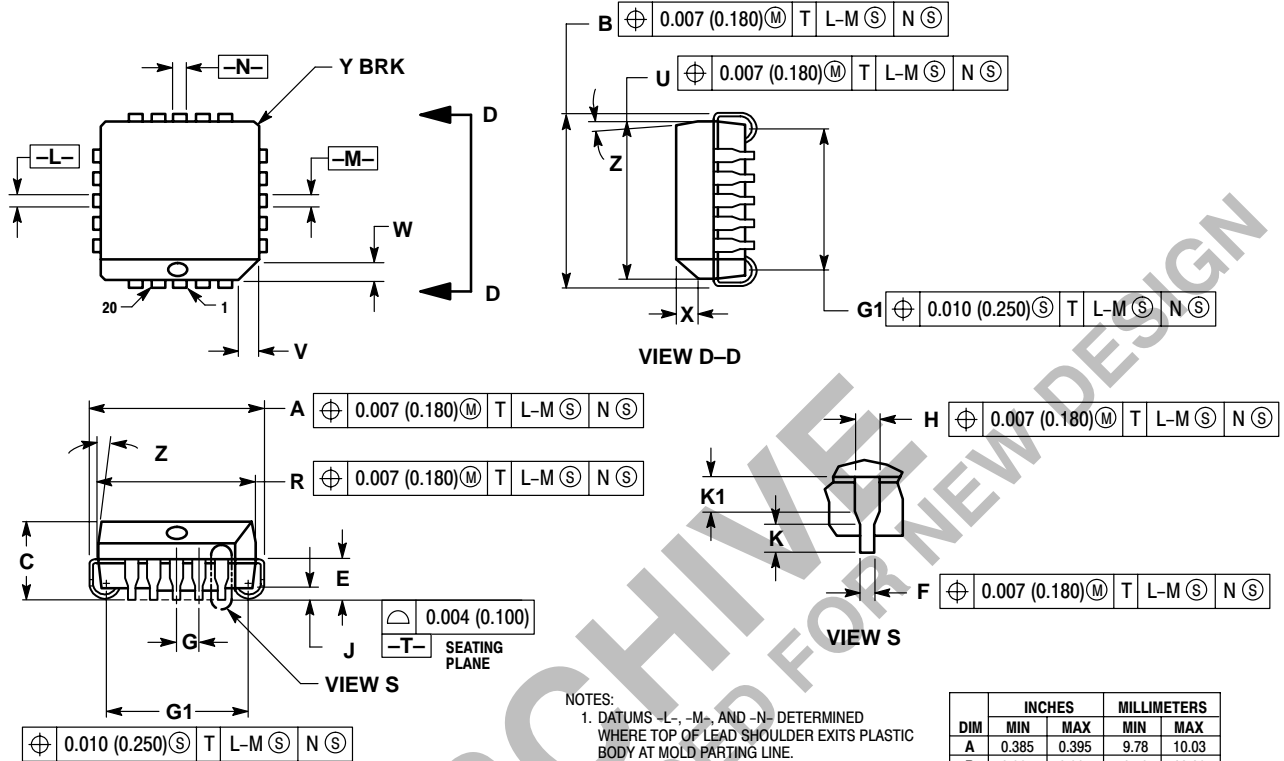
P3
- See shift frequency test circuit for test procedures.
- Reset to zero before performing test.
- Reset to one before performing test.

Each MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to −2.0 volts. Test procedures are shown for only one gate. The other gates are tested in the same manner.

MC10141

PACKAGE DIMENSIONS

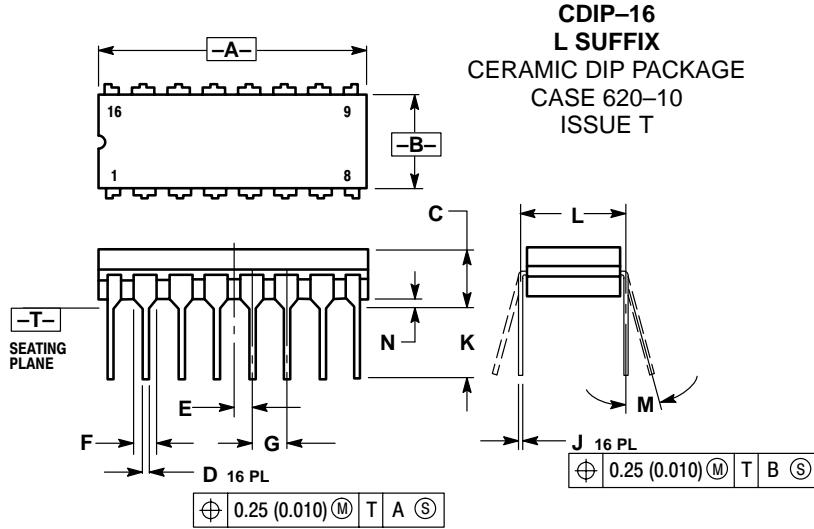
PLCC-20
FN SUFFIX
PLASTIC PLCC PACKAGE
CASE 775-02
ISSUE C



DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.385	0.395	9.78	10.03
B	0.385	0.395	9.78	10.03
C	0.165	0.180	4.20	4.57
E	0.090	0.110	2.29	2.79
F	0.013	0.019	0.33	0.48
G	0.050 BSC		1.27 BSC	
H	0.026	0.032	0.66	0.81
J	0.020	---	0.51	---
K	0.025	---	0.64	---
R	0.350	0.356	8.89	9.04
U	0.350	0.356	8.89	9.04
V	0.042	0.048	1.07	1.21
W	0.042	0.048	1.07	1.21
X	0.042	0.056	1.07	1.42
Y	---	0.020	---	0.50
Z	2 °	10 °	2 °	10 °
G1	0.310	0.330	7.88	8.38
K1	0.040	---	1.02	---

MC10141

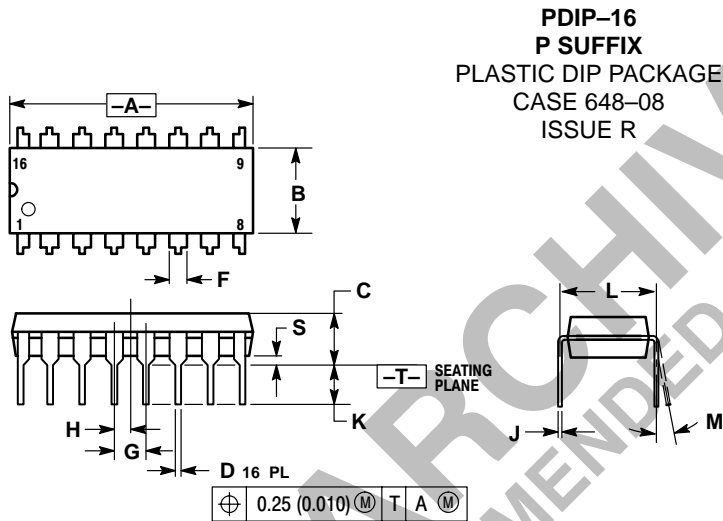
PACKAGE DIMENSIONS



NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.
4. DIMENSION F MAY NARROW TO 0.76 (0.030) WHERE THE LEAD ENTERS THE CERAMIC BODY.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.750	0.785	19.05	19.93
B	0.240	0.295	6.10	7.49
C	---	0.200	---	5.08
D	0.015	0.020	0.39	0.50
E	0.050 BSC		1.27 BSC	
F	0.055	0.065	1.40	1.65
G	0.100 BSC		2.54 BSC	
H	0.008	0.015	0.21	0.38
K	0.125	0.170	3.18	4.31
L	0.300 BSC		7.62 BSC	
M	0°	15°	0°	15°
N	0.020	0.040	0.51	1.01



NOTES:


1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.
5. ROUNDED CORNERS OPTIONAL.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.740	0.770	18.80	19.55
B	0.250	0.270	6.35	6.85
C	0.145	0.175	3.69	4.44
D	0.015	0.021	0.39	0.53
F	0.040	0.70	1.02	1.77
G	0.100 BSC		2.54 BSC	
H	0.050 BSC		1.27 BSC	
J	0.008	0.015	0.21	0.38
K	0.110	0.130	2.80	3.30
L	0.295	0.305	7.50	7.74
M	0°	10°	0°	10°
S	0.020	0.040	0.51	1.01

Notes

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DEVICE NOT RECOMMENDED FOR NEW DESIGN

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