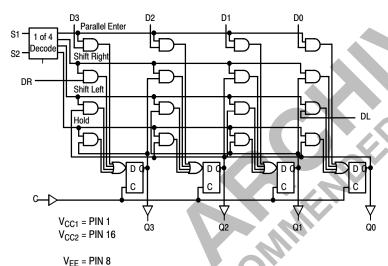
Four Bit Universal Shift Register

The MC10141 is a four—bit universal shift register which performs shift left, or shift right, serial/parallel in, and serial/parallel out operations with no external gating. Inputs S1 and S2 control the four possible operations of the register without external gating of the clock. The flip—flops shift information on the positive edge of the clock. The four operations are stop shift, shift left, shift right, and parallel entry of data. The other six inputs are all data type inputs; four for parallel entry data, and one for shifting in from the left (DL) and one for shifting in from the right (DR).

- $P_D = 425 \text{ mW typ/pkg (No Load)}$
- $f_{Shift} = 200 \text{ MHz typ}$
- t_r , $t_f = 2.0$ ns typ (20%–80%)

LOGIC DIAGRAM



TRUTH TABLE

SEL	ECT			OUTF	PUTS	
S1	S2	OPERATING MODE	Q0 _{n+1}	Q1 _{n+1}	Q2 _{n+1}	Q3 _{n+1}
L	L	Parallel Entry	D0	D1	D2	D3
L	Н	Shift Right*	Q1 _n	Q2 _n	Q3 _n	DR
Н	L	Shift Left*	DL	Q0 _n	Q1 _n	Q2 _n
Н	Н	Stop Shift	Q0 _n	Q1 _n	Q2 _n	Q3 _n

^{*}Outputs as exist after pulse appears at "C" input with input conditions as shown. (Pulse = Positive transition of clock input).



ON Semiconductor

http://onsemi.com

MARKING DIAGRAMS



CDIP-16 L SUFFIX CASE 620 MC10141L AWLYYWW



PDIP-16 P SUFFIX CASE 648





PLCC-20 FN SUFFIX CASE 775



A = Assembly Location

WL = Wafer Lot YY = Year

WW = Work Week

DIP PIN ASSIGNMENT

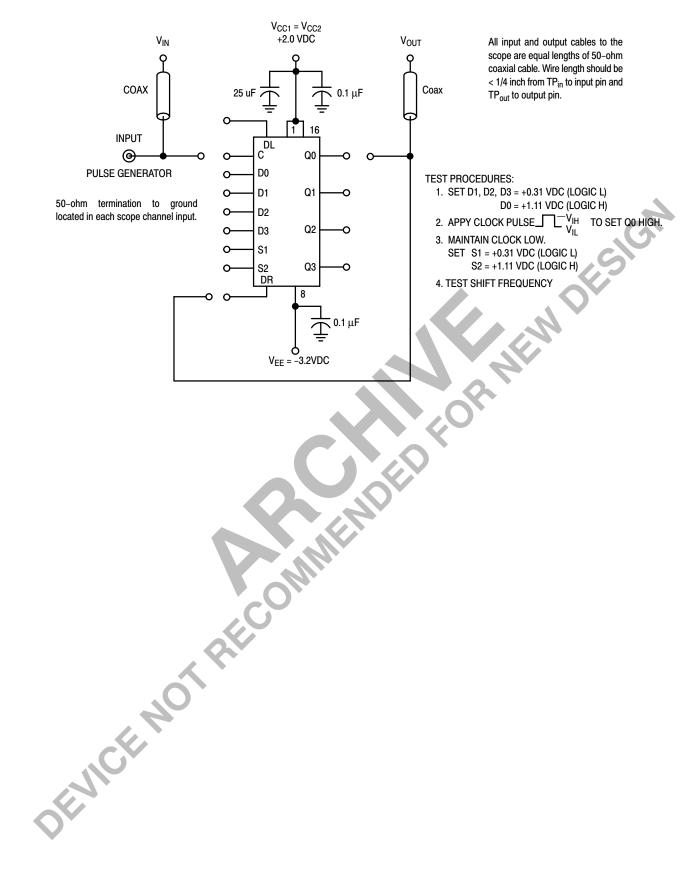
	1		、 ァ		1	
V_{CC1}		1	_	16		V_{CC2}
Q2		2		15		Q1
Q3		3		14		Q0
С		4		13		DL
DR		5		12		D0
D3		6		11		D1
S2		7		10		S1
V_{EE}		8		9		D2

Pin assignment is for Dual–in–Line Package.
For PLCC pin assignment, see the Pin Conversion Tables on page 18 of the ON Semiconductor MECL Data Book (DL122/D).

ORDERING INFORMATION

Device	Package	Shipping
MC10141L	CDIP-16	25 Units / Rail
MC10141P	PDIP-16	25 Units / Rail
MC10141FN	PLCC-20	46 Units / Rail

SHIFT FREQUENCY TEST CIRCUIT



ELECTRICAL CHARACTERISTICS

	8 5 6 7 4 12 3 3 .) 3 3 .) 3 3 3 4 14 14	0.5 -1.060 -1.890 -1.080 -1.080 -1.080 -1.080 -1.080 -1.080 -1.080	-1.675 -1.655 -1.655 -1.655 -3.9	-0.980 -0.980 -0.980 -0.980	+25°C Typ 82	Max 102 220 220 245 265 -0.810 -1.650 -1.630 -1.630 -1.630 3.8	0.3 -0.890 -1.825 -0.910 -0.910 -0.910 2.0 2.5 5.5 1.5	5°C Max 112 220 220 245 265 -0.700 -1.615 -1.595 -1.595 -1.595 -1.595 4.2	Un mAc μAc Vd Vd Vd
Power Supply Drain Current I _E	8 5 6 7 4 12 3 .) 3 .) 3 3 .) 3 14 14 14 14 3	0.5 -1.060 -1.890 -1.080 -1.080 -1.080 -1.080 1.7 2.5 5.5 1.5 1.0	112 350 350 390 425 -0.890 -1.675 -1.655 -1.655 -1.655 3.9	0.5 -0.960 -1.850 -0.980 -0.980 -0.980 -0.980 1.8 2.5 5.0 1.5	2.9	102 220 220 245 265 -0.810 -1.650 -1.630 -1.630 -1.630	0.3 -0.890 -1.825 -0.910 -0.910 -0.910 -0.910 2.0 2.5 5.5	220 220 245 265 -0.700 -1.615 -1.595 -1.595 -1.595	mAc μAc Vd Vd
rent	5 6 7 4 12 3 3 3 3 3 3 3 3 3 3 3 3 3 3 3 3 3 3	-1.060 -1.890 -1.080 -1.080 -1.080 -1.080 -1.080 -1.080 -1.080	350 350 390 425 -0.890 -1.675 -1.655 -1.655 -1.655 3.9	-0.960 -1.850 -0.980 -0.980 -0.980 -0.980 1.8 2.5 5.0 1.5	2.9	220 220 245 265 -0.810 -1.650 -1.630 -1.630 -1.630	-0.890 -1.825 -0.910 -0.910 -0.910 -0.910 2.0 2.5 5.5	220 220 245 265 -0.700 -1.615 -1.595 -1.595 -1.595	μΑσ Vd Vd
I _{inL}	6 7 4 12 3 3 3 3 3 3 3 3 3 3 3 3 3 3 3 3 3 3	-1.060 -1.890 -1.080 -1.080 -1.080 -1.080 -1.080 -1.080 -1.080	350 390 425 -0.890 -1.675 -1.655 -1.655 -1.655 3.9	-0.960 -1.850 -0.980 -0.980 -0.980 -0.980 1.8 2.5 5.0 1.5	O	220 245 265 -0.810 -1.650 -1.630 -1.630 -1.630	-0.890 -1.825 -0.910 -0.910 -0.910 -0.910 2.0 2.5 5.5	220 245 265 -0.700 -1.615 -1.595 -1.595 -1.595 -1.595	μAα Vd Vd Vd
$\begin{array}{c cccc} \text{Output Voltage} & \text{Logic 1} & \text{V}_{OH} \\ \text{Output Voltage} & \text{Logic 0} & \text{V}_{OL} \\ \text{Threshold Voltage} & \text{Logic 1} & \text{V}_{OHA} \\ \text{(Note 1} \\ \end{array}$ $\begin{array}{c ccccccccccccccccccccccccccccccccccc$	7 4 12 3 3 3 3 3 3 3 3 3 3 3 3 3 3 3 3 3 3	-1.060 -1.890 -1.080 -1.080 -1.080 -1.080 -1.080 -1.080 -1.080	390 425 -0.890 -1.675 -1.655 -1.655 -1.655 3.9	-0.960 -1.850 -0.980 -0.980 -0.980 -0.980 1.8 2.5 5.0 1.5	O	245 265 -0.810 -1.650 -1.630 -1.630 -1.630	-0.890 -1.825 -0.910 -0.910 -0.910 -0.910 2.0 2.5 5.5	245 265 -0.700 -1.615 -1.595 -1.595 -1.595 -1.595	Vd Vd
$\begin{array}{c cccc} \text{Output Voltage} & \text{Logic 1} & \text{V}_{OH} \\ \text{Output Voltage} & \text{Logic 0} & \text{V}_{OL} \\ \text{Threshold Voltage} & \text{Logic 1} & \text{V}_{OHA} \\ \text{(Note 1} \\ \end{array}$ $\begin{array}{c ccccccccccccccccccccccccccccccccccc$	4 12 3 3 3 3 3 3 3 3 3 3 3 3 3 3 3 3 3 3	-1.060 -1.890 -1.080 -1.080 -1.080 -1.080 -1.080 -1.080 -1.080	-1.655 -1.655 -1.655 -1.655 -3.9	-0.960 -1.850 -0.980 -0.980 -0.980 -0.980 1.8 2.5 5.0 1.5	O	-1.630 -1.630 -1.630 -1.630	-0.890 -1.825 -0.910 -0.910 -0.910 -0.910 2.0 2.5 5.5	-0.700 -1.615 -1.595 -1.595 -1.595 -1.595	Vo
$\begin{array}{c cccc} \text{Output Voltage} & \text{Logic 1} & \text{V}_{OH} \\ \text{Output Voltage} & \text{Logic 0} & \text{V}_{OL} \\ \text{Threshold Voltage} & \text{Logic 1} & \text{V}_{OHA} \\ \text{(Note 1} \\ \end{array}$ $\begin{array}{c ccccccccccccccccccccccccccccccccccc$	3 3 3 3 3 3 3 3 3 3 3 4 14 14 14 3	-1.060 -1.890 -1.080 -1.080 -1.080 -1.080 -1.080 -1.080 -1.080	-1.675 -1.655 -1.655 -1.655 3.9	-0.960 -1.850 -0.980 -0.980 -0.980 -0.980 1.8 2.5 5.0 1.5	O	-1.650 -1.630 -1.630 -1.630 -1.630	-0.890 -1.825 -0.910 -0.910 -0.910 -0.910 2.0 2.5 5.5	-1.615 -1.595 -1.595 -1.595 -1.595	Vo
$ \begin{array}{c cccc} Output \ Voltage & Logic \ 0 & V_{OL} \\ \hline Threshold \ Voltage & Logic \ 1 & V_{OHA} \\ (Note \ 1 & V_{OHA} \\ (Note \ 1 & V_{OLA} \\ (Note \ 1 &$	3 .) 3 3 3 3 .) 3 3 3 .) 3 14 14 14 14 3	-1.890 -1.080 -1.080 -1.080 -1.080 -1.080	-1.675 -1.655 -1.655 -1.655 3.9	1.8 2.5 5.0 1.5	O	-1.650 -1.630 -1.630 -1.630 -1.630	-1.825 -0.910 -0.910 -0.910 -0.910 2.0 2.5 5.5	-1.615 -1.595 -1.595 -1.595 -1.595	Vo
Threshold Voltage Logic 1 V_{OHA} (Note 1 $V_$	3 3 3 3 3 3 3 3 3 3 3 3 4 14 14 14 3	-1.080 -1.080 -1.080 -1.080 -1.080	-1.655 -1.655 -1.655 -1.655 -3.9	-0.980 -0.980 -0.980 -0.980 1.8 2.5 5.0 1.5	O	-1.630 -1.630 -1.630 -1.630	-0.910 -0.910 -0.910 -0.910 -2.910	-1.595 -1.595 -1.595 -1.595	Vo
Threshold Voltage Logic 0 V_{OLA} (Note 1 V_{OLA} (Note 1 V_{OLA}) Switching Times (50 Ω) Load) Propagation Delay V_{OLA} (Note 1 V_{OLA}) Setup Time (V_{Setup}) Hold Time (V_{Setup}) Rise Time (20 to 80%) Fall Time (20 to 80%) Shift Frequency These tests to be performed in sequence.	.) 3 3 3 3 .) 3 3 3 3 14 14 14 14 3	-1.080 -1.080 -1.080 -1.080 -1.080	-1.655 -1.655 -1.655 -1.655 3.9	-0.980 -0.980 -0.980 -0.980 1.8 2.5 5.0 1.5	O	-1.630 -1.630 -1.630	-0.910 -0.910 -0.910 -0.910 2.0 2.5 5.5	-1.595 -1.595 -1.595	Vo
Threshold Voltage Logic 0 V_{OLA} (Note 1 V_{OLA}) Switching Times (50 Ω) Load) Propagation Delay V_{OLA} Setup Time (V_{Setup}) Hold Time (V_{Setup}) Rise Time (20 to 80%) V_{OLA} Fall Time (20 to 80%) V_{OLA} Shift Frequency V_{OLA}	3 3 3 3 3 3 3 3 3 14 14 14 14 3	-1.080 -1.080 -1.080	-1.655 -1.655 -1.655 -1.655 3.9	-0.980 -0.980 1.8 2.5 5.0 1.5	O	-1.630 -1.630 -1.630	-0.910 -0.910 2.0 2.5 5.5	-1.595 -1.595 -1.595	
$\begin{array}{c} \text{Switching Times} & (50\Omega \\ \text{Load}) \\ \text{Propagation Delay} & t_{4+3+} \\ \text{Setup TIme } (t_{\text{setup}}) & t_{12+4+} \\ t_{10+4+} \\ \text{Hold Time } (t_{\text{hold}}) & t_{4+12+} \\ \text{Rise Time} & (20 \text{ to } 80\%) & t_{3+} \\ \text{Fall Time} & (20 \text{ to } 80\%) & t_{3-} \\ \text{Shift Frequency} & f_{\text{shift}} \\ \end{array}$	3 3 3 3 3 3 3 14 14 14 14 3	1.7 2.5 5.5 1.0	-1.655 -1.655 -1.655 -1.655 3.9	-0.980 1.8 2.5 5.0 1.5	O	-1.630 -1.630 -1.630	2.0 2.5 5.5	-1.595 -1.595 -1.595	
$\begin{array}{c} \text{Switching Times} & (50\Omega \\ \text{Load}) \\ \text{Propagation Delay} & t_{4+3+} \\ \text{Setup TIme } (t_{\text{setup}}) & t_{12+4+} \\ t_{10+4+} \\ \text{Hold Time } (t_{\text{hold}}) & t_{4+12+} \\ \text{Rise Time} & (20 \text{ to } 80\%) & t_{3+} \\ \text{Fall Time} & (20 \text{ to } 80\%) & t_{3-} \\ \text{Shift Frequency} & f_{\text{shift}} \\ \end{array}$	3 3 3 3 14 14 14 3	2.5 5.5 1.5 1.0	-1.655 -1.655 -1.655 -3.9	1.8 2.5 5.0 1.5	O	-1.630 -1.630 -1.630	2.5 5.5	-1.595 -1.595 -1.595	
Switching Times (50Ω) Load) Propagation Delay t_{4+3+} t_{10+4+} t_{10+4+} Hold Time (t_{hold}) t_{4+12+} Rise Time $(20 \text{ to } 80\%)$ t_{3+} Fall Time $(20 \text{ to } 80\%)$ t_{3-} Shift Frequency t_{hold} t_{hold}	3 3 14 14 14 3	2.5 5.5 1.5 1.0	-1.655 -1.655 3.9	1.8 2.5 5.0 1.5	O	-1.630 -1.630	2.5 5.5	-1.595 -1.595	n:
$ \begin{array}{c ccccccccccccccccccccccccccccccccccc$	3 3 14 14 14 3	2.5 5.5 1.5 1.0	3.9	1.8 2.5 5.0 1.5	O	-1.630	2.5 5.5	-1.595	n:
Load) $ \begin{array}{c} \text{Load)} \\ \text{Propagation Delay} \\ \text{Setup TIme } (t_{\text{Setup}}) \\ \text{Hold Time } (t_{\text{hold}}) \\ \text{Rise Time} \\ \text{C20 to 80\%)} \\ \text{Fall Time} \\ \text{Shift Frequency} \\ \end{array} \begin{array}{c} t_{4+3+} \\ t_{10+4+} \\ t_{4+12+} \\ t_{4+12+} \\ t_{4+12+} \\ t_{3+} \\ t_{4+12+} \\ t_{4+12+} \\ t_{4+12+} \\ t_{5+12+} \\ t_{4+12+} \\ t_{10+4+} \\ t_{4+12+} \\ t_{4+$	3 14 14 14 3	2.5 5.5 1.5 1.0	3.9	1.8 2.5 5.0 1.5	O		2.5 5.5		n
Propagation Delay Setup TIme (t_{setup}) t_{4+3+} t_{12+4+} t_{10+4+} t_{10+4+} t_{4+12+} Rise Time (20 to 80%) t_{3+} Fall Time (20 to 80%) t_{3-} Shift Frequency t_{shift}	14 14 14 3	2.5 5.5 1.5 1.0	3.4	2.5 5.0 1.5	O	3.8	2.5 5.5	4.2	
$\begin{array}{cccccccccccccccccccccccccccccccccccc$	14 14 14 3	2.5 5.5 1.5 1.0	3.4	2.5 5.0 1.5	O	>	2.5 5.5		
Hold Time (t_{hold}) Rise Time (20 to 80%) Fall Time (20 to 80%) Shift Frequency t_{3+} t_{3+} t_{3-} Shift Frequency I. These tests to be performed in sequence	14 3	1.5 1.0		1.5	10,				1
Rise Time (20 to 80%) t_{3+} Fall Time (20 to 80%) t_{3-} Shift Frequency f_{shift} These tests to be performed in sequence.	3	1.0					1.5		
Fall Time (20 to 80%) t_{3-} Shift Frequency f_{shift} 1. These tests to be performed in sequence f_{shift}				1.1		۱			
Shift Frequency f _{shift} 1. These tests to be performed in sequence in sequen	3	1.0			2.0	3.3	1.1	3.6	
. These tests to be performed in sequ	1		3.4	1.1	2.0	3.3	1.1	3.6	
		150		150	200		150		MI
Reset to one before performing tes:				V _{IH} P	22	─ V _{IHA} ─ V _{IL}	P3	V _{II}	
401		BILL							
NOT!	,G								
407	2								
40	•								
. ()									
V									
~									



ELECTRICAL CHARACTERISTICS (continued)

				TEST VOL	TAGE VALU	JES (Volts)					
(@ Test Tem	perature	V _{IHmax}	V _{ILmin}	V _{IHAmin}	V _{ILAmax}	V _{EE}				
		–30°C	-0.890	-1.890	-1.205	-1.500	-5.2				
		+25°C	-0.810	-1.850	-1.105	-1.475	-5.2				
		+85°C	-0.700	-1.825	-1.035	-1.440	-5.2				
		Pin	TEST VOL	TAGE APP	LIED TO P	INS LISTED	BELOW				
Characteristic	Symbol	Under Test	V _{IHmax}	V _{ILmin}	V _{IHAmin}	V _{ILAmax}	V _{EE}	P1	P2	Р3	(V _{CC}) Gnd
Power Supply Drain Current	ΙE	8					8				1, 16
Input Current	l _{inH}	5 6 7 4	5 6 7 4				8 8 8				1, 16 1, 16 1, 16 1, 16
	l _{inL}	12	4,5,6,7,9, 10,11,13	12			8				1, 16
Output Voltage Logic 1	V _{OH}	3	6				8	4	K		1, 16
Output Voltage Logic 0	V _{OL}	3					8	4			1, 16
Threshold Voltage Logic 1	V _{OHA} (Note 1.)	3 3 3 3	6	Note 3. Note 3.	6	7	8 8 8 8	4 4	4	4	1, 16 1, 16 1, 16 1, 16
Threshold Voltage Logic 0	V _{OLA} (Note 1.)	3 3 3	6	Note 4. Note 4.		6 7	8 8 8 8	4	4	4	1, 16 1, 16 1, 16 1, 16
Switching Times (50Ω Load)					\		−3.2 V				+2.0 V
Propagation Delay Setup Time (t_{setup}) Hold Time (t_{hold})	t ₄₊₃₊ t ₁₂₊₄₊ t ₁₀₊₄₊ t ₄₊₁₂₊	3 14 14 14	C				8 8 8				1, 16 1, 16 1, 16 1, 16
Rise Time (20 to 80%)	t ₃₊	3		47			8				1, 16
Fall Time (20 to 80%)	t ₃₋	3					8				1, 16
Shift Frequency	f _{shift}		Note 2.				8				1, 16

2. See shift frequency test circuit for test procedures.

Each MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibitum has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to -2.0 volts. Test procedures are shown for only one gate. The other gates are tested in the same manner.

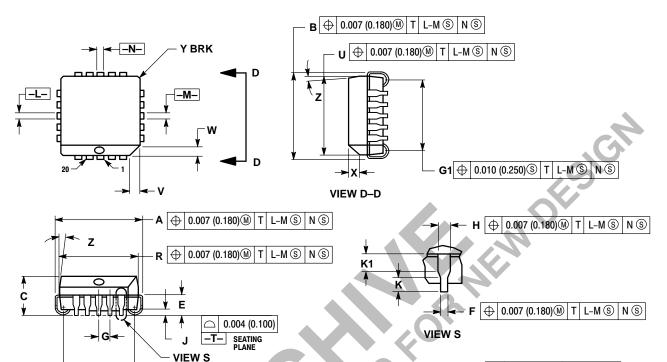
^{3.} Reset to zero before performing test.

^{4.} Reset to one before performing test.

PACKAGE DIMENSIONS

PLCC-20 **FN SUFFIX**

PLASTIC PLCC PACKAGE CASE 775-02 ISSUE C



NOTES:

G1 ⊕ 0.010 (0.250)③ T L-M ⑤ N ⑤

OF VICE NOT PRESCO

- IOTES:

 1. DATUMS -L-, -M-, AND -N- DETERMINED WHERE TOP OF LEAD SHOULDER EXITS PLASTIC BODY AT MOLD PARTING LINE.

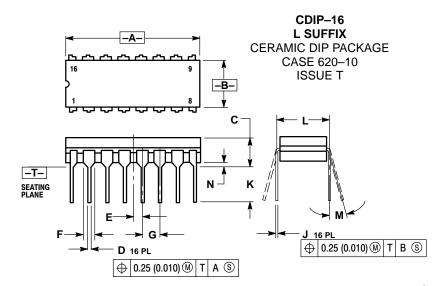
 2. DIMENSION G1, TRUE POSITION TO BE MEASURED AT DATUM -T-, SEATING PLANE.

 3. DIMENSIONS R AND U DO NOT INCLUDE MOLD FLASH. ALLOWABLE MOLD FLASH IS 0.010 (0.250) PER SIDE.

 4. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M. 1982.
- Y14.5M, 1982. CONTROLLING DIMENSION: INCH.
- THE PACKAGE TOP MAY BE SMALLER THAN THE PACKAGE BOTTOM BY UP TO 0.012 (0.300). DIMENSIONS R AND U ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY EXCLUSIVE OF MOLD FLASH, TIE BAR BURRS, GATE BURRS AND INTERLEAD FLASH, BUT INCLUDING ANY MISMATCH BETWEEN THE TOP AND BOTTOM OF THE PLASTIC BODY.
- DIMENSION H DOES NOT INCLUDE DAMBAR PROTRUSION OR INTRUSION. THE DAMBAR PROTRUSION(S) SHALL NOT CAUSE THE H DIMENSION TO BE GREATER THAN 0.037 (0.940). THE DAMBAR INTRUSION(S) SHALL NOT CAUSE THE H DIMENSION TO BE SMALLER THAN 0.025 (0.635).

	INC	HES	MILLIM	ETERS
DIM	MIN	MAX	MIN	MAX
Α	0.385	0.395	9.78	10.03
В	0.385	0.395	9.78	10.03
С	0.165	0.180	4.20	4.57
E	0.090	0.110	2.29	2.79
F	0.013	0.019	0.33	0.48
G	0.050	BSC	1.27	BSC
Н	0.026	0.032	0.66	0.81
J	0.020		0.51	
K	0.025		0.64	
R	0.350	0.356	8.89	9.04
U	0.350	0.356	8.89	9.04
٧	0.042	0.048	1.07	1.21
W	0.042	0.048	1.07	1.21
X	0.042	0.056	1.07	1.42
Y		0.020		0.50
Z	2°	10°	2°	10 °
G1	0.310	0.330	7.88	8.38
K1	0.040		1.02	

PACKAGE DIMENSIONS



NOTES:

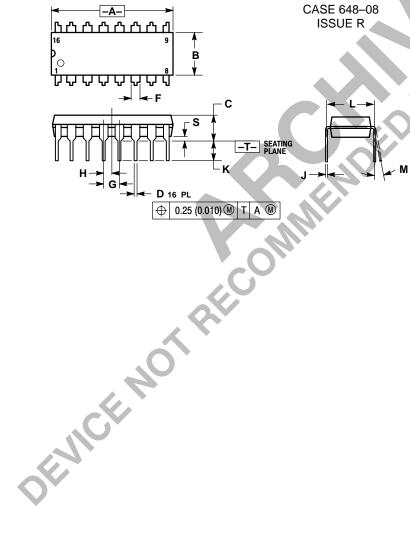
- DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 CONTROLLING DIMENSION: INCH.
 DIMENSION LTO CENTER OF LEAD WHEN CONTROLLING DIMENSION LTO CENTER OF LEAD WHEN

- FORMED PARALLEL

 DIMENSION F MAY NARROW TO 0.76 (0.030)
 WHERE THE LEAD ENTERS THE CERAMIC
 BODY.

	INC	HES	MILLIN	IETERS	
DIM	MIN	MAX	MIN	MAX	
Α	0.750	0.785	19.05	19.93	
В	0.240	0.295	6.10	7.49	
С		0.200		5.08	
D	0.015	0.020	0.39	0.50	
E	0.050	BSC	1.27 BSC		
F	0.055	0.065	1.40	1.65	
G	0.100	.100 BSC 2.54 B			
Н	0.008	0.015	0.21	0.38	
K	0.125	0.170	3.18	4.31	
L	0.300	300 BSC 7.62 BS		BSC	
М	0 °	15°	0 °	15°	
N	0.020	0.040	0.51	1.01	

PDIP-16 **P SUFFIX** PLASTIC DIP PACKAGE CASE 648-08 ISSUE R



- NOTES:
 1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 2. CONTROLLING DIMENSION: INCH.
 3. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
 4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.
 5. ROUNDED CORNERS OPTIONAL

	INC	HES	MILLIN	IETERS	
DIM	MIN	MAX	MIN	MAX	
Α	0.740	0.770	18.80	19.55	
В	0.250	0.270	6.35	6.85	
С	0.145	0.175	3.69	4.44	
D	0.015	0.021	0.39	0.53	
F	0.040	0.70	1.02	1.77	
G	0.100	BSC	2.54 BSC		
Н	0.050	BSC	1.27	BSC	
J	0.008	0.015	0.21	0.38	
K	0.110	0.130	2.80	3.30	
L	0.295	0.305	7.50	7.74	
M	0°	10°	0°	10 °	
S	0.020	0.040	0.51	1.01	

Notes





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