



# Dual-Voltage $\mu$ P Supervisory Circuits with Sequenced Reset Outputs

## General Description

The MAX6391/MAX6392 microprocessor ( $\mu$ P) supervisory circuits provide sequenced logic reset outputs for multi-component or dual-voltage systems. Each device can monitor two supply voltages and time-sequence two reset outputs to control the order in which system components are turned on and off. The MAX6391/MAX6392 increase system reliability and reduce circuit complexity and cost compared to separate ICs or discrete components.

The MAX6391/MAX6392 monitor  $V_{CC}$  as the master reset supply. Both  $\overline{\text{RESET1}}$  and  $\overline{\text{RESET2}}$  are asserted whenever  $V_{CC}$  drops below the selected factory-fixed reset threshold voltage.  $\overline{\text{RESET1}}$  remains asserted as long as  $V_{CC}$  is below the threshold and deasserts 140ms (min) after  $V_{CC}$  exceeds the thresholds.

RESET IN2 is monitored as the secondary reset supply and is adjustable with an external resistive-divider network.  $\overline{\text{RESET2}}$  is asserted whenever either  $V_{CC}$  or RESET IN2 is below the selected thresholds.  $\overline{\text{RESET2}}$  remains asserted 140ms (min) or a capacitor-adjustable time period after  $V_{CC}$  and RESET IN2 exceed their thresholds.  $\overline{\text{RESET2}}$  is always deasserted after  $\overline{\text{RESET1}}$  during system power-up and is always asserted before  $\overline{\text{RESET1}}$  during power-down.

The MAX6391 includes two internal pullup resistors for  $\overline{\text{RESET1}}$  and  $\overline{\text{RESET2}}$  (the open-drain outputs can be externally connected to the desired pullup voltages). The MAX6392 includes an active-low manual reset input ( $\overline{\text{MR}}$ ) that asserts both  $\overline{\text{RESET1}}$  (push-pull) and  $\overline{\text{RESET2}}$  (open drain).

The MAX6391/MAX6392 are available in small 8-pin SOT23 packages and are specified over the  $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$  extended temperature range.

## Applications

Computers  
Controllers  
Critical  $\mu$ P Power Monitoring  
Set-Top Boxes  
Printers  
Servers/Workstations  
Industrial Equipment  
Multivoltage Monitoring

Typical Operating Circuit appears at end of data sheet.

## Features

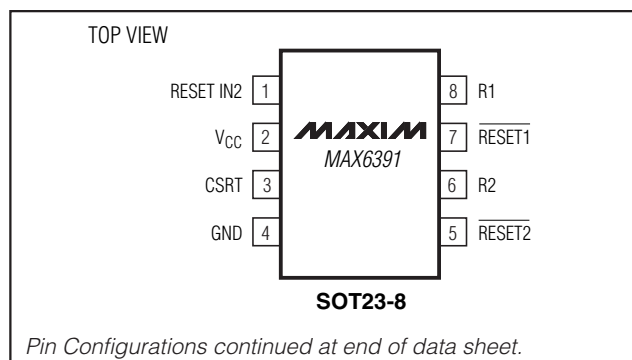
- ◆ Preset  $V_{CC}$  Reset Threshold Voltages from 1.58V to 4.63V (master supply)
- ◆ Customer-Adjustable RESET IN2 to Monitor Voltages Down to 625mV (secondary supply)
- ◆ Fixed (140ms min)  $\overline{\text{RESET1}}$  Timeout
- ◆ Fixed (140ms min) or Customer-Adjustable  $\overline{\text{RESET2}}$  Timeout Period
- ◆ Guaranteed Reset Valid to  $V_{CC} = 1\text{V}$
- ◆ Active-Low Open-Drain Outputs or Push-Pull/Open-Drain Combination
- ◆ Internal Open-Drain Pullup Resistors (for external  $V_{OH}$  voltage connections)
- ◆ Manual Reset Input (MAX6392 only)
- ◆ Immune to Short Negative  $V_{CC}$  Transients
- ◆ 15 $\mu\text{A}$  Typical Supply Current
- ◆ Few External Components
- ◆ Small 8-Pin SOT23 Package

## Ordering Information

| PART*          | TEMP RANGE                                     | PIN-PACKAGE |
|----------------|------------------------------------------------|-------------|
| MAX6391KA_ _-T | $-40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$ | SOT23-8     |
| MAX6392KA_ _-T | $-40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$ | SOT23-8     |

\*Insert the desired suffix (see Selector Guide) into the blanks to complete the part number. The MAX6391/MAX6392 require a 2.5k minimum order increment and are available in tape-and-reel only. Samples are typically available for standard versions (see Selector Guide for standard versions). Contact factory for availability.

## Pin Configurations



# Dual-Voltage $\mu$ P Supervisory Circuits with Sequenced Reset Outputs

## ABSOLUTE MAXIMUM RATINGS

$V_{CC}$  to GND .....-0.3V to +6.0V  
 $\overline{\text{RESET1}}$  (MAX6392), RESET IN2, CSRT,  
 $\overline{\text{MR}}$  to GND .....-0.3V to ( $V_{CC}$  + 0.3V)  
 $\overline{\text{RESET1}}$  (MAX6391), RESET2, R1, R2 to GND .....-0.3V to +6.0V  
 Input Current ( $V_{CC}$ , GND, CSRT, R1, R2,  $\overline{\text{MR}}$ ) ..... $\pm 20$ mA  
 Output Current (RESET1, RESET2) ..... $\pm 20$ mA  
 Continuous Power Dissipation ( $T_A = +70^\circ\text{C}$ )  
 8-Pin SOT23 (derate 5.26mW/ $^\circ\text{C}$  above  $+70^\circ\text{C}$ ) .....421mW

Operating Temperature Range .....-40 $^\circ\text{C}$  to +85 $^\circ\text{C}$   
 Junction Temperature .....+150 $^\circ\text{C}$   
 Storage Temperature Range .....-65 $^\circ\text{C}$  to +150 $^\circ\text{C}$   
 Lead Temperature (soldering, 10s) .....+300 $^\circ\text{C}$

*Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

## ELECTRICAL CHARACTERISTICS

( $V_{CC} = 1.2\text{V}$  to  $5.5\text{V}$ ,  $T_A = T_{\text{MIN}}$  to  $T_{\text{MAX}}$ , unless otherwise specified. Typical values are at  $V_{CC} = +5\text{V}$  and  $T_A = +25^\circ\text{C}$ .) (Note 1)

| PARAMETER                                                 | SYMBOL    | CONDITIONS                                            | MIN  | TYP  | MAX  | UNITS         |
|-----------------------------------------------------------|-----------|-------------------------------------------------------|------|------|------|---------------|
| $V_{CC}$ Range                                            |           | $T_A = 0^\circ\text{C}$ to $+85^\circ\text{C}$        | 1.0  |      | 5.5  | V             |
|                                                           |           | $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$      | 1.2  |      | 5.5  |               |
| Supply Current                                            | $I_{CC}$  | No load                                               |      | 15   | 25   | $\mu\text{A}$ |
| $V_{CC}$ Reset Threshold                                  | $V_{TH1}$ | MAX639_UA46                                           | 4.50 | 4.63 | 4.75 | V             |
|                                                           |           | MAX639_UA44                                           | 4.25 | 4.38 | 4.50 |               |
|                                                           |           | MAX639_UA31                                           | 3.00 | 3.08 | 3.15 |               |
|                                                           |           | MAX639_UA29                                           | 2.85 | 2.93 | 3.00 |               |
|                                                           |           | MAX639_UA26                                           | 2.55 | 2.63 | 2.70 |               |
|                                                           |           | MAX639_UA23                                           | 2.25 | 2.32 | 2.38 |               |
|                                                           |           | MAX639_UA22                                           | 2.12 | 2.19 | 2.25 |               |
|                                                           |           | MAX639_UA17                                           | 1.62 | 1.67 | 1.71 |               |
|                                                           |           | MAX639_UA16                                           | 1.54 | 1.58 | 1.61 |               |
| RESET IN2 Threshold                                       | $V_{TH2}$ | $V_{CC} = 5\text{V}$                                  | 610  | 625  | 640  | mV            |
| RESET IN2 Input Current                                   |           |                                                       |      |      | 50   | nA            |
| $V_{CC}$ to $\overline{\text{RESET1}}$ Delay              | $t_{RD1}$ | $V_{CC}$ falling at $1\text{mV}/\mu\text{s}$ (Note 2) |      | 20   |      | $\mu\text{s}$ |
| $V_{CC}$ or RESET IN2 to $\overline{\text{RESET2}}$ Delay | $t_{RD2}$ |                                                       |      | 10   |      |               |

# Dual-Voltage $\mu$ P Supervisory Circuits with Sequenced Reset Outputs

MAX6391/MAX6392

## ELECTRICAL CHARACTERISTICS (continued)

( $V_{CC} = 1.2V$  to  $5.5V$ ,  $T_A = T_{MIN}$  to  $T_{MAX}$ , unless otherwise specified. Typical values are at  $V_{CC} = +5V$  and  $T_A = +25^\circ C$ .) (Note 1)

| PARAMETER                                          | SYMBOL    | CONDITIONS                                                                   | MIN                                                          | TYP                     | MAX                     | UNITS     |
|----------------------------------------------------|-----------|------------------------------------------------------------------------------|--------------------------------------------------------------|-------------------------|-------------------------|-----------|
| RESET1 Timeout Period                              | $t_{RP1}$ |                                                                              | 140                                                          | 200                     | 280                     | ms        |
| RESET2 Timeout Period (Note 3)                     | $t_{RP2}$ | CCSRT = 1500pF                                                               | 2.2                                                          | 3.1                     | 4.0                     | ms        |
|                                                    |           | CCSRT = $V_{CC}$                                                             | 140                                                          | 200                     | 280                     |           |
| RESET_ Output Voltage Low                          | $V_{OL}$  | $I_{SINK} = 50\mu A$ ,<br>reset asserted                                     | $V_{CC} \geq 1.0V$ ,<br>$T_A = 0^\circ C$ to $+85^\circ C$   |                         | 0.3                     | V         |
|                                                    |           |                                                                              | $V_{CC} \geq 1.2V$ ,<br>$T_A = -40^\circ C$ to $+85^\circ C$ |                         | 0.3                     |           |
|                                                    |           | $I_{SINK} = 1.2mA$ , reset asserted, $V_{CC} \geq 2.5V$                      |                                                              |                         | 0.3                     |           |
|                                                    |           | $I_{SINK} = 3.2mA$ , reset asserted, $V_{CC} \geq 4.25V$                     |                                                              |                         | 0.4                     |           |
| Open-Drain RESET Output Leakage Current            | $I_{LKG}$ | $V_{CC} \geq V_{TH1}$ , $V_{RESET IN2} \geq V_{TH2}$ ,<br>reset not asserted |                                                              |                         | 1.0                     | $\mu A$   |
| Push-Pull RESET Output Voltage High (MAX6392 only) | $V_{OH}$  | $V_{CC} \geq 2.25V$ , $I_{SOURCE} = 500\mu A$ ,<br>reset not asserted        |                                                              |                         | 0.8 $\star$<br>$V_{CC}$ | V         |
|                                                    |           | $V_{CC} \geq 4.5V$ , $I_{SOURCE} = 800\mu A$ , reset not<br>asserted         |                                                              |                         |                         |           |
| MR Input                                           | $V_{IL}$  | $V_{CC} > 4.0V$                                                              |                                                              |                         | 0.8                     | V         |
|                                                    | $V_{IH}$  |                                                                              | 2.4                                                          |                         |                         |           |
|                                                    | $V_{IL}$  | $V_{CC} < 4.0V$                                                              |                                                              |                         | 0.3 $\star$<br>$V_{CC}$ |           |
|                                                    | $V_{IH}$  |                                                                              |                                                              | 0.7 $\star$<br>$V_{CC}$ |                         |           |
| MR Minimum Pulse Width                             |           |                                                                              | 50                                                           |                         |                         | $\mu s$   |
| MR Glitch Rejection                                |           |                                                                              |                                                              | 100                     |                         | ns        |
| MR to RESET1 Delay                                 | $t_{MR1}$ |                                                                              |                                                              | 10                      |                         | $\mu s$   |
| MR to RESET2 Delay                                 | $t_{MR2}$ |                                                                              |                                                              | 100                     |                         | ns        |
| tMR Skew                                           |           | $t_{MR1} - t_{MR2}$                                                          |                                                              | 10                      |                         | $\mu s$   |
| MR Pullup Resistance                               |           | Pullup to $V_{CC}$                                                           | 35                                                           | 47                      | 60                      | $k\Omega$ |
| Reset Pullup Resistance                            |           | RESET1 to R1 or RESET2 to R2                                                 | 35                                                           | 47                      | 60                      | $k\Omega$ |

**Note 1:** Overtemperature limits are guaranteed by design and not production tested. Devices tested at  $+25^\circ C$  only.

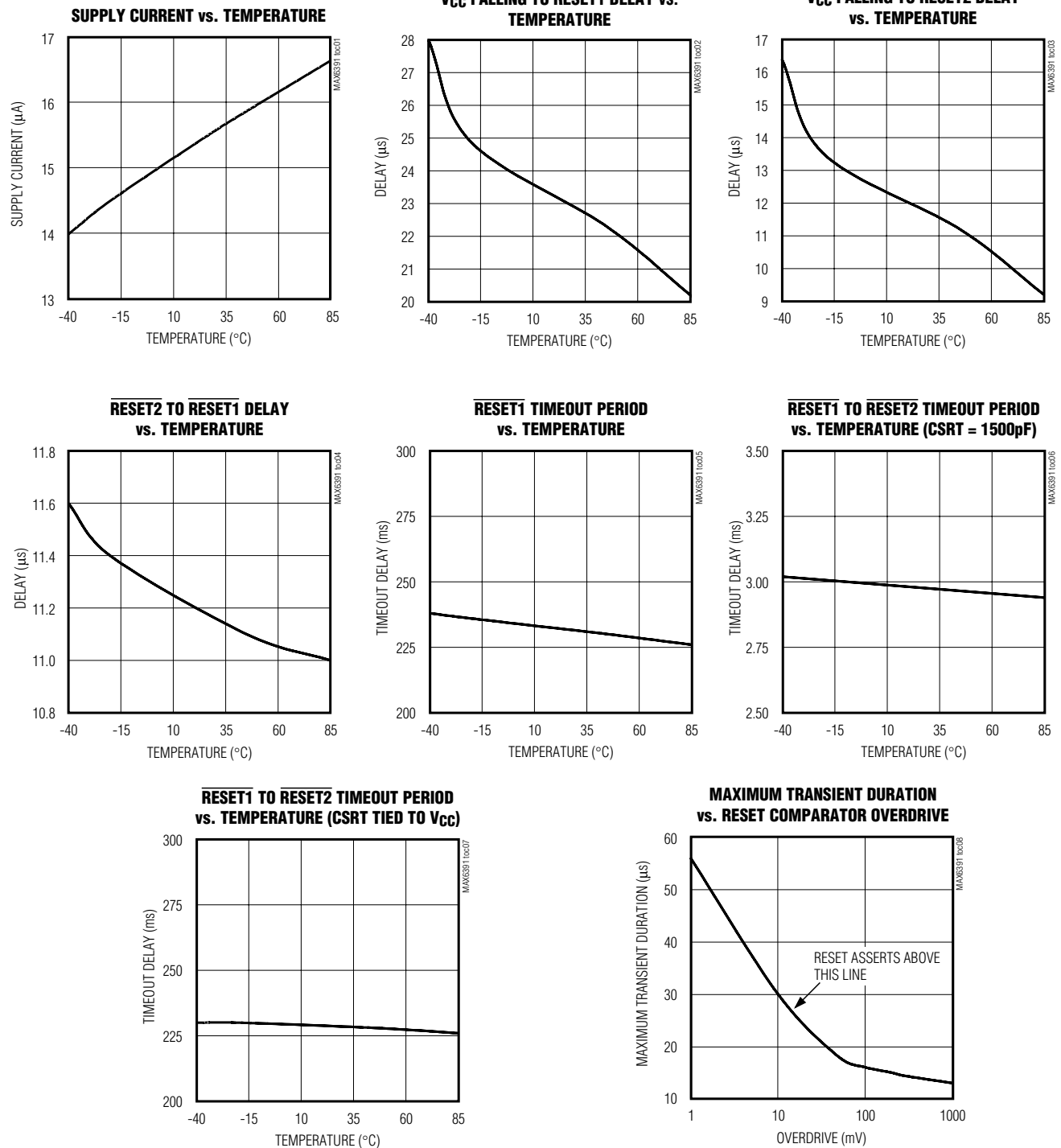
**Note 2:** RESET2 asserts before RESET1 when  $V_{CC}$  goes below the threshold for all supply voltage and temperature ranges.

**Note 3:** CSRT must be connected to either  $V_{CC}$  (for fixed RESET2 timeout period) or an external capacitor (for user-adjustable RESET2 timeout period).

# Dual-Voltage $\mu$ P Supervisory Circuits with Sequenced Reset Outputs

## Typical Operating Characteristics

( $V_{CC} = +5V$ ,  $T_A = +25^\circ C$ , unless otherwise noted.)



# Dual-Voltage $\mu$ P Supervisory Circuits with Sequenced Reset Outputs

## Pin Description

MAX6391/MAX6392

| PIN     |         | NAME                       | FUNCTION                                                                                                                                                                                                                                                                                                                                                                                                           |
|---------|---------|----------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| MAX6391 | MAX6392 |                            |                                                                                                                                                                                                                                                                                                                                                                                                                    |
| 1       | 1       | RESET IN2                  | Input Voltage for $\overline{\text{RESET2}}$ Monitor. High-impedance input for internal reset comparator. Connect this pin to an external resistive-divider network to set the reset threshold voltage.                                                                                                                                                                                                            |
| 2       | 2       | V <sub>CC</sub>            | Supply Voltage and Input Voltage for Primary Supply Monitor                                                                                                                                                                                                                                                                                                                                                        |
| 3       | 3       | CSRT                       | $\overline{\text{RESET2}}$ Delay Set Capacitor. Connect to V <sub>CC</sub> for a fixed 140ms (min) timeout period or to an external capacitor for a user-adjustable timeout period after V <sub>CC</sub> exceeds its minimum threshold.                                                                                                                                                                            |
| 4       | 4       | GND                        | Ground                                                                                                                                                                                                                                                                                                                                                                                                             |
| 5       | 5       | $\overline{\text{RESET2}}$ | Secondary Reset Output, Open-Drain, Active-Low. $\overline{\text{RESET2}}$ changes from high to low when either V <sub>CC</sub> or RESET IN2 drop below their thresholds. $\overline{\text{RESET2}}$ remains low for a user-adjustable timeout period (see CSRT) or a fixed 140ms (min) after V <sub>CC</sub> and RESET IN2 meet their minimum thresholds.                                                         |
| 6       | 6       | R2                         | 47k $\Omega$ Internal Pullup Resistor for $\overline{\text{RESET2}}$ . Connect to external voltage for $\overline{\text{RESET2}}$ high pullup.                                                                                                                                                                                                                                                                     |
| 7       | 7       | $\overline{\text{RESET1}}$ | Primary Reset Output, Open-Drain (MAX6391) or Push-Pull (MAX6392), Active-Low. $\overline{\text{RESET1}}$ changes from HIGH to LOW when the V <sub>CC</sub> input drops below the selected reset threshold. $\overline{\text{RESET1}}$ remains LOW for the reset timeout period after V <sub>CC</sub> exceeds the minimum threshold.                                                                               |
| 8       | —       | R1                         | 47k $\Omega$ Internal Pullup Resistor for $\overline{\text{RESET1}}$ . Connect to external voltage for $\overline{\text{RESET1}}$ high pullup.                                                                                                                                                                                                                                                                     |
| —       | 8       | $\overline{\text{MR}}$     | Manual Reset, Active-Low, Internal 47k $\Omega$ Pullup to V <sub>CC</sub> . Pull LOW to force a reset. $\overline{\text{RESET1}}$ and $\overline{\text{RESET2}}$ remain asserted as long as $\overline{\text{MR}}$ is LOW and for the $\overline{\text{RESET1}}$ and $\overline{\text{RESET2}}$ timeout periods after $\overline{\text{MR}}$ goes HIGH. Leave unconnected or connect to V <sub>CC</sub> if unused. |

## Detailed Description

Each device includes a pair of voltage monitors with sequenced reset outputs. The first block monitors V<sub>CC</sub> only ( $\overline{\text{RESET1}}$  output is independent of the RESET IN2 monitor). It asserts a reset signal (LOW) whenever V<sub>CC</sub> is below the preset voltage threshold.  $\overline{\text{RESET1}}$  remains asserted for at least 140ms after V<sub>CC</sub> rises above the reset threshold.  $\overline{\text{RESET1}}$  timing is internally set in each device. V<sub>CC</sub> voltage thresholds are available from 1.57V to 4.63V. In all cases V<sub>CC</sub> acts as the master supply (all resets are asserted when V<sub>CC</sub> goes below its selected threshold). The V<sub>CC</sub> input also acts as the device power supply.

The second block monitors both RESET IN2 and V<sub>CC</sub>. It asserts a reset signal (LOW) whenever RESET IN2 is below the 625mV threshold or V<sub>CC</sub> is below its reset threshold.  $\overline{\text{RESET2}}$  remains asserted for a fixed 140ms

(min) or a user-adjustable time period after RESET IN2 rises above the 625mV reset threshold and  $\overline{\text{RESET1}}$  is deasserted. Resets are guaranteed valid for V<sub>CC</sub> down to 1V.

The timing diagram in Figure 2 shows the reset timing characteristics of the MAX6391/MAX6392. As shown in Figure 2,  $\overline{\text{RESET1}}$  deasserts 140ms (min) ( $t_{RP1}$ ) after V<sub>CC</sub> exceeds the reset threshold.  $\overline{\text{RESET2}}$  deasserts  $t_{RP2}$  (140ms minimum or a user-adjustable timeout period) after RESET IN2 exceeds 625mV and  $\overline{\text{RESET1}}$  is deasserted. When RESET IN2 drops below 625mV while V<sub>CC</sub> is above the reset threshold,  $\overline{\text{RESET2}}$  asserts within 10 $\mu$ s typ.  $\overline{\text{RESET1}}$  is unaffected when this happens. When V<sub>CC</sub> falls below V<sub>TH1</sub>,  $\overline{\text{RESET2}}$  always asserts before  $\overline{\text{RESET1}}$  ( $t_{RD2} < t_{RD1}$ ).

# Dual-Voltage $\mu$ P Supervisory Circuits with Sequenced Reset Outputs

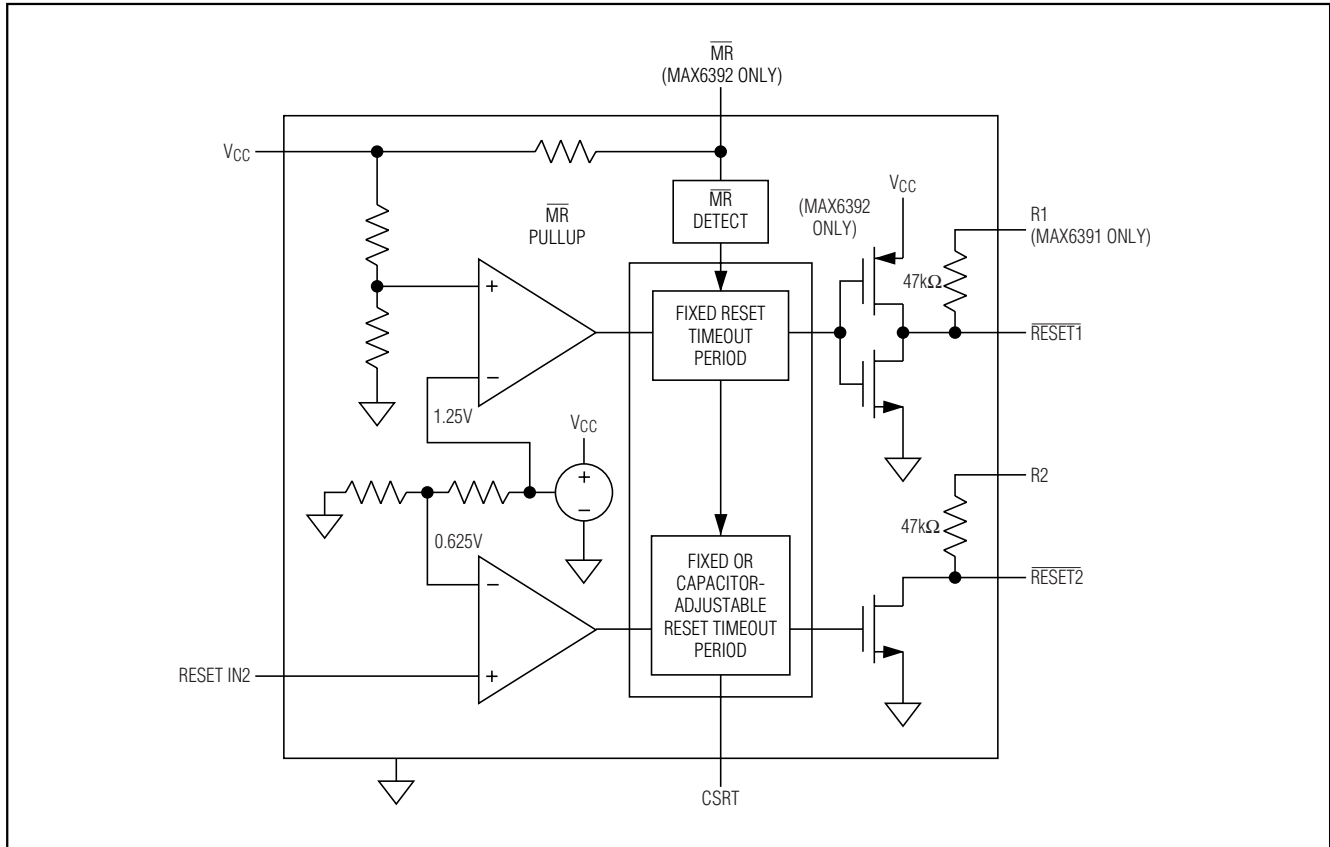


Figure 1. Functional Diagram

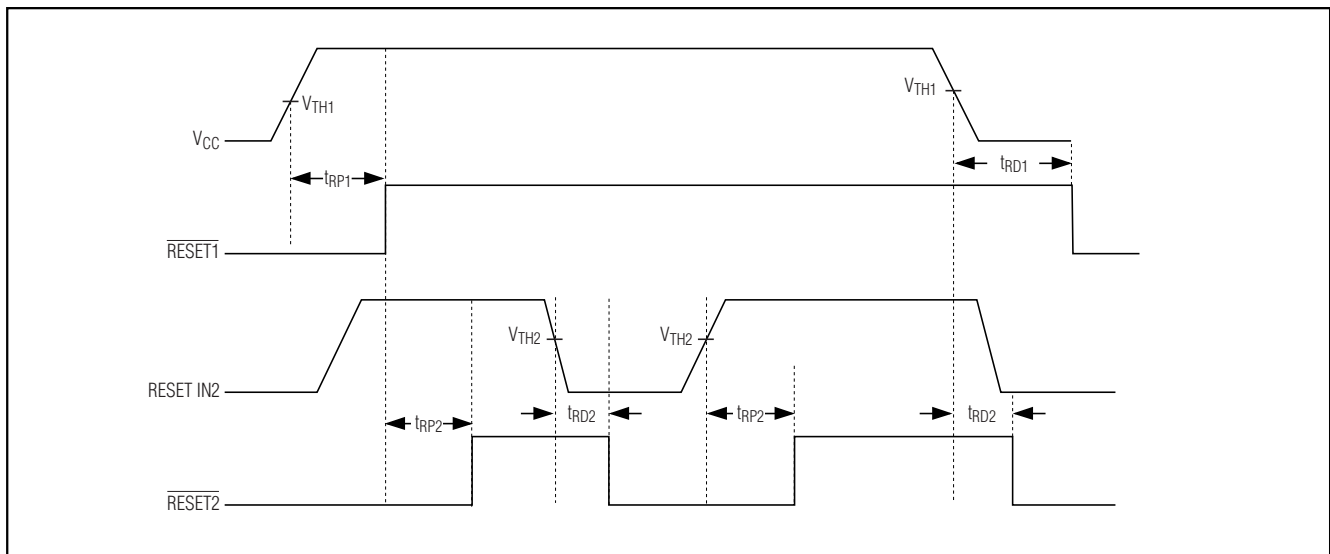


Figure 2. Timing Diagram

# Dual-Voltage $\mu$ P Supervisory Circuits with Sequenced Reset Outputs

## Selector Guide

| PART NUMBER         | NOMINAL THRESHOLD (V) | TOP MARK |
|---------------------|-----------------------|----------|
| MAX6391KA <b>46</b> | 4.63                  | AAHJ     |
| MAX6391KA44         | 4.38                  | AAHK     |
| MAX6391KA31         | 3.08                  | AAHL     |
| MAX6391KA <b>29</b> | 2.93                  | AAHM     |
| MAX6391KA26         | 2.63                  | AAHN     |
| MAX6391KA <b>23</b> | 2.32                  | AAHO     |
| MAX6391KA22         | 2.19                  | AAHP     |
| MAX6391KA17         | 1.67                  | AAHQ     |
| MAX6391KA <b>16</b> | 1.58                  | AAHR     |
| MAX6392KA <b>46</b> | 4.63                  | AAHS     |
| MAX6392KA44         | 4.38                  | AAHT     |
| MAX6392KA31         | 3.08                  | AAHU     |
| MAX6392KA <b>29</b> | 2.93                  | AAHV     |
| MAX6392KA26         | 2.63                  | AAHW     |
| MAX6392KA <b>23</b> | 2.32                  | AAHX     |
| MAX6392KA22         | 2.19                  | AAHY     |
| MAX6392KA17         | 1.67                  | AAHZ     |
| MAX6392KA <b>16</b> | 1.58                  | AAIA     |

Standard versions in bold face. Samples are typically available for standard versions. Contact factory for availability.

## Applications Information

### Selecting the Reset Timeout Capacitor

The  $\overline{\text{RESET2}}$  delay may be adjusted by the user with an external capacitor connected from the CSRT pin to ground. The MAX6391 includes a 600nA current source that is switched to CCSRT to create a voltage ramp. The voltage ramp is compared to the internal 1.25V reference to set the  $\overline{\text{RESET2}}$  delay period. The period is calculated by:

$$\Delta t = C \times \Delta V / I$$

where  $\Delta V = 1.25\text{V}$ ,  $I = 600\text{nA}$ , and  $C$  is the external capacitor.

Simplifying,

$$t_{\text{RP}} = 2.08 \times 10^6 \text{ s} / F \times \text{CCSRT}$$

$$\text{For CCSRT} = 1500\text{pF}, t_{\text{RP}} = 3.1\text{ms}$$

A fixed internal 140ms (min) reset delay time for  $\overline{\text{RESET2}}$  may be chosen by connecting the CSRT pin to  $V_{\text{CC}}$ . The  $V_{\text{CC}}$  to CSRT connection disables the voltage ramp and enables a separate fixed delay counter

chain. The MAX6391 internally determines the CSRT connection and provides the proper timing setup.

In all cases,  $\overline{\text{RESET IN2}}$  acts as the slave supply.  $V_{\text{CC}}$  can assert the  $\overline{\text{RESET2}}$  output but  $\overline{\text{RESET IN2}}$  will have no effect on the  $\overline{\text{RESET1}}$  output.

### Monitoring Voltages Other Than $V_{\text{CC}}$

An external resistive-divider network is required at  $\overline{\text{RESET IN2}}$  for most applications. The divider resistors,  $R3$  and  $R4$ , may be calculated by the following formula:

$$V_{\text{RST}} = V_{\text{TH2}} \times (R3 + R4) / R4$$

where  $V_{\text{TH2}} = 625\text{mV}$  (internal reference voltage) and  $V_{\text{RST}}$  is the desired reset threshold voltage.  $R4$  may be set to a conveniently high value (500k $\Omega$  for example, to minimize current consumption) and the equation may be solved for  $R3$  by:

$$R3 = R4 \times (V_{\text{RST}} / V_{\text{TH2}} - 1)$$

For single-supply operations requiring two reset outputs ( $\overline{\text{RESET1}}$  before  $\overline{\text{RESET2}}$ ), connect  $\overline{\text{RESET IN2}}$  directly to  $V_{\text{CC}}$  and adjust  $\overline{\text{RESET2}}$  timeout delay with CCSRT as desired.

### Pullup Resistors

The MAX6391 includes open-drain outputs for both  $\overline{\text{RESET1}}$  and  $\overline{\text{RESET2}}$ . Two internal resistors,  $R1$  and  $R2$ , of 47k $\Omega$  each are provided with internal connections to  $\overline{\text{RESET1}}$  and  $\overline{\text{RESET2}}$ . These resistors may be connected to the appropriate external voltage for independent  $V_{\text{OH}}$  drive with no additional component requirements.

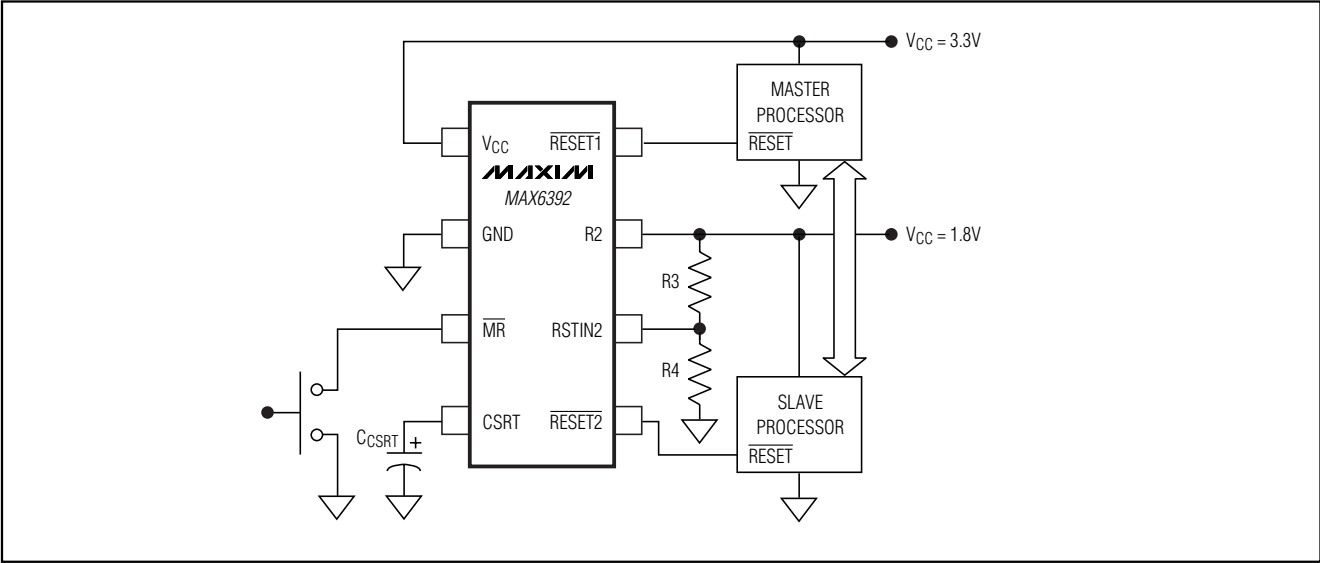
The MAX6392 includes a manual reset option,  $\overline{\text{MR}}$ , that replaces the  $R1$  pullup resistor. The active-low manual reset input forces both  $\overline{\text{RESET1}}$  and  $\overline{\text{RESET2}}$  low.  $\overline{\text{RESET2}}$  is driven active before  $\overline{\text{RESET1}}$  in all cases (10 $\mu\text{s}$  typ). The resets follow standard reset timing specifications after the manual reset is released. The manual reset is internally pulled up to  $V_{\text{CC}}$  through a 47k $\Omega$  resistor.

### Negative-Going $V_{\text{CC}}$ Transients

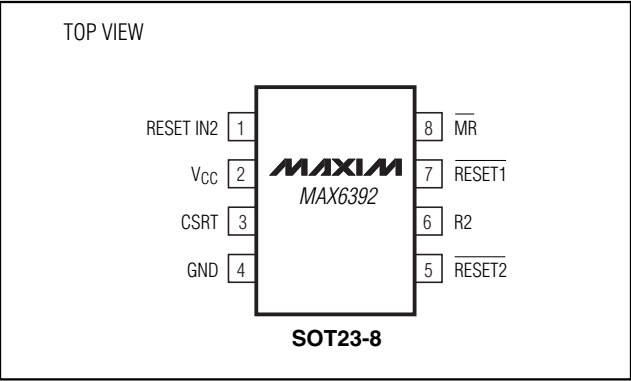
In addition to issuing a reset to the  $\mu\text{P}$  during power-up, power-down, and brownout conditions, these devices are relatively immune to short-duration, negative-going  $V_{\text{CC}}$  or  $\overline{\text{RESET IN2}}$  transients (glitches). The *Typical Operating Characteristics* show the Maximum Transient Duration vs. Reset Comparator Overdrive graph. The graph shows the maximum pulse width that a negative-going  $V_{\text{CC}}$  transient may typically have without issuing a reset signal. As the amplitude of the transient increases, the maximum allowable pulse width decreases.

# Dual-Voltage $\mu$ P Supervisory Circuits with Sequenced Reset Outputs

Typical Operating Circuit



## Pin Configurations (continued)



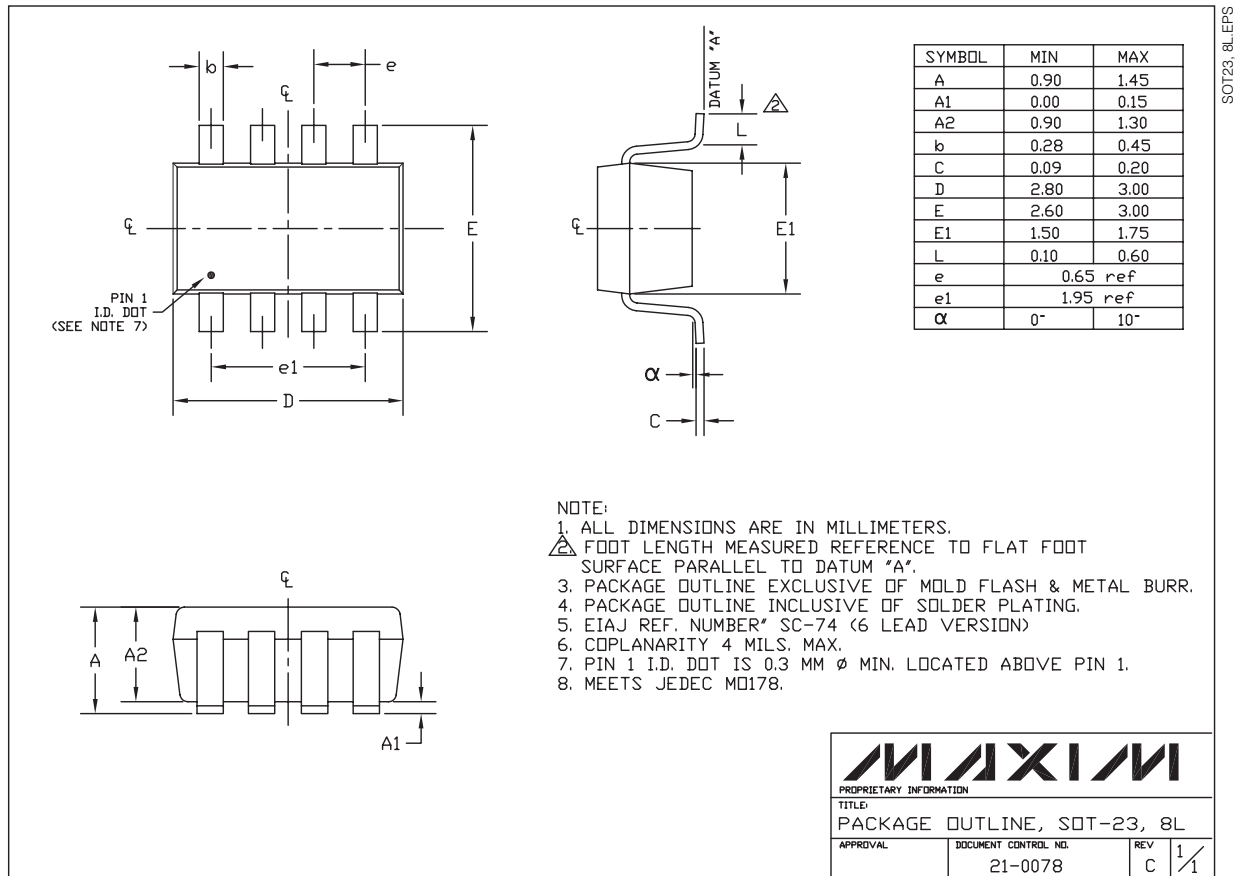
## Chip Information

TRANSISTOR COUNT: 810  
PROCESS: BiCMOS

# Dual-Voltage $\mu$ P Supervisory Circuits with Sequenced Reset Outputs

## Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to [www.maxim-ic.com/packages](http://www.maxim-ic.com/packages).)



SOT23, 8LEPS

MAX6391/MAX6392

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