19-3776; Rev 0; 7/05

Overvoltage-Protection Controller with Internal Disconnect Switch

General Description

The MAX4880 is an overvoltage-protection controller with an internal current-limited switch that can be configured as a low-cost battery charger. When the input voltage exceeds the overvoltage trip level (5.7V), or drops below the undervoltage-lockout level (4.2V), the MAX4880 turns off the external n-channel MOSFET and asserts an undervoltage/overvoltage flag indicator ($\overline{FLAGV}$) low to notify the processor.

The MAX4880 internal current-limited switch limits the charge current flowing to the battery to 525mA. The switch opens when the battery voltage reaches its full-charged state (4.2V), and a flag ($\overline{BAT\_OK}$) asserts to notify the processor. The MAX4880 includes a switch-control input (CB) to turn off the internal current-limited switch, regardless of the battery voltage.

The MAX4880 also features a built-in startup delay that allows the adapter voltage to settle down before turning on the MOSFET. Other features include 15kV ESD protection for the input and a shutdown function ($\overline{EN}$) to turn off the external n-channel MOSFET.

The MAX4880 is available in a space-saving 10-pin TDFN package and is specified for operation over the extended -40°C to +85°C temperature range.

Applications

Cell Phones

Digital Still Cameras

PDAs and Palmtop Devices

MP3 Players

Features

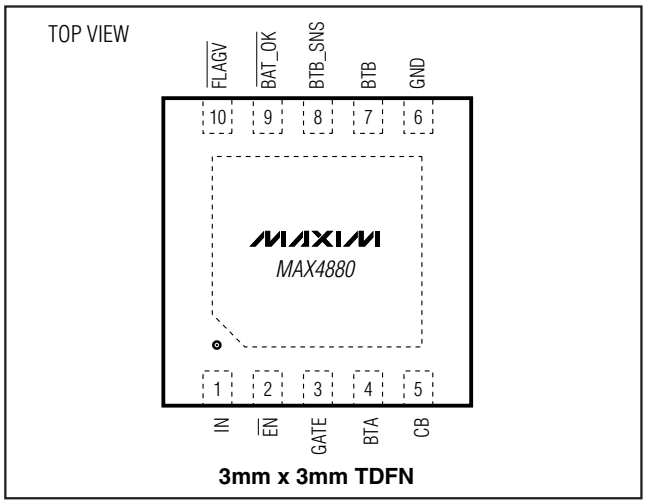
- **Overvoltage Protection Up to 28V**
- **Preset 5.6V Overvoltage Trip Level**
- **Internal 525mA Current-Limited Switch**
- **±1.2% Accurate Battery Disconnect (4.2V)**
- **Drives Low-Cost n-Channel MOSFET**
- **Internal 50ms Startup Delay**
- **Overvoltage/Undervoltage-Fault $\overline{FLAGV}$ Indicator**
- **Battery-Voltage-Trip $\overline{BAT\_OK}$ Indicator**
- **Undervoltage Lockout**
- **Thermal Shutdown Protection**
- **Tiny 10-Pin TDFN Package**

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE	TOP MARK
MAX4880ETB	-40°C to +85°C	10 TDFN-EP*	APJ

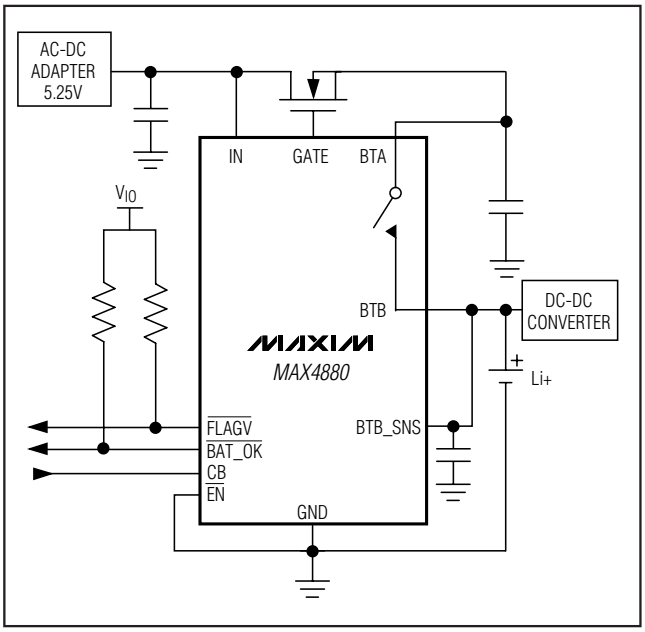
** EP = Exposed Pad*

Pin Configuration



3mm x 3mm TDFN

Typical Operating Circuit



Overvoltage-Protection Controller with Internal Disconnect Switch

ABSOLUTE MAXIMUM RATINGS

(All voltages referenced to GND.)
IN .....-0.3V to +30V
GATE .....-0.3V to +12V
$\overline{EN}$, CB, $\overline{FLAGV}$, $\overline{BAT\_OK}$, BTA, BTB, BTB_SNS .....-0.3V to +6V
Continuous Power Dissipation (T_A = +70°C)
10-Pin TDFN (derate 18.5mW/°C above +70°C) ...1481.5mW

Operating Temperature Range .....-40°C to +85°C
Junction Temperature ..... +150°C
Storage Temperature Range .....-65°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{IN} = 5V, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
INPUT VOLTAGE (IN)						
Input Voltage Range	V_{IN}		1.2		28.0	V
Overvoltage Trip Level	OVLO	V_{IN} rising	5.5	5.6	5.7	V
Overvoltage-Trip-Level Hysteresis				50		mV
Undervoltage-Lockout Threshold	UVLO	V_{IN} falling	4.2	4.35	4.5	V
Undervoltage-Lockout Hysteresis				50		mV
Supply Current	I_{IN} + I_{BTA}	No load, V_{IN} = 5.4V, $V_{\overline{EN}}$ = 0 or 5.5V, V_{CB} = 0 or V_{IN}		240	380	µA
INTERNAL SWITCH						
BTA Input Range	V_{BTA}		2.8		5.7	V
BTA Undervoltage Lockout	BTA_{UVLO}	Falling edge	2.4		2.7	V
BTA-Undervoltage-Lockout Hysteresis				50		mV
BTB-Switch-Disconnect Trip Level	BTB_{TRIP}		4.10		4.20	V
BTB-Switch-Disconnect Hysteresis				200		mV
Switch-Forward Current Limit	I_{FWD}		450	525	600	mA
Switch-Reverse Current Limit	I_{REV}	T_A = +25°C			600	mA
					650	
Voltage Drop (V_{BTA} – V_{BTB})		I_L = 400mA			110	mV
BTB Off Current	$I_{BTB-OFF}$	$V_{\overline{EN}}$ = 0 (V_{CB} = 0, or V_{IN} < V_{UVLO} and V_{BTA} = 0)			1	µA
GATE						
GATE Voltage	V_{GATE}	I_{GATE} sourcing 1µA , V_{IN} = 5V	9		10	V
GATE Pulldown Current	I_{PD}	V_{IN} > V_{OVLO}, V_{GATE} = 5V		60		mA
TIMING						
GATE Startup Delay	t_{START}	V_{IN} > V_{UVLO}, V_{GATE} > 0.3V (Figure 1)	20	50	80	ms
$\overline{FLAGV}$ Delay Time	t_{DELAY}	V_{GATE} = 0.3V, $V_{\overline{FLAGV}}$ = 2.4V (Figure 1)	20	50	80	ms
GATE Turn-On Time	t_{GON}	V_{GATE} = 0.3V to 8V, C_{GATE} = 1500pF (Figure 1)		7		ms
GATE Turn-Off Time	t_{GOFF}	V_{IN} increasing from 5V to 8V at 3V/µs, V_{GATE} = 0.3V, C_{GATE} = 1500pF (Figure 2)		6	20	µs

ELECTRICAL CHARACTERISTICS (continued)

(V_{IN} = 5V, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

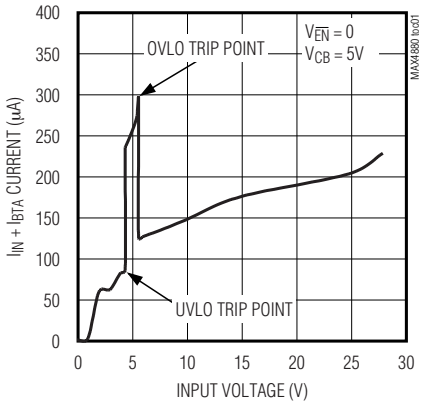
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
$\overline{FLAGV}$ Assertion Delay	$t_{\overline{FLAGV}}$	V_{IN} increasing from 5V to 8V at 3V/µs, $V_{\overline{FLAGV}}$ = 0.4V (Figure 2)		5.8		µs
Initial Overvoltage Fault Delay	t_{OVP}	V_{IN} increasing from 0 to 8V, I_{GATE} = 80% of I_{PD} (Figure 3)		100		ns
Disable Time	t_{DIS}	$V_{\overline{EN}}$ = 2.4V, V_{GATE} = 0.3V (Figure 4)		580		ns
$\overline{EN}$, CB INPUTS						
Input-High Voltage	V_{IH}		1.4			V
Input-Low Voltage	V_{IL}				0.5	V
Input Leakage					1	µA
$\overline{FLAGV}$, $\overline{BAT\_OK}$ OUTPUTS						
Output Voltage Low	V_{OL}	I_{SINK} = 1mA, $\overline{FLAGV}$, $\overline{BAT\_OK}$ assert			0.4	V
Leakage Current		$V_{\overline{BAT\_OK}}$ = $V_{\overline{FLAGV}}$ = 5.5V			1	µA
THERMAL PROTECTION						
Thermal Shutdown				+150		°C
Thermal Hysteresis				40		°C

Note 1: All devices are 100% tested at T_A = +25°C. Electrical limits over the full temperature range are guaranteed by design.

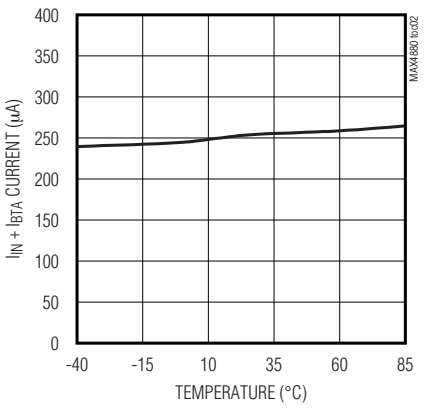
Typical Operating Characteristics

(V_{IN} = 5V, T_A = +25°C, otherwise noted.)

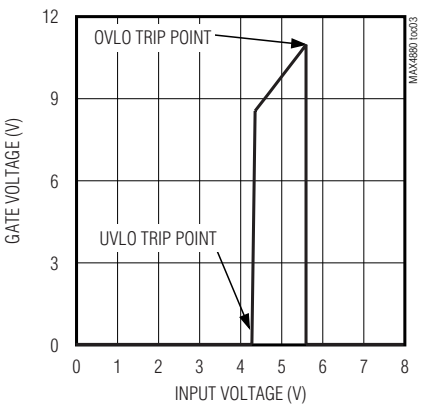
I_{IN} + I_{BTA} CURRENT vs. INPUT VOLTAGE



I_{IN} + I_{BTA} CURRENT vs. TEMPERATURE



GATE VOLTAGE vs. INPUT VOLTAGE

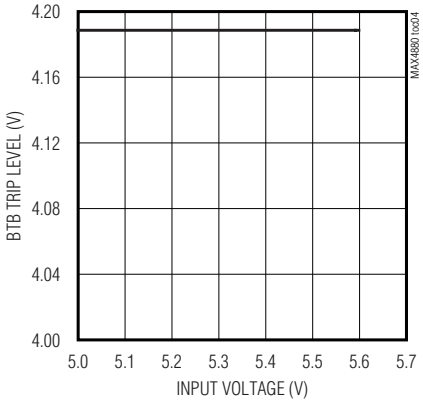


Overvoltage-Protection Controller with Internal Disconnect Switch

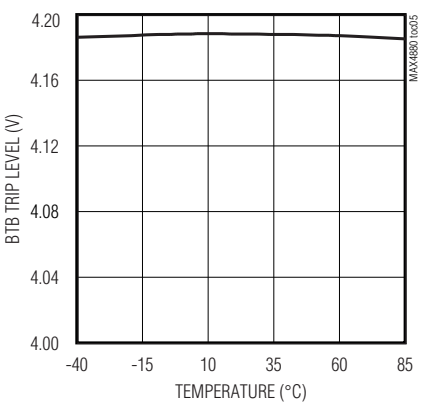
Typical Operating Characteristics (continued)

(V_{IN} = 5V, T_A = +25°C, otherwise noted.)

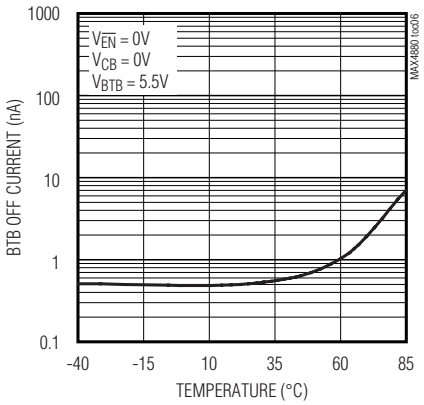
BTB TRIP LEVEL vs. INPUT VOLTAGE



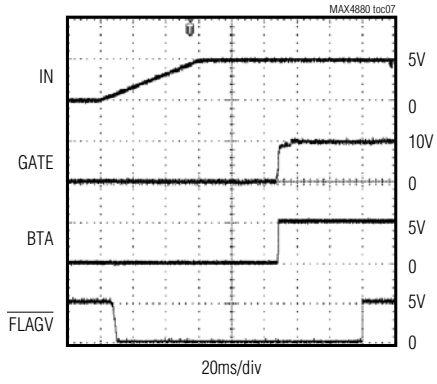
BTB TRIP LEVEL vs. TEMPERATURE



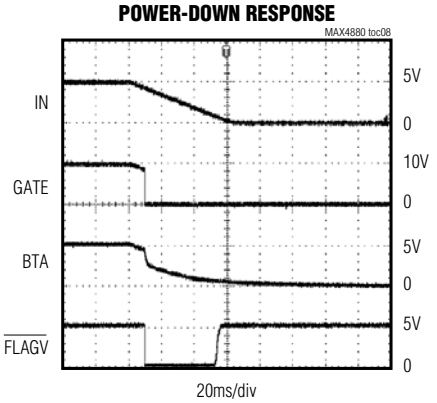
BTB OFF CURRENT vs. TEMPERATURE



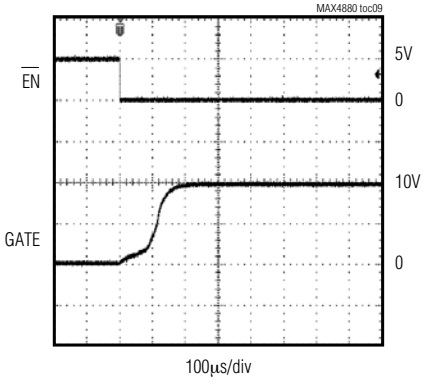
POWER-UP RESPONSE



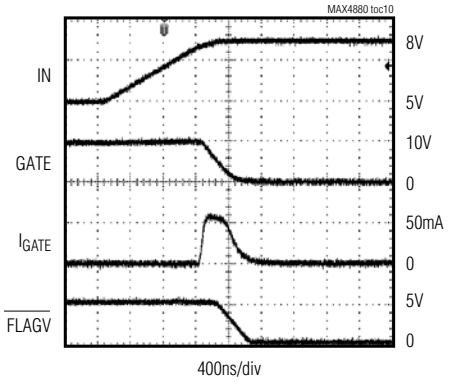
POWER-DOWN RESPONSE



$\overline{EN}$ vs. GATE



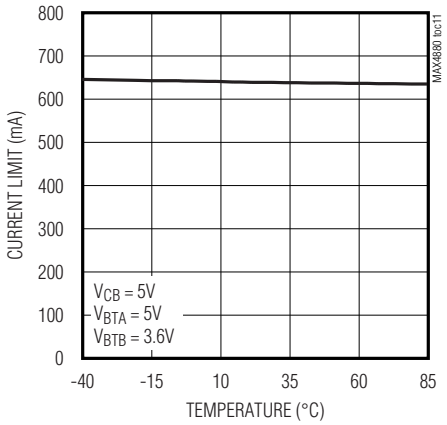
OVERVOLTAGE RESPONSE



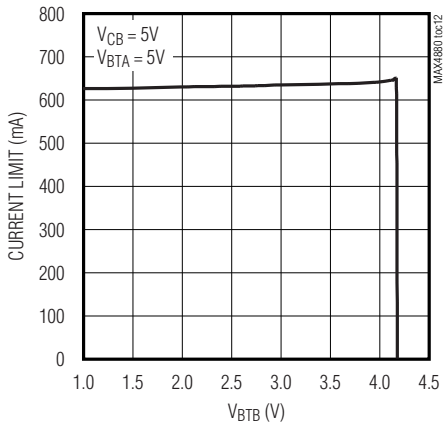
Typical Operating Characteristics (continued)

(V_{IN} = 5V, TA = +25°C, otherwise noted.)

CURRENT LIMIT vs. TEMPERATURE



CURRENT LIMIT vs. V_{BTB}



Pin Description

PIN	NAME	FUNCTION
1	IN	Input. IN is the power input for the overvoltage (OVP) charge pump. Bypass IN to GND with a 1µF or larger capacitor to achieve 15kV ESD protection.
2	$\overline{EN}$	Active-Low Enable Input. Driving $\overline{EN}$ high turns off the external MOSFET. Pulling $\overline{EN}$ low activates the overvoltage-protection circuitry and turns on the external MOSFET.
3	GATE	Gate-Drive Output. GATE is the output of an on-chip OVP charge pump. When $V_{UVLO} < V_{IN} < V_{OVLO}$, GATE is driven high to turn on the external n-channel MOSFET. When $V_{IN\ (MIN)} < V_{IN} < V_{UVLO}$ or $V_{IN} > V_{OVLO}$, GATE is driven low to turn off the external n-channel MOSFET.
4	BTA	Input Terminal for the Internal-Current-Limited Switch. Connect BTA to the source of the external n-channel MOSFET. BTA is the power input for the entire device (except the OVP charge pump). Bypass BTA to GND with a 0.1µF capacitor as close to the device as possible.
5	CB	Control Input for the Internal-Current-Limited Switch. Drive CB high to leave the internal switch control for the internal logic. The internal switch turns on and off depending on the battery voltage level. The internal switch turns off when the battery voltage reaches the BTB trip level (4.2V), and turns back on when the battery falls by 200mV. Driving CB low turns off the internal switch regardless of the battery voltage.
6	GND	Ground
7	BTB	Output Terminal for the Internal-Current-Limited Switch. When the BTB voltage exceeds the trip level (4.2V), the internal switch opens. The switch closes only when the BTB voltage drops 200mV below the trip level.
8	BTB_SNS	Battery-Voltage-Sensing Input. BTB_SNS must be connected to BTB for proper operation. Bypass BTB_SNS to GND with a 0.1µF capacitor as close to the device as possible.
9	$\overline{BAT\_OK}$	Active-Low, Open-Drain, Battery-Voltage-Limit Flag Output. $\overline{BAT\_OK}$ asserts low when the voltage on BTB exceeds the BTB trip level (4.2V). $\overline{BAT\_OK}$ is disabled when $\overline{EN}$ goes high.

Overvoltage-Protection Controller with Internal Disconnect Switch

Pin Description (continued)

PIN	NAME	FUNCTION
10	$\overline{FLAGV}$	Active-Low, Open-Drain-Fault Flag Output. $\overline{FLAGV}$ goes low when either an overvoltage or undervoltage fault occurs at IN. $\overline{FLAGV}$ is disabled when $\overline{EN}$ goes high. During startup, $\overline{FLAGV}$ has a delay of 50ms after V_{GATE} > 0.3V, before being initially driven high.
—	EP	Exposed Pad. EP is internally connected to GND. Do not use EP as the only electrical ground connection.

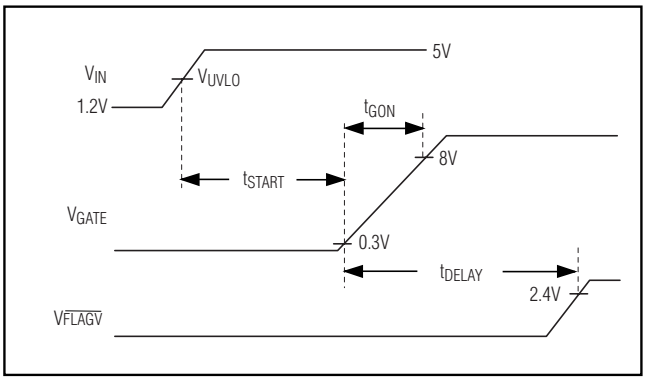


Figure 1. Startup Timing Diagram

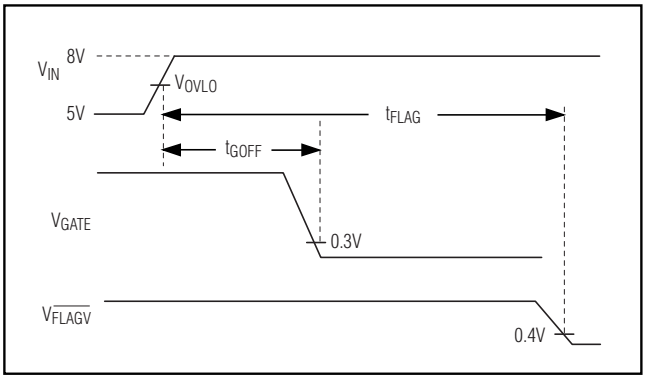


Figure 2. Overvoltage Fault Timing Diagram

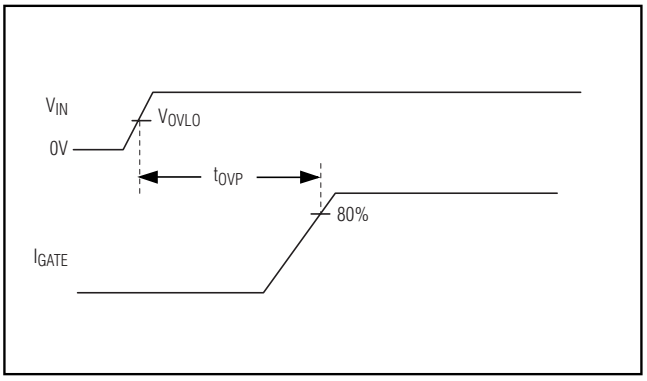


Figure 3. Power-Up Overvoltage Timing Diagram

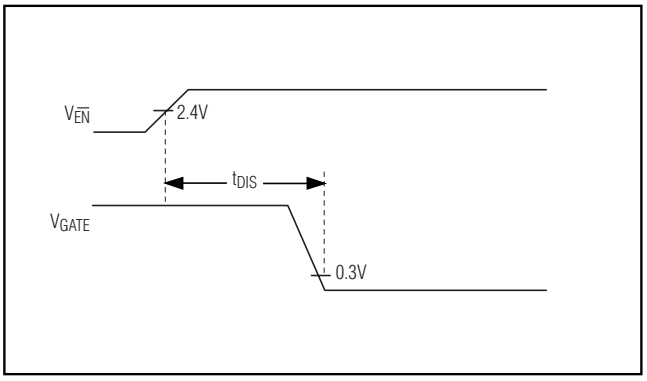


Figure 4. Disable Timing Diagram

Overvoltage-Protection Controller with Internal Disconnect Switch

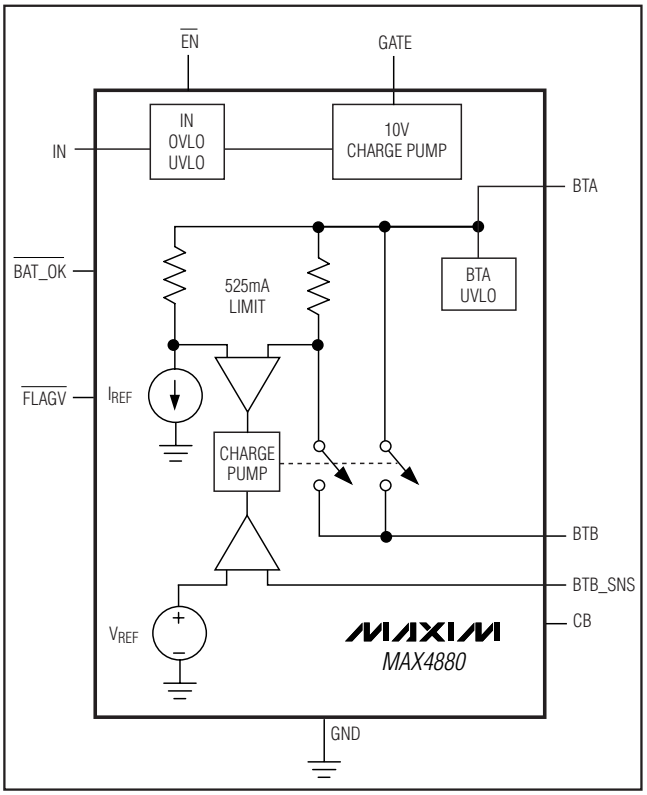


Figure 5. Functional Diagram

Detailed Description

The MAX4880 provides up to 28V overvoltage protection for low-voltage systems. When the input voltage at IN exceeds the overvoltage trip level (OVLO), the MAX4880 turns off a low-cost, external n-channel MOSFET to prevent damage to the protected components and issues an overvoltage fault flag.

When the correct adapter is plugged in, the n-channel MOSFET is turned on. The output of the MOSFET is then connected to the internal current-limit switch that provides the charge-current path to the battery. When the battery reaches the trip voltage (4.2V), the internal switch turns off and $\overline{BAT\_OK}$ asserts low, indicating that the battery has reached its full charged state. The internal switch turns back on only when the battery voltage drops by more than 200mV.

IN Overvoltage Lockout (OVLO)

The MAX4880 has a 5.6V typical overvoltage threshold (OVLO). When V_{IN} is higher than V_{OVLO}, GATE goes low to turn off the external n-channel MOSFET. An overvoltage $\overline{FLAGV}$ is asserted low to notify the processor of the fault condition.

IN Undervoltage Lockout (UVLO)

The MAX4880 includes a fixed 4.35V typical undervoltage-lockout level (UVLO). When V_{IN} is below the V_{UVLO} ($1.2V \le V_{IN} \le 4.35V$), GATE goes low to turn off the external n-channel MOSFET. In addition, the driver for the internal switch (BTA-BTB) is also turned off; therefore, this switch is open. This ensures the reverse current, drained from the battery, is less than 1µA when the adapter is not present.

Fault Flag Output ($\overline{FLAGV}$)

The $\overline{FLAGV}$ output signals the host system that there is a fault with the input voltage. $\overline{FLAGV}$ asserts low in response to either an overvoltage or an undervoltage fault. $\overline{FLAGV}$ stays low for 50ms after GATE turns on, before deasserting high.

$\overline{FLAGV}$ is an open-drain, active-low output. Connect a pullup resistor from $\overline{FLAGV}$ to the logic I/O voltage of the host system or to any voltage source up to 6V. $\overline{FLAGV}$ is invalid when driving $\overline{EN}$ high.

Battery-Voltage-Limit Flag Output ($\overline{BAT\_OK}$)

The MAX4880 includes a battery-voltage-limit flag output ($\overline{BAT\_OK}$). $\overline{BAT\_OK}$ asserts low to indicate the voltage on BTB exceeds the BTB trip level of 4.2V. $\overline{BAT\_OK}$ deasserts high when the voltage on BTB falls by the BTB hysteresis voltage of more than 200mV.

$\overline{BAT\_OK}$ is an open-drain, active-low output. Connect a pullup resistor from $\overline{BAT\_OK}$ to the logic I/O voltage of the host system, or to any voltage source up to 6V. $\overline{BAT\_OK}$ is invalid when driving $\overline{EN}$ high.

$\overline{EN}$ Input

The MAX4880 features an active-low enable input ($\overline{EN}$). Drive $\overline{EN}$ low or connect to ground for normal operation. Drive $\overline{EN}$ high to force the external n-channel MOSFET off, disabling $\overline{FLAGV}$ and $\overline{BAT\_OK}$.

Internal Current Limit (BTA to BTB)

The internal switch from BTA to BTB has a preset current-limit of 525mA (typ). If the load current from BTA to BTB reaches this current limit, the switch operates in the continuous mode, limiting the load current to the preset value.

The switch remains in the current-limit condition until the battery voltage on BTB exceeds 4.2V, or until the control bit CB is driven low to open the switch.

Internal Switch Control Input (CB)

The CB input controls the internal switch. When CB is high, the on/off state of the internal switch depends on the battery voltage level. The internal switch turns off when the battery voltage reaches the BTB trip level,

Overvoltage-Protection Controller with Internal Disconnect Switch

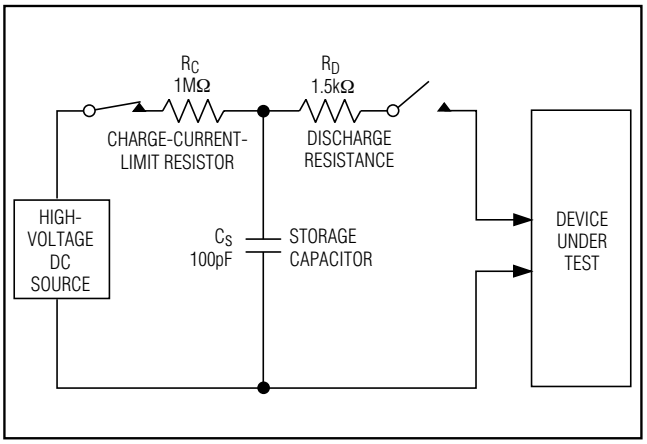


Figure 6. Human-Body ESD Test Model

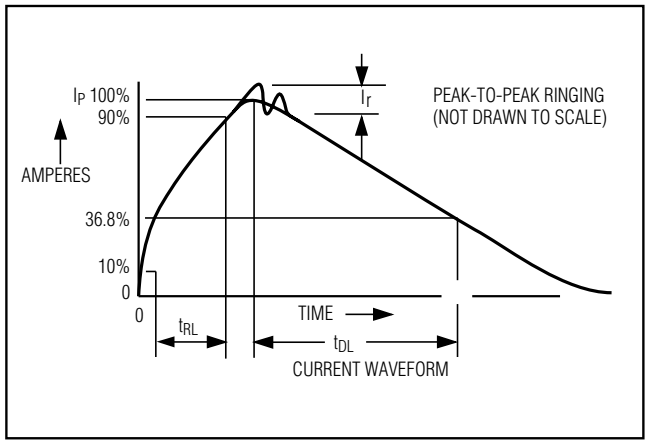


Figure 7. Human-Body-Model Current Waveform

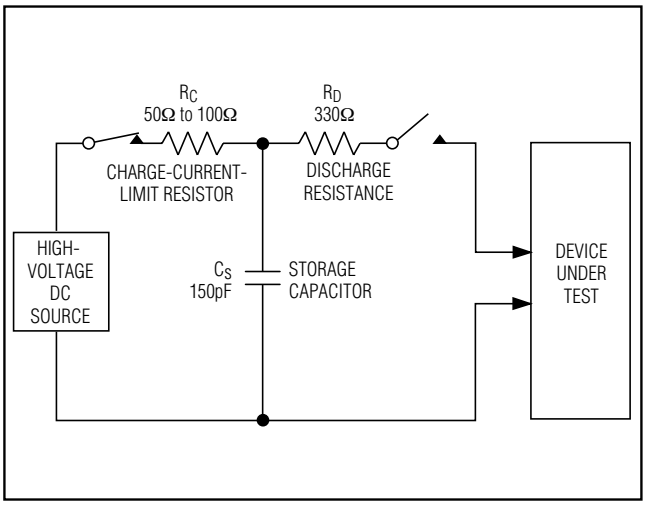


Figure 8. IEC 61000-4-2 ESD Test Model

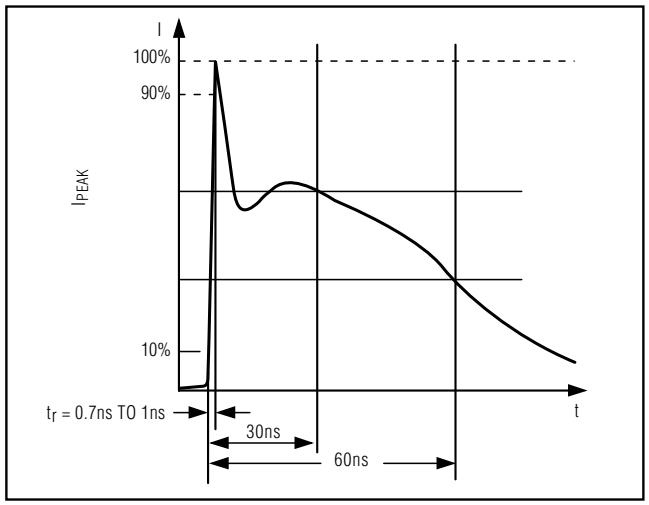


Figure 9. IEC 61000-4-2 ESD Generator Current

and turns back on when the battery falls below the BTB trip level minus BTB hysteresis. Drive CB low to turn off the internal switch, regardless of the battery voltage. This control bit can be used to provide additional top-off charge for the battery. When the CB pin is cycled, the internal battery switch is turned on and off. This effectively provides an average current that is lower than the full-charge current.

GATE Driver

An on-chip charge pump drives the GATE voltage to approximately twice V_{IN}, allowing the use of a low-cost, n-channel MOSFET (Figure 5). The actual GATE output voltage tracks approximately 2 x V_{IN}, until V_{IN} exceeds the OVLO trip level, 5.6V (typ). The GATE output voltage, as a function of input voltage, is shown in the *Typical Operating Characteristics*.

Applications Information

MOSFET Selection

The MAX4880 is designed for use with an n-channel MOSFET. MOSFETs with $R_{DS(ON)}$ specified for a V_{GS} of 4.5V are ideal. If the input supply is near the UVLO minimum of 4.2V, consider using a MOSFET specified for a lower V_{GS} voltage. Also, the V_{DS} should be 30V for the MOSFET to withstand the full 28V IN range of the MAX4880. Table 1 shows a selection of MOSFETs appropriate for use with the MAX4880.

IN Bypass Considerations

Bypass IN to GND with a 1µF ceramic capacitor to achieve 15kV ESD-protected input. When the power source has significant inductance due to long lead length, take care to prevent overshoots due to the LC

Table 1. MOSFET Suggestions

PART	CONFIGURATION/ PACKAGE	V_{DS} MAX (V)	R_{ON} AT 4.5V (mΩ)	MANUFACTURER
Si1426DH	Single/SC70-6	30	115	Vishay Siliconix www.vishay.com 402-563-6866
FDG315N	Single/SC70-6	30	160	Fairchild Semiconductor www.fairchildsemi.com 207-775-8100

tank circuit and provide protection if necessary to prevent exceeding the 30V absolute maximum rating on IN.

The MAX4880 provides protection against voltage faults up to 28V, but this does not include negative voltages. If negative voltages are a concern, connect a Schottky diode from IN to GND to clamp negative input voltages.

Exposed Pad

The MAX4880 provides an exposed pad on the bottom of the package. This pad is internally connected to GND. For the best thermal conductivity and higher power dissipation, solder the exposed pad to the ground plane. Do not use the ground-connected pad as the only electrical ground connection or ground return. Use GND (pin 6) as the primary electrical ground connection.

ESD Test Conditions

ESD performance depends on a number of conditions. The MAX4880 is specified for 15kV typical ESD resistance on IN when IN is bypassed to ground with a 1µF low-ESR ceramic capacitor. Contact Maxim for a reliability report that documents test setup, methodology, and results.

Human Body Model

Figure 6 shows the Human Body Model, and Figure 7 shows the current waveform it generates when discharged into a low impedance. This model consists of a 100pF capacitor charged to the ESD voltage of interest, which is then discharged into the device through a 1.5kΩ resistor.

IEC 61000-4-2

Since January 1996, all equipment manufactured and/or sold in the European community has been required to meet the stringent IEC 61000-4-2 specification. The IEC 61000-4-2 standard covers ESD testing and performance of finished equipment; it does not specifically refer to integrated circuits. The MAX4880 helps users design equipment that meets Level 3 of IEC 61000-4-2, without additional ESD-protection components.

The main difference between tests done using the Human Body Model and IEC 61000-4-2 is higher peak current in IEC 61000-4-2. Because series resistance is lower in the IEC 61000-4-2 ESD test model (Figure 8), the ESD-withstand voltage measured to this standard is generally lower than that measured using the Human Body Model. Figure 9 shows the current waveform for the ±8kV IEC 61000-4-2 Level 4 ESD Contact-Discharge test. The Air-Gap test involves approaching the device with a charger probe. The Contact-Discharge method connects the probe to the device before the probe is energized.

Chip Information

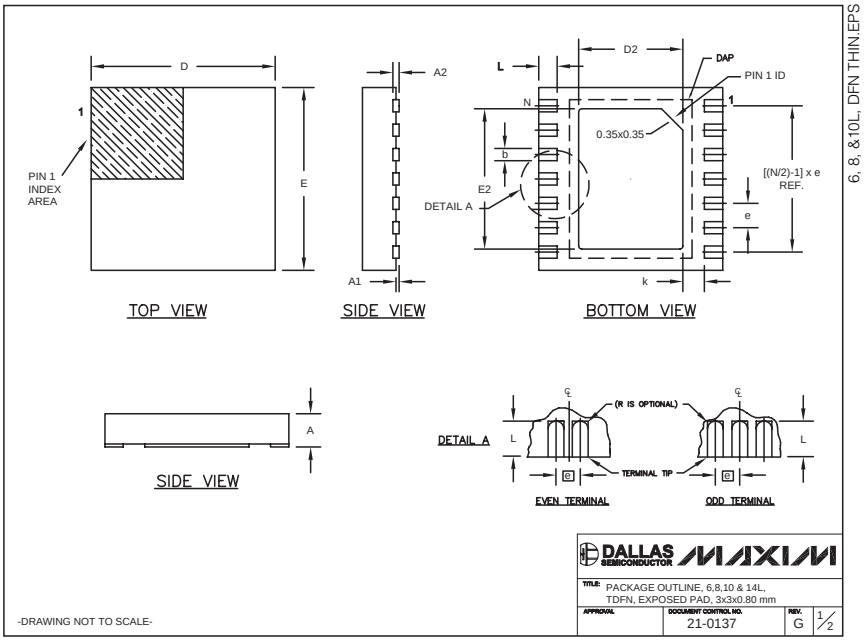
TRANSISTOR COUNT: 2391

PROCESS: BiCMOS

Overvoltage-Protection Controller with Internal Disconnect Switch

Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to **www.maxim-ic.com/packages**.)



COMMON DIMENSIONS		
SYMBOL	MIN.	MAX.
A	0.70	0.80
D	2.90	3.10
E	2.90	3.10
A1	0.00	0.05
L	0.20	0.40
k	0.25 MIN.	
A2	0.20 REF.	

PACKAGE VARIATIONS								
PKG. CODE	N	D2	E2	e	JEDEC SPEC	b	[(N/2)-1] x e	DOWNBONDS ALLOWED
T633-1	6	1.50±0.10	2.30±0.10	0.95 BSC	MO229 / WEEA	0.40±0.05	1.90 REF	NO
T633-2	6	1.50±0.10	2.30±0.10	0.95 BSC	MO229 / WEEA	0.40±0.05	1.90 REF	NO
T833-1	8	1.50±0.10	2.30±0.10	0.65 BSC	MO229 / WEEC	0.30±0.05	1.95 REF	NO
T833-2	8	1.50±0.10	2.30±0.10	0.65 BSC	MO229 / WEEC	0.30±0.05	1.95 REF	NO
T833-3	8	1.50±0.10	2.30±0.10	0.65 BSC	MO229 / WEEC	0.30±0.05	1.95 REF	YES
T1033-1	10	1.50±0.10	2.30±0.10	0.50 BSC	MO229 / WEED-3	0.25±0.05	2.00 REF	NO
T1433-1	14	1.70±0.10	2.30±0.10	0.40 BSC	- - - -	0.20±0.05	2.40 REF	YES
T1433-2	14	1.70±0.10	2.30±0.10	0.40 BSC	- - - -	0.20±0.05	2.40 REF	NO

NOTES:
1. ALL DIMENSIONS ARE IN mm. ANGLES IN DEGREES.
2. COPLANARITY SHALL NOT EXCEED 0.08 mm.
3. WARPAGE SHALL NOT EXCEED 0.10 mm.
4. PACKAGE LENGTH/PACKAGE WIDTH ARE CONSIDERED AS SPECIAL CHARACTERISTIC(S).
5. DRAWING CONFORMS TO JEDEC MO229, EXCEPT DIMENSIONS "D2" AND "E2", AND T1433-1 & T1433-2.
6. "N" IS THE TOTAL NUMBER OF LEADS.
7. NUMBER OF LEADS SHOWN ARE FOR REFERENCE ONLY.

DALLAS SEMICONDUCTOR MAXIM
TITLE: PACKAGE OUTLINE, 6,8,10 & 14L, TDFN, EXPOSED PAD, 3x3x0.80 mm
APPROVAL
DOCUMENT CONTROL NO. 21-0137
REV. G
2/2
-DRAWING NOT TO SCALE-