VOICE COIL MOTOR DRIVER FOR CAMERA AUTO FOCUS

Check for Samples: DRV201

FEATURES

- **Configurable for Linear or PWM Mode VCM Current Generation**
- **High Efficiency PWM Current Control for VCM**
- **Advanced Ringing Compensation**
- **Integrated 10-bit D/A Converter for VCM Current Control**
- **Protection**
  - **Open and Short-Circuit Detection on VCM Pins**
  - **Undervoltage Lockout (UVLO)**
  - **Thermal Shutdown**
  - **Open and Short Circuit Protection on VCM Output**
  - **Internal Current Limit for VCM Driver**
- **I^2C Interface**
- **Operating Temperature Range: -40°C to 85°C**
- **6-Ball WCSP Package With 0.4-mm Pitch**
- **Max Die Size: 0.8 mm x 1.48 mm**
- **Package Height: 0.15 mm**

APPLICATIONS

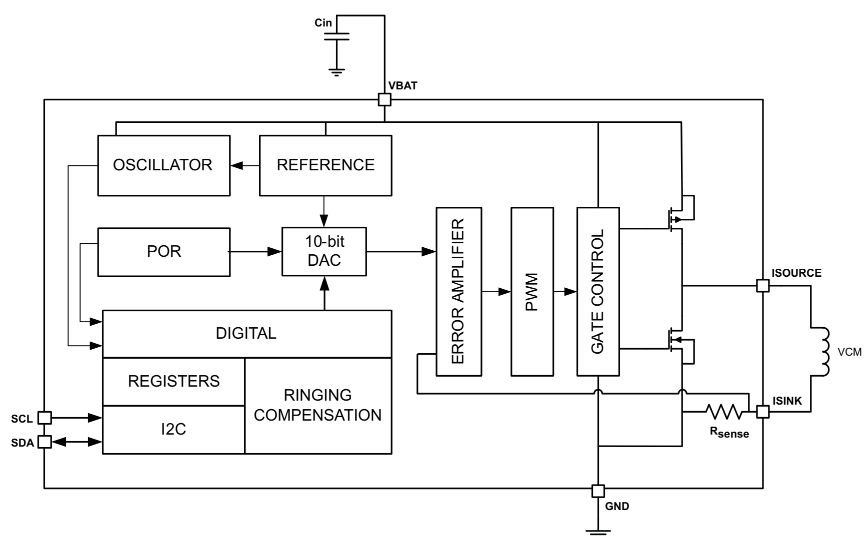
- **Cell Phone Auto Focus**
- **Digital Still Camera Auto Focus**
- **Iris/Exposure Control**
- **Security Cameras**
- **Web and PC Cameras**
- **Actuator Controls**

DESCRIPTION

The DRV201 is an advanced voice coil motor driver for camera auto focus. It has an integrated D/A converter for setting the VCM current. VCM current is controlled with a fixed frequency PWM controller or a linear mode driver. Current generation can be selected via I^2C register. The DRV201 has an integrated sense resistor for current regulation and the current can be controlled through I^2C.

When changing the current in the VCM, the lens ringing is compensated with an advanced ringing compensation function. Ringing compensation reduces the needed time for auto focus significantly. The device also has VCM short and open protection functions.

FUNCTIONAL BLOCK DIAGRAM



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This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ORDERING INFORMATION(1)

T_A	PACKAGE(2)	ORDERABLE PART NUMBER
-40°C to 85°C	YFM	DRV201YFMR

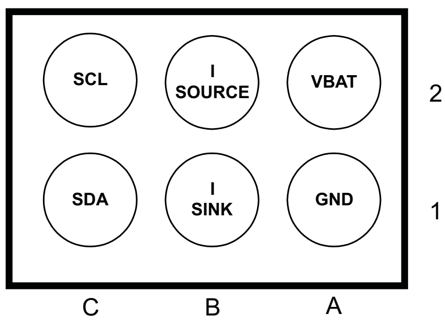
(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.

(2) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.

DEVICE INFORMATION

NanoFree PACKAGE

(BOTTOM VIEW)



TERMINAL FUNCTIONS

TERMINAL		I/O	DESCRIPTION
NAME	NO.		
VBAT	2A		Power
GND	1A		Ground
I_SOURCE	2B		Voice coil positive terminal
I_SINK	1B		Voice coil negative terminal
SCL	2C	I	I^2C serial interface clock input
SDA	1C	I/O	I^2C serial interface data input/output (open drain)

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ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted) (1)

			VALUE	UNIT
	VBAT, ISOURCE, ISOURCE pin voltage range(2)		–0.3 to 5.5	V
	Voltage range at SDA, SCL		–0.3 to 3.6	V
	Continuous total power dissipation		Internally limited	
θ_{JA}	Junction-to-ambient thermal resistance(3)		130	°C/W
T_J	Operating junction temperature		-40 to 125	°C
T_A	Operating ambient temperature		-40 to 85	°C
T_{stg}	Storage temperature		-55 to 150	°C
	ESD rating	(HBM) Human body model	±4000	V
		(CDM) Charged device model	±500	

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions is not implied. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to network ground terminal.
(3) This thermal data is measured with high-K board (4-layer board).

ELECTRICAL CHARACTERISTICS

Over recommended free-air temperature range and over recommended input voltage range (typical at an ambient temperature range of 25°C) (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
INPUT VOLTAGE						
V_{BAT}	Input supply voltage		2.5	3.7	4.8	V
V_{UVLO}	Undervoltage lockout threshold	V_{BAT} rising			2.2	V
		V_{BAT} falling	2			
V_{HYS}	Undervoltage lockout hysteresis		50	100	250	mV
INPUT CURRENT						
$I_{SHUTDOWN}$	Input supply current shutdown, includes switch leakage currents	MAX: V_{BAT} = 4.4 V		0.15	1	µA
$I_{STANDBY}$	Input supply current standby, includes switch leakage currents	MAX: V_{BAT} = 4.4 V		120	200	µA
STARTUP, MODE TRANSITIONS, AND SHUTDOWN						
t_1	Shutdown to standby				100	µs
t_2	Standby to active				100	µs
t_3	Active to standby				100	µs
t_4	Shutdown time	Active or standby to shutdown	0.5		1	ms
VCM DRIVER STAGE						
I_{RES}	Resolution			10		bits
	Relative accuracy		-10		10	LSB
	Differential nonlinearity		-1		1	
	Zero code error			0		mA
	Offset error	At code 32			3	mA
	Gain error			±3		% of FSR
	Gain error drift			0.3	0.4	%/°C
	Offset error drift			0.3	0.5	%/°C
I_{MAX}	Maximum output current			102.3		mA
I_{LIMIT}	Average VCM current limit	See (1)	110	160	240	mA

(1) During short circuit condition driver current limit comparator will trip and short is detected and driver goes into STANDBY and short flag is set high in the status register.

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ELECTRICAL CHARACTERISTICS (continued)

Over recommended free-air temperature range and over recommended input voltage range (typical at an ambient temperature range of 25°C) (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_{DETCODE}$	Minimum VCM code for OPEN and SHORT detection	See (2)	256			mA
f_{SW}	Switching frequency	Selectable through CONTROL register	0.5		4	MHz
V_{DRP}	Internal dropout	See (3)			0.4	V
L_{VCM}	VCM inductance		30		150	µH
R_{VCM}	VCM resistance		11		22	Ω
LENS MOVEMENT CONTROL						
t_{set1}	Lens settling time	±10% error band		$2/f_{VCM}$		ms
t_{set2}	Lens settling time	±10% error band		$1/f_{VCM}$		ms
f_{VCM}	VCM resonance frequency		50		150	Hz
	VCM resonance frequency tolerance		-20		20	%
LOGIC I/Os (SDA AND SCL)						
I_{IN}	Input leakage current	V = 3.6 V, SCL	-20		20	µA
		V = 3.6 V, SDA	-1		1	
R_{PullUp}	I^2C pull-up resistors	SDA and SCL pins		4.7		kΩ
V_{IH}	Input high level	See (4)	1.17		3.6	V
V_{IL}	Input low level	See (5)	0		0.63	V
$t_{TIMEOUT}$	SCL timeout for shutdown detection		0.5		1	ms
R_{PD}	Pull down resistor at SCL line			500		kΩ
f_{SCL}	I^2C clock frequency				400	kHz
INTERNAL OSCILLATOR						
f_{OSC}	Internal oscillator	20°C ≤ T_A ≤ 70°C	-3		3	%
	Frequency accuracy	-40°C ≤ T_A ≤ 85°C	-5		5	%
THERMAL SHUTDOWN						
T_{TRIP}	Thermal shutdown trip point			140		°C

(2) When testing VCM open or short this is the recommended minimum VCM code (in dec) to be used.
(3) This is the voltage that is needed for the feedback resistor and high side driver. It should be noted that the maximum VCM resistance is limited by this voltage and supply voltage. E.g. 3-V supply maximum VCM resistance is: $R_{VCM} = (V_{BAT} – V_{DRP})/I_{VCM}$ = (3 V - 0.4 V)/102.3 mA = 25.4 Ω.
(4) During shutdown to standby transition V_{IH} low limit is 1.28 V.
(5) During shutdown to standby transition V_{IL} low limit is 0.51 V.

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FUNCTIONAL DESCRIPTION

The DRV201 is intended for high performance autofocus in camera modules. It is used to control the current in the voice coil motor (VCM). The current in the VCM generates a magnetic field which forces the lens stack connected to a spring to move. The VCM current and thus the lens position can be controlled via the I^2C interface and an auto focus function can be implemented.

The device connects to a video processor or image sensor through a standard I^2C interface which supports up to 400-kbit/s data rate. The digital interface supports IO levels from 1.8 V to 3.3 V. All pins have 4-kV HBM ESD rating.

When SCL is low for at least 0.5 ms, the device enters SHUTDOWN mode. If SCL goes from low to high the driver enters STANDBY mode in less than 100 µs and default register values are set as shown in Figure 1. ACTIVE mode is entered when ever the VCM_CURRENT register is set to something else than zero.

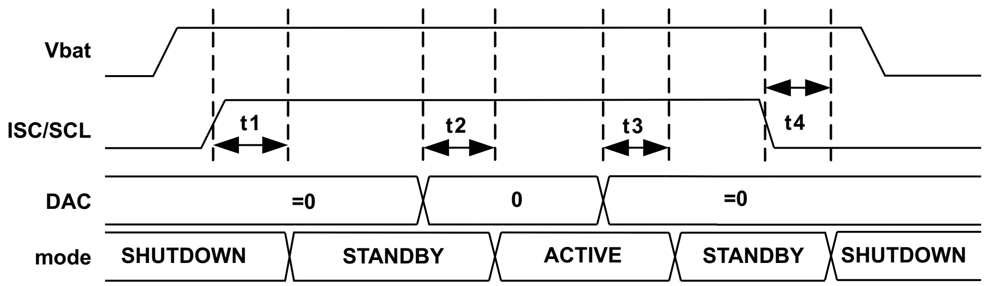

Figure 1. Power Up and Down Sequence

VCM current can be controlled via an I^2C interface and VCM_CURRENT registers. Lens stack is connected to a spring which causes a dampened ringing in the lens position when current is changed. This mechanical ringing is compensated internally by generating an optimized ramp when ever the current value in the VCM_CURRENT register is changed. This enables a fast autofocus algorithm and pleasant user experience.

Current in the VCM can be generated with a linear or PWM control. In linear mode the high side PMOS is configured as a current source and current is set by the VCM_CURRENT control register. In PWM control the VCM is driven with a half bridge driver. With PWM control the VCM current is increased by connecting the VCM between V_{BAT} and GND through the high side PMOS and then released to a ‘freewheeling’ mode through the sense resistor and low side NMOS. PWM mode switching frequency can be selected from 0.5 MHz up to 4 MHz through a CONTROL register. PWM or linear mode can be selected with the PWM/LIN bit in the MODE register.

MODES OF OPERATION

SHUTDOWN

If the driver detects SCL has a DC level below 0.63 V for duration of at least 0.5 ms, the driver will enter shutdown mode. This is the lowest power mode of operation. The driver will remain in shutdown for as long as SCL pin remain low.

STANDBY

If SCL goes from low to high the driver enters STANDBY mode and sets the default register values. In this mode registers can be written to through the I^2C interface. Device will be in STANDBY mode when VCM_CURRENT register is set to zero. From ACTIVE mode the device will enter STANDBY if the SW_RST bit of the CONTROL register is set. In this case all registers will be reset to default values.

STANDBY mode is entered from ACTIVE mode if any of the following faults occur: Over temperature protection fault (OTPF), VCM short (VCMS), or VCM open (VCMO). When STANDBY mode is entered due to a fault condition current register is cleared.

ACTIVE

The device is in ACTIVE mode whenever the VCM_CURRENT control is set to something else than zero through the I^2C interface. In ACTIVE mode VCM driver output stage is enabled all the time resulting in higher power consumption. The device remains in active mode until the SW_RST bit in the CONTROL register is set, SCL is pulled low for duration of 0.5 ms, VCM_CURRENT control is set to zero, or any of the following faults occur: Over temperature protection fault (OTPF), VCM short (VCMS), or VCM open (VCMO). If active mode is entered after fault the status register is automatically cleared.

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VCM DRIVER OUTPUT STAGE OPERATION

Current in the VCM can be controlled with a linear or PWM mode output stage. Output stage is enabled in ACTIVE mode which can be controlled through VCM_CURRENT control register and the output stage mode is selected from MODE register bit PWM/LIN.

In linear mode the output PMOS is configured to a high side current source and current can be controlled from a VCM_CURRENT registers.

In PWM control the VCM is driven with a half bridge driver. With PWM control the VCM current is increased by connecting the VCM between V_{BAT} and GND through the high side PMOS and then released to a 'freewheeling' mode through the sense resistor and low side NMOS. Current in the VCM is sensed with a 1-Ω sense resistor which is connected into an error amplifier input where the other input is controlled by the 10-bit DAC output. PWM mode switching frequency can be selected from 0.5 MHz up to 4 MHz through a CONTROL register. PWM or linear mode can be selected with the PWM/LIN bit in the MODE register.

RINGING COMPENSATION

VCM current can be controlled via an I^2C interface and VCM_CURRENT registers. Lens stack is connected to a spring which causes a dampened ringing in the lens position when current is changed. This mechanical ringing is compensated internally by generating an optimized ramp when ever the current value in the VCM_CURRENT register is changed. This enables a fast auto focus algorithm and pleasant user experience.

Ringing compensation is dependent on the VCM resonance frequency and this can be controlled via VCM_FREQ register from 50 Hz up 152 Hz with 0.4-Hz steps. Ringing compensation is designed in a way that it can tolerate ±20% frequency variation in the VCM resonance frequency so only statistical data from the VCM is needed in production.

I^2C BUS OPERATION

The DRV201 hosts a slave I^2C interface that supports data rates up to 400 kbit/s and auto-increment addressing and is compliant to I^2C standard 3.0.

Slave Address + R/nW										Sub Address									Data									
Start	G3	G2	G1	G0	A2	A1	A0	R/nW	ACK	S7	S6	S5	S4	S3	S2	S1	S0	ACK	D7	D6	D5	D4	D3	D2	D1	D0	ACK	Stop

Figure 2. Subaddress in I^2C Transmission

Start – Start condition

G(3:0) – Group ID: Address fixed at '0001'

A(2:0) – Device Address: Address fixed at '110'

R/nW – Read/not Write select bit

ACK – Acknowledge

S(7:0) – Subaddress: Defined per register map

D(7:0) – Data: Data to be loaded into the device

Stop – Stop condition

The I^2C Bus is a communications link between a controller and a series of slave terminals. The link is established using a two-wire bus consisting of a serial clock signal (SCL) and a serial data signal (SDA). The serial clock is sourced from the controller in all cases where the serial data line is bi-directional for data communication between the controller and the slave terminals. Each device has an open drain output to transmit data on the serial data line. An external pull-up resistor must be placed on the serial data line to pull the drain output high during data transmission.

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Data transmission is initiated with a start bit from the controller as shown in Figure 3. The start condition is recognized when the SDA line transitions from high to low during the high portion of the SCL signal. Upon reception of a start bit, the device will receive serial data on the SDA input and check for valid address and control information. If the appropriate slave address bits are set for the device, then the device will issue an acknowledge pulse and prepare to receive the register address. Depending on the R/nW bit, the next byte received from the master is written to the addressed register (R/nW = 0) or the device responds with 8-bit data from the register (R/nW = 1). Data transmission is completed by either the reception of a stop condition or the reception of the data word sent to the device. A stop condition is recognized as a low to high transition of the SDA input during the high portion of the SCL signal. All other transitions of the SDA line must occur during the low portion of the SCL signal. An acknowledge is issued after the reception of valid address, sub-address and data words. The I^2C interfaces will auto-sequence through register addresses, so that multiple data words can be sent for a given I^2C transmission. Reference Figure 4.

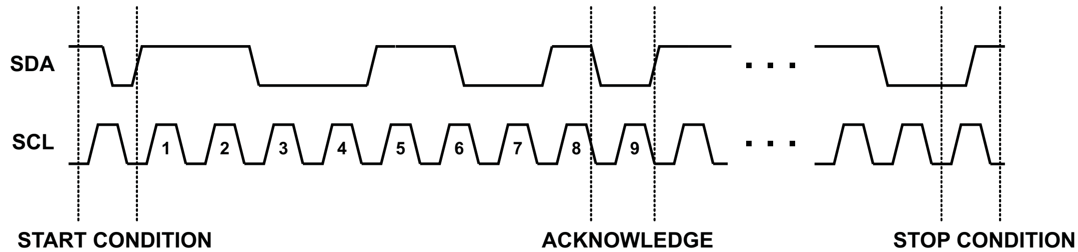

Figure 3. I^2C Start/Stop/Acknowledge Protocol

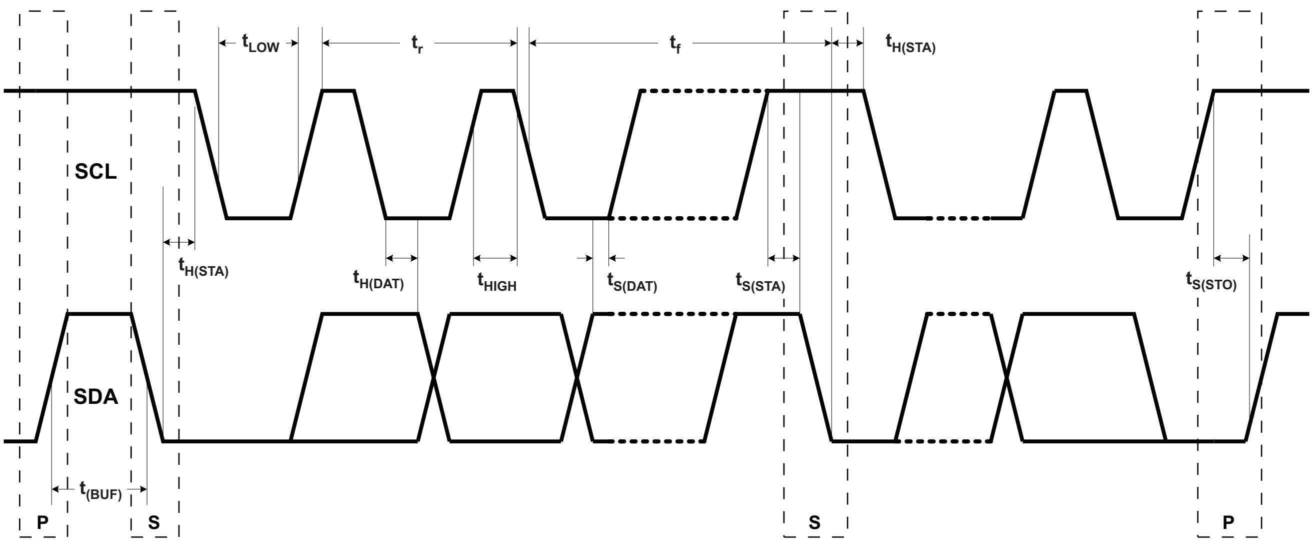

Figure 4. I^2C Data Transmission Protocol

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DATA TRANSMISSION TIMING

V_{BAT} = 3.6 V ±5%, T_A = 25ºC, C_L = 100 pF (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$f_{(SCL)}$	Serial clock frequency		100		400	KHz
t_{BUF}	Bus Free Time Between Stop and Start Condition	SCL = 100 KHz	4.7			μs
		SCL = 400 KHz	1.3			
t_{SP}	Tolerable spike width on bus	SCL = 100 KHz			50	ns
		SCL = 400 KHz				
t_{LOW}	SCL low time	SCL = 100 KHz	4.7			μs
		SCL = 400 KHz	1.3			
t_{HIGH}	SCL high time	SCL = 100 KHz	4			μs
		SCL = 400 KHz	600			ns
$t_{S(DAT)}$	SDA → SCL setup time	SCL = 100 KHz	250			ns
		SCL = 400 KHz	100			
$t_{S(STA)}$	Start condition setup time	SCL = 100 KHz	4.7			μs
		SCL = 400 KHz	600			ns
$t_{S(STO)}$	Stop condition setup time	SCL = 100 KHz	4			μs
		SCL = 400 KHz	600			ns
$t_{H(DAT)}$	SDA → SCL hold time	SCL = 100 KHz	0		3.45	μs
		SCL = 400 KHz	0		0.9	
$t_{H(STA)}$	Start condition hold time	SCL = 100 KHz	4			μs
		SCL = 400 KHz	600			ns
$t_{r(SCL)}$	Rise time of SCL Signal	SCL = 100 KHz			1000	ns
		SCL = 400 KHz			300	
$t_{f(SCL)}$	Fall time of SCL Signal	SCL = 100 KHz			300	ns
		SCL = 400 KHz			300	
$t_{r(SDA)}$	Rise time of SDA Signal	SCL = 100 KHz			1000	ns
		SCL = 400 KHz			300	
$t_{f(SDA)}$	Rise time of SDA Signal	SCL = 100 KHz			300	ns
		SCL = 400 KHz			300	

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REGISTER ADDRESS MAP

REGISTER	ADDRESS (HEX)	NAME	DEFAULT VALUE	DESCRIPTION
1	01	not used		
2	02	CONTROL	0000 0010	Control register
3	03	VCM_CURRENT_MSB	0000 0000	Voice coil motor MSB current control
4	04	VCM_CURRENT_LSB	0000 0000	Voice coil motor LSB current control
5	05	STATUS	0000 0000	Status register
6	06	MODE	0000 0000	Mode register
7	07	VCM_FREQ	1000 0011	VCM resonance frequency

CONTROL REGISTER (CONTROL)

Address – 0x02h

DATA BIT	D7	D6	D5	D4	D3	D2	D1	D0
FIELD NAME	not used	not used	not used	not used	not used	not used	EN_RING	RESET
READ/WRITE	R	R	R	R	R	R	R/W	R/W
RESET VALUE	0	0	0	0	0	0	1	0

FIELD NAME	BIT DEFINITION
RESET	Forced software reset (reset all registers to default values) and device goes into STANDBY. RESET bit is automatically cleared when written high. 0 – inactive 1 – device goes to STANDBY
EN_RING	Enables ringing compensation. 0 – disabled 1 – enabled

VCM MSB CURRENT CONTROL REGISTER (VCM_CURRENT_MSB)

Address – 0x03h

DATA BIT	D7	D6	D5	D4	D3	D2	D1	D0
FIELD NAME	not used	not used	not used	not used	not used	not used	VCM_CURRENT[9:0]	
READ/WRITE	R	R	R	R	R	R	R/W	
RESET VALUE	0	0	0	0	0	0	0	0

FIELD NAME	BIT DEFINITION
VCM_CURRENT[9:0]	VCM current control 00 0000 0000b – 0 mA 00 0000 0001b – 0.1 mA 00 0000 0010b – 0.2 mA … 11 1111 1110b – 102.2 mA 11 1111 1111b – 102.3 mA

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VCM LSB CURRENT CONTROL REGISTER (VCM_CURRENT_LSB)

Address – 0x04h

DATA BIT	D7	D6	D5	D4	D3	D2	D1	D0
FIELD NAME	VCM_CURRENT[7:0]							
READ/WRITE	R/W							
RESET VALUE	0	0	0	0	0	0	0	0

FIELD NAME	BIT DEFINITION
VCM_CURRENT[7:0]	VCM current control 00 0000 0000b – 0 mA 00 0000 0001b – 0.1 mA 00 0000 0010b – 0.2 mA … 11 1111 1110b – 102.2 mA 11 1111 1111b – 102.3 mA

STATUS REGISTER (STATUS)(1)

Address – 0x05h

DATA BIT	D7	D6	D5	D4	D3	D2	D1	D0
FIELD NAME	not used	not used	not used	TSD	VCMS	VCMO	UVLO	OVC
READ/WRITE	R	R/WR	R	R	R	R	R	R
RESET VALUE	0	0	0	0	0	0	0	0

(1) Status bits are cleared when device changes it's state from standby to active. If TSD was tripped the device goes into Standby and will not allow the transition into Active until the device cools down and TSD is cleared.

FIELD NAME	BIT DEFINITION
OVC	Over current detection
UVLO	Undervoltage Lockout
VCMO	Voice coil motor open detected
VCMS	Voice coil motor short detected
TSD	Thermal shutdown detected

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MODE REGISTER (MODE)

Address – 0x06h

DATA BIT	D7	D6	D5	D4	D3	D2	D1	D0
FIELD NAME	not used	not used	not used	PWM_FREQ[2:0]			PWM/LIN	RING_MODE
READ/WRITE	R	R	R	R/W	R/W	R/W	R/W	R/W
RESET VALUE	0	0	0	0	0	0	0	0

FIELD NAME	BIT DEFINITION
RING_MODE	Ringing compensation settling time 0 – 2x(1/f_{VCM}) 1 – 1x(1/f_{VCM})
PWM/LIN	Driver output stage in linear or PWM mode 0 – PWM mode 1 – Linear mode
PWM_FREQ[2:0]	Output stage PWM switching frequency 000 – 0.5 MHz 001 – 1 MHz 010 – N/A 011 – 2 MHz 100 – N/A 101 – N/A 110 – N/A 111 – 4 MHz

VCM RESONANCE FREQUENCY REGISTER (VCM_FREQ)

Address – 0x07h

DATA BIT	D7	D6	D5	D4	D3	D2	D1	D0
FIELD NAME	VCM_FREQ[7:0]							
READ/WRITE	R/W							
RESET VALUE	1	0	0	0	0	0	1	1

FIELD NAME	BIT DEFINITION
VCM_FREQ[7:0]	VCM mechanical ringing frequency for the ringing compensation can be selected with the below formula. The formula gives the VCM_FREQ[7:0] register value in decimal which should be rounded to the nearest integer. $$VCM\_FREQ = 383 - \frac{19200}{F_{res}} \quad (1)$$ Default VCM mechanical ringing frequency is 76.4 Hz. $$VCM\_FREQ = 383 - \frac{19200}{76.4} = 131.69 \Rightarrow 132 \Rightarrow '1000\ 0011' \quad (2)$$

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/ Ball Finish	MSL Peak Temp (3)	Samples (Requires Login)
DRV201YFMR	ACTIVE	DSLGA	YFM	6	3000	Green (RoHS & no Sb/Br)	Call TI	Level-1-260C-UNLIM	
DRV201YFMT	ACTIVE	DSLGA	YFM	6	250	Green (RoHS & no Sb/Br)	Call TI	Level-1-260C-UNLIM	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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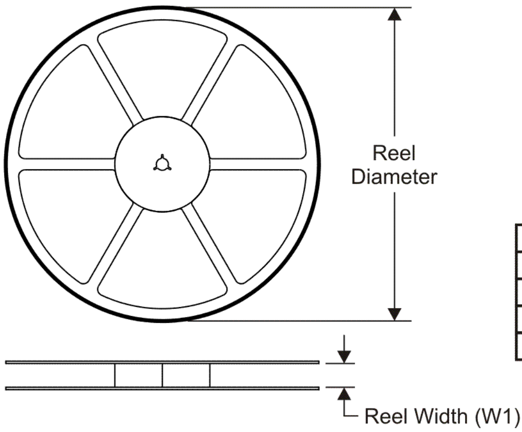
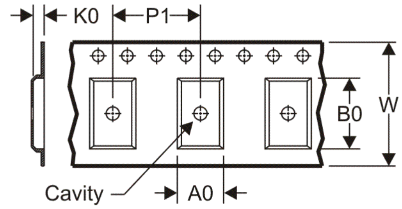
TAPE AND REEL INFORMATION

REEL DIMENSIONS

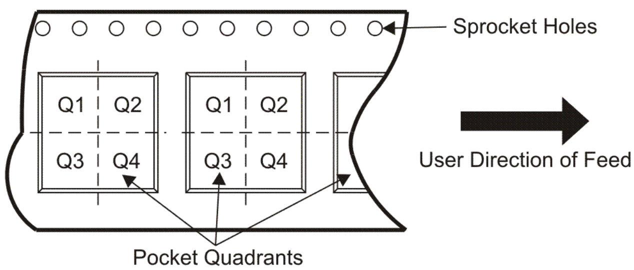


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

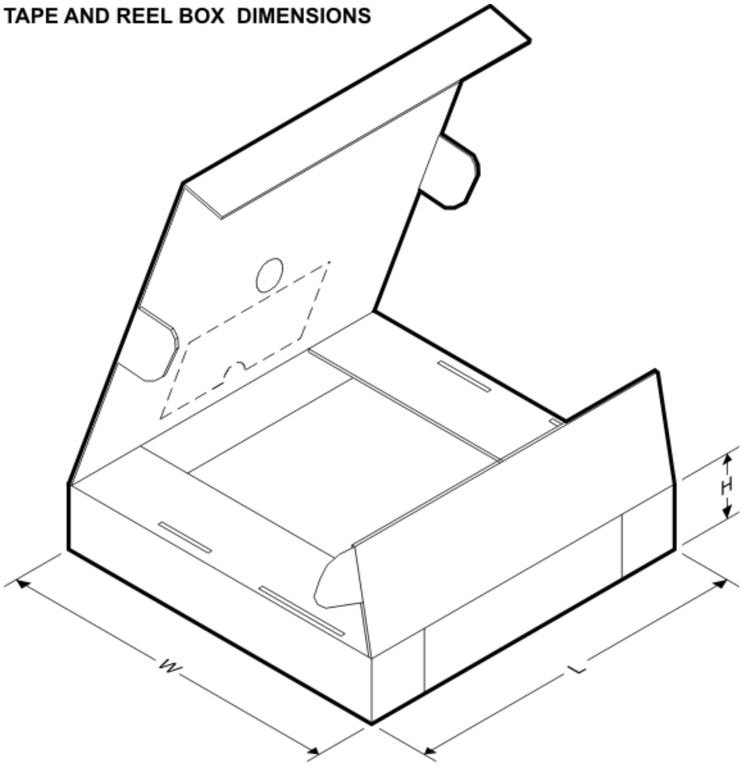
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DRV201YFMR	DSLGA	YFM	6	3000	180.0	8.4	0.85	1.52	0.19	4.0	8.0	Q1
DRV201YFMT	DSLGA	YFM	6	250	180.0	8.4	0.85	1.52	0.19	4.0	8.0	Q1

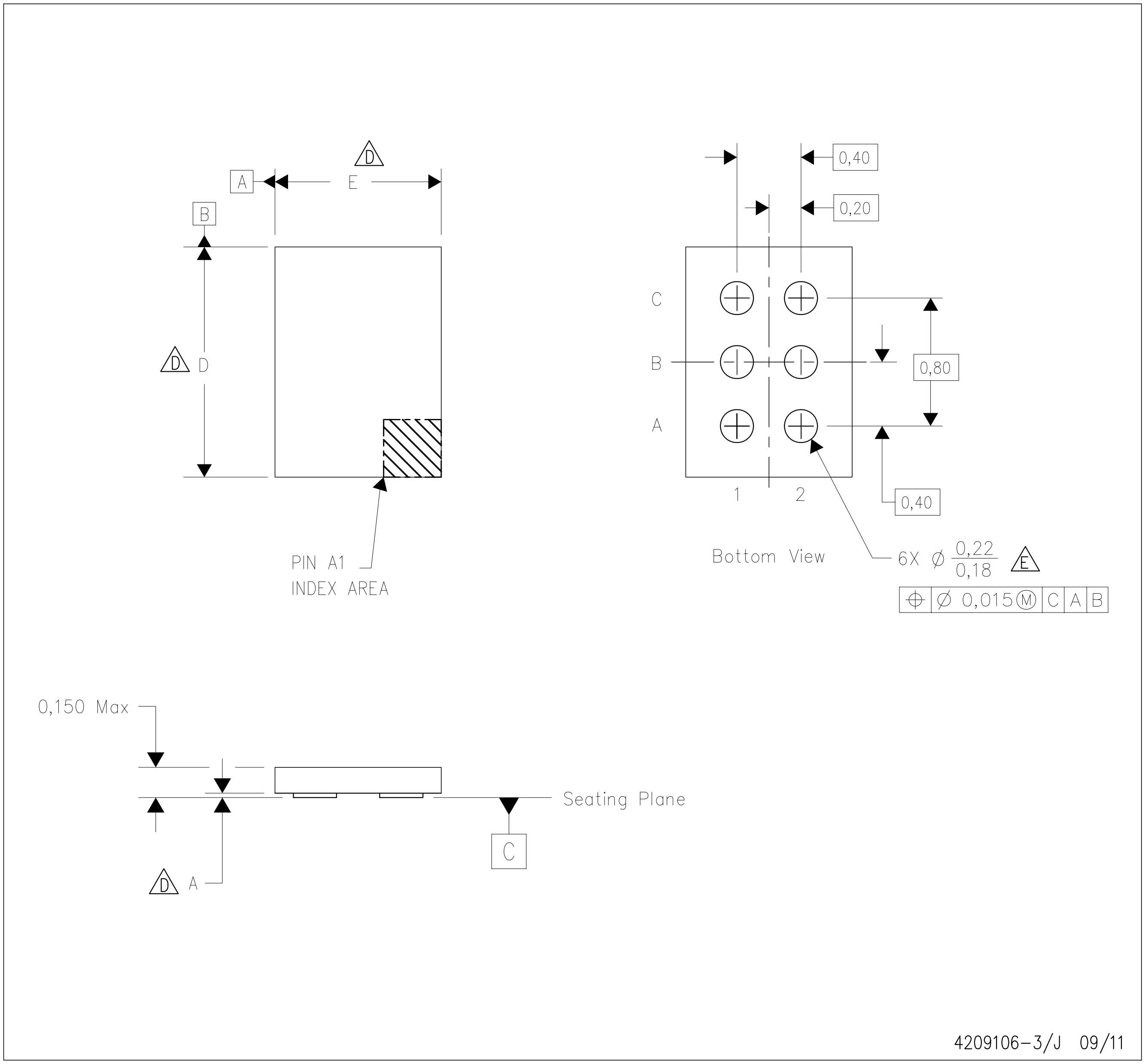
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DRV201YFMR	DSLGA	YFM	6	3000	210.0	185.0	35.0
DRV201YFMT	DSLGA	YFM	6	250	210.0	185.0	35.0

YFM (R-pSTAR-N6) PicoStar™



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
B. This drawing is subject to change without notice.
C. PicoStar™ package configuration.
D. The package size (Dimension D and E) of a particular device is specified in the device Product Data Sheet version of this drawing, in case it cannot be found in the product data sheet please contact a local TI representative.
E. Reference Product Data Sheet for array population. 2 x 3 matrix pattern is shown for illustration only.
F. This package is a Pb-free solder land design.

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