

TOSHIBA CMOS Digital Integrated Circuit Silicon Monolithic

TC74HC564AP, TC74HC564AF, TC74HC574AP, TC74HC574AF

Octal D-Type Flip-Flop with 3-State Output

TC74HC564AP/AF Inverting

TC74HC574AP/AF Non-Inverting

The TC74HC564A and HC574A are high speed CMOS OCTAL FLIP-FLOPs with 3-STATE OUTPUT fabricated with silicon gate C²MOS technology.

They achieve the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

These 8-bit D-type flip-flops are controlled by a clock input (CK) and an output enable input ($\overline{OE}$).

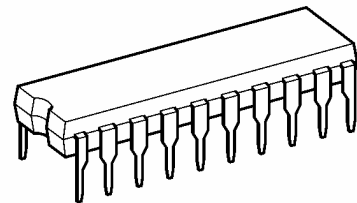
The TC74HC564A has inverting outputs, and the TC74HC574A has non-inverting outputs.

All inputs are equipped with protection circuits against static discharge or transient excess voltage.

Features

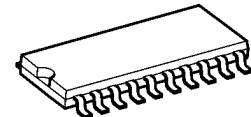
- High speed: $f_{\max} = 62$ MHz (typ.) at $V_{CC} = 5$ V
- Low power dissipation: $I_{CC} = 4$ μ A (max) at $T_a = 25^\circ\text{C}$
- High noise immunity: $V_{NIH} = V_{NIL} = 28\% V_{CC}$ (min)
- Output drive capability: 15 LSTTL loads
- Symmetrical output impedance: $|I_{OH}| = I_{OL} = 6$ mA (min)
- Balanced propagation delays: $t_{PLH} \approx t_{PHL}$
- Wide operating voltage range: $V_{CC}(\text{opr}) = 2$ to 6 V
- Pin and function compatible with 74LS564/574

TC74HC564AP, TC74HC574AP



DIP20-P-300-2.54A

TC74HC564AF, TC74HC574AF



SOP20-P-300-1.27A

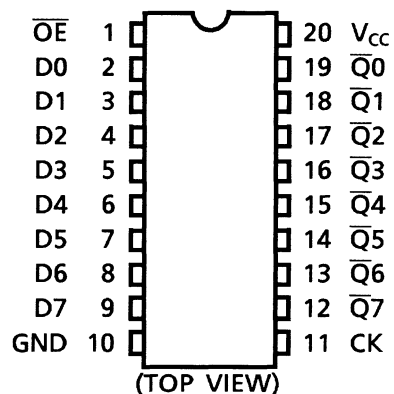
Weight

DIP20-P-300-2.54A : 1.30 g (typ.)

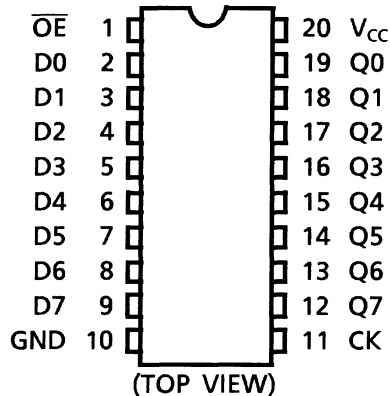
SOP20-P-300-1.27A : 0.22 g (typ.)

Pin Assignment

TC74HC564A

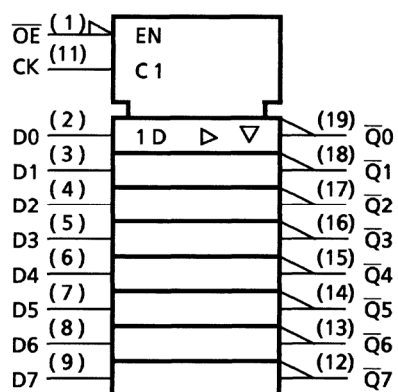


TC74HC574A

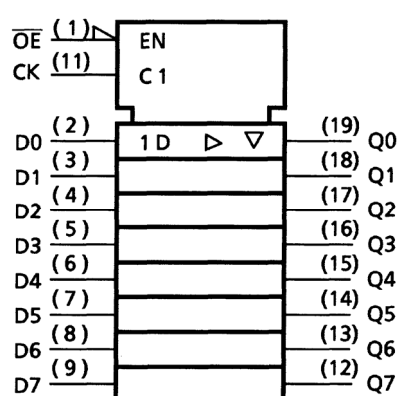


IEC Logic Symbol

TC74HC564A



TC74HC574A



Truth Table

Inputs			Outputs	
OE	CK	D	Q (574A)	Q̄ (564A)
H	X	X	Z	Z
L		X	Q _n	Q̄ _n
L		L	L	H
L		H	H	L

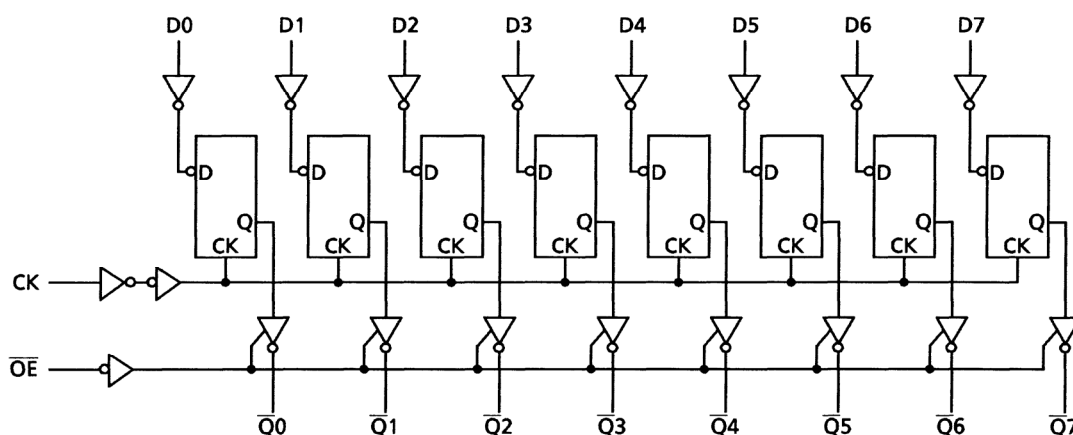
X: Don't care

Z: High impedance

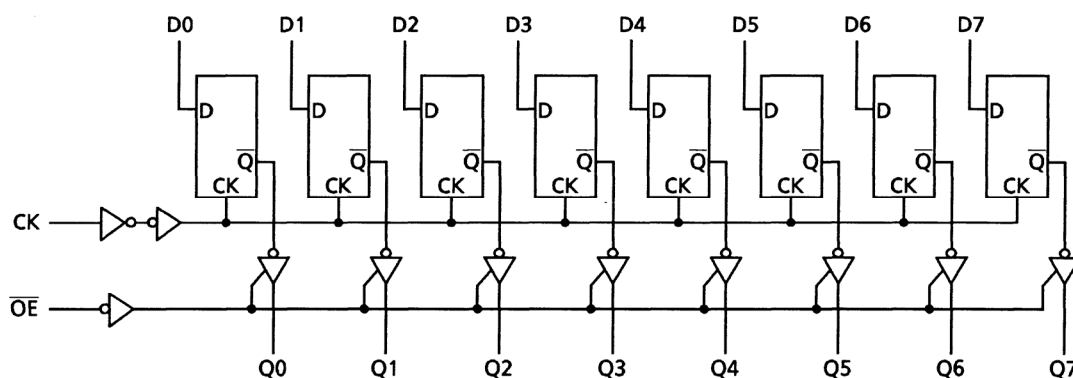
Q_n (Q̄_n): No change

System Diagram

TC74HC564A



TC74HC574A



Absolute Maximum Ratings (Note 1)

Characteristics	Symbol	Rating	Unit
Supply voltage range	V_{CC}	-0.5 to 7	V
DC input voltage	V_{IN}	-0.5 to $V_{CC} + 0.5$	V
DC output voltage	V_{OUT}	-0.5 to $V_{CC} + 0.5$	V
Input diode current	I_{IK}	± 20	mA
Output diode current	I_{OK}	± 20	mA
DC output current	I_{OUT}	± 35	mA
DC V_{CC} /ground current	I_{CC}	± 75	mA
Power dissipation	P_D	500 (DIP) (Note 2)/180 (SOP)	mW
Storage temperature	T_{stg}	-65 to 150	°C

Note 1: Exceeding any of the absolute maximum ratings, even briefly, lead to deterioration in IC performance or even destruction.

Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings and the operating ranges.

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc.).

Note 2: 500 mW in the range of $T_a = -40$ to 65°C . From $T_a = 65$ to 85°C a derating factor of -10 mW/°C shall be applied until 300 mW.

Operating Ranges (Note)

Characteristics	Symbol	Rating	Unit
Supply voltage	V_{CC}	2 to 6	V
Input voltage	V_{IN}	0 to V_{CC}	V
Output voltage	V_{OUT}	0 to V_{CC}	V
Operating temperature	T_{opr}	-40 to 85	°C
Input rise and fall time	t_r, t_f	0 to 1000 ($V_{CC} = 2.0$ V) 0 to 500 ($V_{CC} = 4.5$ V) 0 to 400 ($V_{CC} = 6.0$ V)	ns

Note: The operating ranges must be maintained to ensure the normal operation of the device.
Unused inputs must be tied to either VCC or GND.

Electrical Characteristics
DC Characteristics

Characteristics	Symbol	Test Condition		Ta = 25°C			Ta = −40 to 85°C		Unit		
				V _{CC} (V)	Min	Typ.	Max	Min		Max	
High-level input voltage	V _{IH}	—		2.0 4.5 6.0	1.50 3.15 4.20	— — —	— — —	1.50 3.15 4.20	V		
Low-level input voltage	V _{IL}	—		2.0 4.5 6.0	— — —	— — —	0.50 1.35 1.80	— — —	0.50 1.35 1.80	V	
High-level output voltage	V _{OH}	V _{IN} = V _{IH} or V _{IL}	I _{OH} = −20 μA	2.0	1.9	2.0	—	1.9	—	V	
				4.5	4.4	4.5	—	4.4	—		
				6.0	5.9	6.0	—	5.9	—		
			I _{OH} = −6 mA	4.5	4.18	4.31	—	4.13	—		V
I _{OH} = −7.8 mA	6.0	5.68	5.80	—	5.63	—					
Low-level output voltage	V _{OL}	V _{IN} = V _{IH} or V _{IL}	I _{OL} = 20 μA	2.0	—	0.0	0.1	—	0.1	V	
				4.5	—	0.0	0.1	—	0.1		
				6.0	—	0.0	0.1	—	0.1		
			I _{OL} = 6 mA	4.5	—	0.17	0.26	—	0.33		V
			I _{OL} = 7.8 mA	6.0	—	0.18	0.26	—	0.33		
3-state output off-state current	I _{OZ}	V _{IN} = V _{IH} or V _{IL} V _{OUT} = V _{CC} or GND		6.0	—	—	±0.5	—	±5.0	μA	
Input leakage current	I _{IN}	V _{IN} = V _{CC} or GND		6.0	—	—	±0.1	—	±1.0	μA	
Quiescent supply current	I _{CC}	V _{IN} = V _{CC} or GND		6.0	—	—	4.0	—	40.0	μA	

Timing Requirements (input: $t_r = t_f = 6 \text{ ns}$)

Characteristics	Symbol	Test Condition	Ta = 25°C		Ta = -40 to 85°C	Unit
			V _{CC} (V)	Typ.	Limit	
Minimum pulse width (CK)	t_W (H) t_W (L)	—	2.0	—	75	ns
			4.5	—	15	
			6.0	—	13	
Minimum set-up time (Dn)	t_s	—	2.0	—	75	ns
			4.5	—	15	
			6.0	—	13	
Minimum hold time (Dn)	t_h	—	2.0	—	0	ns
			4.5	—	0	
			6.0	—	0	
Clock frequency	f	—	2.0	—	6	MHz
			4.5	—	31	
			6.0	—	36	

AC Characteristics (input: $t_r = t_f = 6 \text{ ns}$)

Characteristics	Symbol	Test Condition			Ta = 25°C			Ta = -40 to 85°C		Unit
			CL (pF)	V _{CC} (V)	Min	Typ.	Max	Min	Max	
Output transition time	t_{TLH} t_{THL}	—	50	2.0	—	25	60	—	75	ns
				4.5	—	7	12	—	15	
				6.0	—	6	10	—	13	
Propagation delay time (CK-Q, $\bar{Q}$)	t_{pLH} t_{pHL}	—	50	2.0	—	70	150	—	190	ns
				4.5	—	20	30	—	38	
				6.0	—	15	26	—	33	
			150	2.0	—	88	190	—	240	
				4.5	—	25	38	—	48	
				6.0	—	19	33	—	41	
Output enable time	t_{pZL} t_{pZH}	$R_L = 1 \text{ k}\Omega$	50	2.0	—	48	125	—	155	ns
				4.5	—	15	25	—	31	
				6.0	—	12	21	—	26	
			150	2.0	—	60	165	—	205	
				4.5	—	20	33	—	41	
				6.0	—	16	28	—	35	
Output disable time	t_{pLZ} t_{pHZ}	$R_L = 1 \text{ k}\Omega$	50	2.0	—	34	125	—	155	ns
				4.5	—	17	25	—	31	
				6.0	—	15	21	—	26	
Maximum clock frequency	f_{max}	—	50	2.0	6	17	—	5	—	MHz
				4.5	31	50	—	24	—	
				6.0	36	59	—	28	—	
Input capacitance	C_{IN}	—	—	—	—	5	10	—	10	pF
Output capacitance	C_{OUT}	—	—	—	—	10	—	—	—	pF
Power dissipation capacitance	C_{PD} (Note)	—	—	—	—	54	—	—	—	pF

Note: C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.

Average operating current can be obtained by the equation:

$$I_{\text{CC}} (\text{opr}) = C_{\text{PD}} \cdot V_{\text{CC}} \cdot f_{\text{IN}} + I_{\text{CC}}/8 \text{ (per bit)}$$

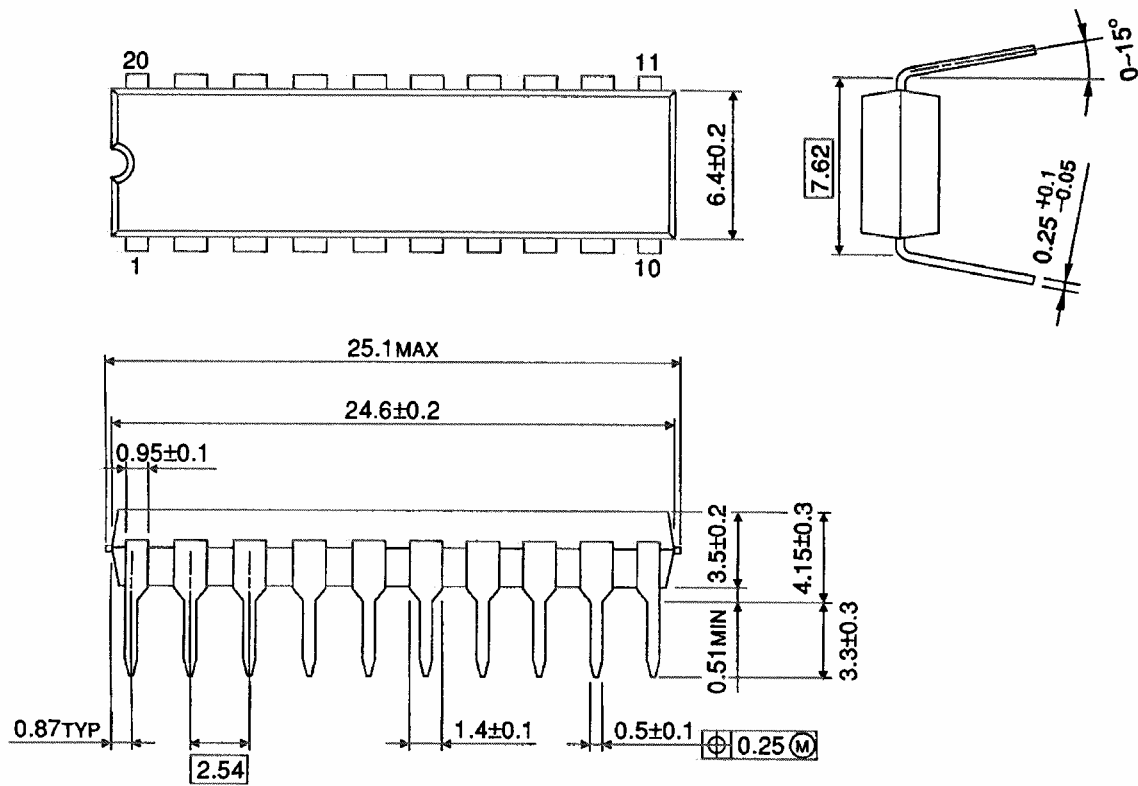
And the total C_{PD} when n pcs. of flip flop operate can be gained by the following equation:

$$C_{\text{PD}} (\text{total}) = 39 + 15 \cdot n$$

Package Dimensions

DIP20-P-300-2.54A

Unit : mm

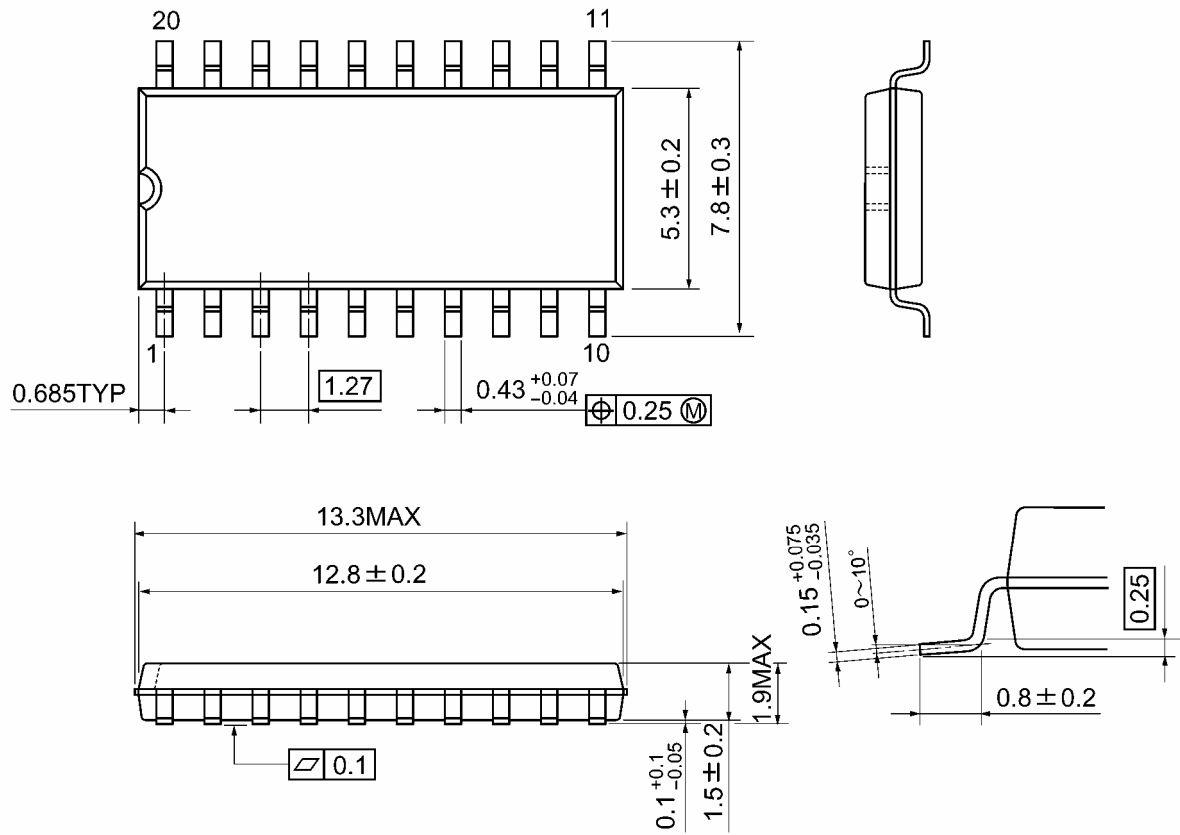


Weight: 1.30 g (typ.)

Package Dimensions

SOP20-P-300-1.27A

Unit: mm



Weight: 0.22 g (typ.)

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20070701-EN GENERAL

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