TOSHIBA CMOS Digital Integrated Circuit Silicon Monolithic

TC74HC4514AP

4-to-16 Line Decoder/Latch

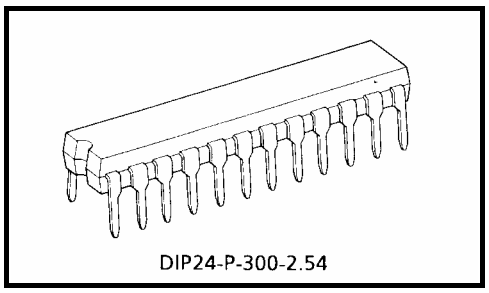
The TC74HC4514A are high speed CMOS 4-LINE TO 16-LINE DECODER WITH LATCHED INPUTs fabricated with silicon gate C^2MOS technology.

It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

The selected output is enabled by a low on the inhibit input (INHIBIT). A binary code stored in the four input latches (A thru D) is decided and provides a high level at the corresponding one of sixteen outputs. When the INHIBIT is held low, all outputs are kept low however, the latch function is available.

The data applied to the data inputs are transferred to the outputs of latches when the strobe input is held high. When the strobe input is taken low, the data is retained at the output of the latches.

All inputs are equipped with protection circuits against static discharge or transient excess voltage.

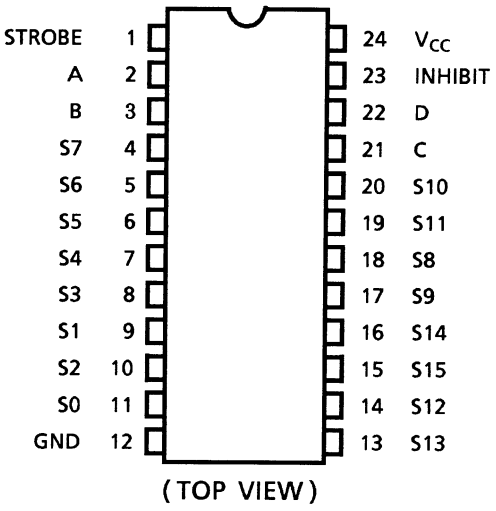


Weight: 1.50 g (typ.)

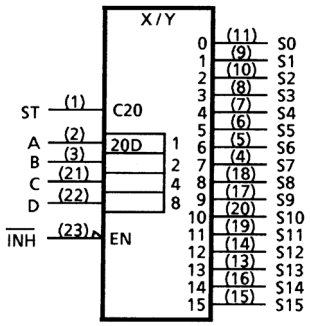
Features

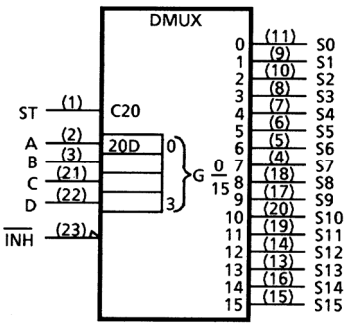
- High speed: t_{pd} = 18 ns (typ.) at V_{CC} = 5 V
- Low power dissipation: I_{CC} = 4 μA (max) at Ta = 25°C
- High noise immunity: $V_{NIH} = V_{NIL}$ = 28% V_{CC} (min)
- Output drive capability: 10 LSTTL loads
- Symmetrical output impedance: $|I_{OH}| = I_{OL}$ = 4 mA (min)
- Balanced propagation delays: $t_{pLH} \simeq t_{pHL}$
- Wide operating voltage range: V_{CC} (opr) = 2 to 6 V
- Pin and function compatible with 4514B

Pin Assignment



IEC Logic Symbol





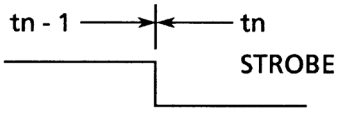
Truth Table

Inputs					Selected Outputs
Inhibit	A	B	C	D	"H"
L	L	L	L	L	S0
L	H	L	L	L	S1
L	L	H	L	L	S2
L	H	H	L	L	S3
L	L	L	H	L	S4
L	H	L	H	L	S5
L	L	H	H	L	S6
L	H	H	H	L	S7
L	L	L	L	H	S8
L	H	L	L	H	S9
L	L	H	L	H	S10
L	H	H	L	H	S11
L	L	L	H	H	S12
L	H	L	H	H	S13
L	L	H	H	H	S14
L	H	H	H	H	S15
H	X	X	X	X	All Outputs "L"

X: Don't care

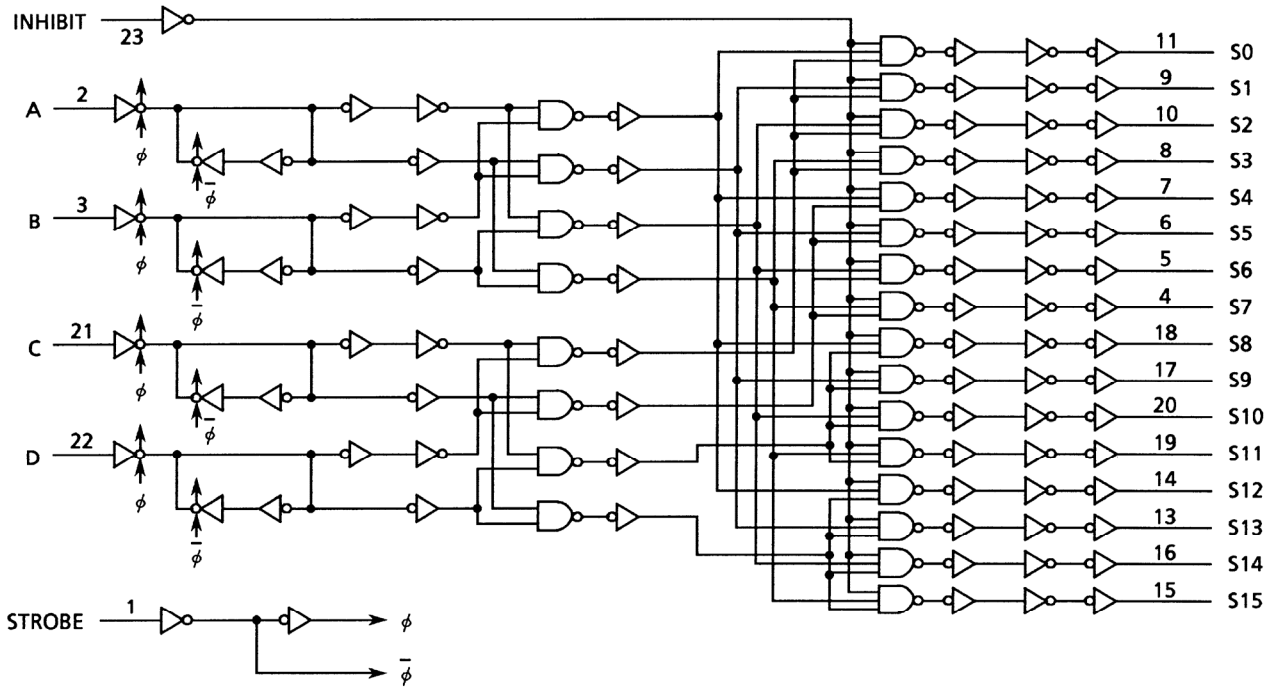
STROBE = "H"; Refer to truth table

STROBE = "L"



Data at the negative going transition of strobe shall be provided on each output while strobe is held low.

System Diagram



Absolute Maximum Ratings (Note 1)

Characteristics	Symbol	Rating	Unit
Supply voltage range	V_{CC}	−0.5 to 7	V
DC input voltage	V_{IN}	−0.5 to V_{CC} + 0.5	V
DC output voltage	V_{OUT}	−0.5 to V_{CC} + 0.5	V
Input diode current	I_{IK}	±20	mA
Output diode current	I_{OK}	±20	mA
DC output current	I_{OUT}	±25	mA
DC V_{CC}/ground current	I_{CC}	±50	mA
Power dissipation	P_D	500 (DIP) (Note 2)	mW
Storage temperature	T_{stg}	−65 to 150	°C

Note 1: Exceeding any of the absolute maximum ratings, even briefly, lead to deterioration in IC performance or even destruction.
Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings and the operating ranges.
Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook (“Handling Precautions”/“Derating Concept and Methods”) and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Note 2: 500 mW in the range of Ta = −40 to 65°C. From Ta = 65 to 85°C a derating factor of −10 mW/°C shall be applied until 300 mW.

Operating Ranges (Note)

Characteristics	Symbol	Rating	Unit
Supply voltage	V_{CC}	2 to 6	V
Input voltage	V_{IN}	0 to V_{CC}	V
Output voltage	V_{OUT}	0 to V_{CC}	V
Operating temperature	T_{opr}	−40 to 85	°C
Input rise and fall time	t_r, t_f	0 to 1000 (V_{CC} = 2.0 V) 0 to 500 (V_{CC} = 4.5 V) 0 to 400 (V_{CC} = 6.0 V)	ns

Note: The operating ranges must be maintained to ensure the normal operation of the device. Unused inputs must be tied to either VCC or GND.

Electrical Characteristics

DC Characteristics

Characteristics	Symbol	Test Condition		V_{CC} (V)	Ta = 25°C Min	Ta = 25°C Typ.	Ta = 25°C Max	Ta = −40 to 85°C Min	Ta = −40 to 85°C Max	Unit
High-level input voltage	V_{IH}	—		2.0	1.50	—	—	1.50	—	V
				4.5	3.15	—	—	3.15	—	
				6.0	4.20	—	—	4.20	—	
Low-level input voltage	V_{IL}	—		2.0	—	—	0.50	—	0.50	V
				4.5	—	—	1.35	—	1.35	
				6.0	—	—	1.80	—	1.80	
High-level output voltage	V_{OH}	V_{IN} = V_{IH} or V_{IL}	I_{OH} = −20 μA	2.0	1.9	2.0	—	1.9	—	V
				4.5	4.4	4.5	—	4.4	—	
				6.0	5.9	6.0	—	5.9	—	
			I_{OH} = −4 mA	4.5	4.18	4.31	—	4.13	—	
			I_{OH} = −5.2 mA	6.0	5.68	5.80	—	5.63	—	
Low-level output voltage	V_{OL}	V_{IN} = V_{IH} or V_{IL}	I_{OL} = 20 μA	2.0	—	0.0	0.1	—	0.1	V
				4.5	—	0.0	0.1	—	0.1	
				6.0	—	0.0	0.1	—	0.1	
			I_{OL} = 4 mA	4.5	—	0.17	0.26	—	0.33	
			I_{OL} = 5.2 mA	6.0	—	0.18	0.26	—	0.33	
Input leakage current	I_{IN}	V_{IN} = V_{CC} or GND		6.0	—	—	±0.1	—	±1.0	μA
Quiescent supply current	I_{CC}	V_{IN} = V_{CC} or GND		6.0	—	—	4.0	—	40.0	μA

Timing Requirements (input: $t_r = t_f = 6$ ns)

Characteristics	Symbol	Test Condition		Ta = 25°C		Ta = −40 to 85°C	Unit
			V_{CC} (V)	Typ.	Limit	Limit	
Minimum pulse width (STROBE)	$t_{W(H)}$	—	2.0	—	75	95	ns
			4.5	—	15	19	
			6.0	—	13	16	
Minimum set-up time (DATA)	t_s	—	2.0	—	50	65	ns
			4.5	—	10	13	
			6.0	—	9	11	
Minimum hold time (DATA)	t_h	—	2.0	—	5	5	ns
			4.5	—	5	5	
			6.0	—	5	5	

AC Characteristics ($C_L = 15$ pF, $V_{CC} = 5$ V, Ta = 25°C, input: $t_r = t_f = 6$ ns)

Characteristics	Symbol	Test Condition	Min	Typ.	Max	Unit
Output transition time	t_{TLH} t_{THL}	—	—	4	8	ns
Propagation delay time (DATA-Sn)	t_{pLH} t_{pHL}	—	—	18	30	ns
Propagation delay time (STROBE-Sn)	t_{pLH} t_{pHL}	—	—	20	30	ns
Propagation delay time (INHIBIT-Sn)	t_{pLH} t_{pHL}	—	—	16	30	ns

AC Characteristics (C_L = 50 pF, input: $t_r = t_f$ = 6 ns)

Characteristics	Symbol	Test Condition		Ta = 25°C			Ta = −40 to 85°C		Unit
			V_{CC} (V)	Min	Typ.	Max	Min	Max	
Output transition time	t_{TLH} t_{THL}	—	2.0	—	30	75	—	95	ns
			4.5	—	8	15	—	19	
			6.0	—	7	13	—	16	
Propagation delay time (DATA-Sn)	t_{pLH} t_{pHL}	—	2.0	—	65	175	—	220	ns
			4.5	—	22	35	—	44	
			6.0	—	19	30	—	37	
Propagation delay time (STROBE-Sn)	t_{pLH} t_{pHL}	—	2.0	—	75	175	—	220	ns
			4.5	—	24	35	—	44	
			6.0	—	20	30	—	37	
Propagation delay time (INHIBIT-Sn)	t_{pLH} t_{pHL}	—	2.0	—	60	175	—	220	ns
			4.5	—	20	35	—	44	
			6.0	—	17	30	—	37	
Input capacitance	C_{IN}	—		—	5	10	—	10	pF
Power dissipation capacitance	C_{PD} (Note)	—		—	61	—	—	—	pF

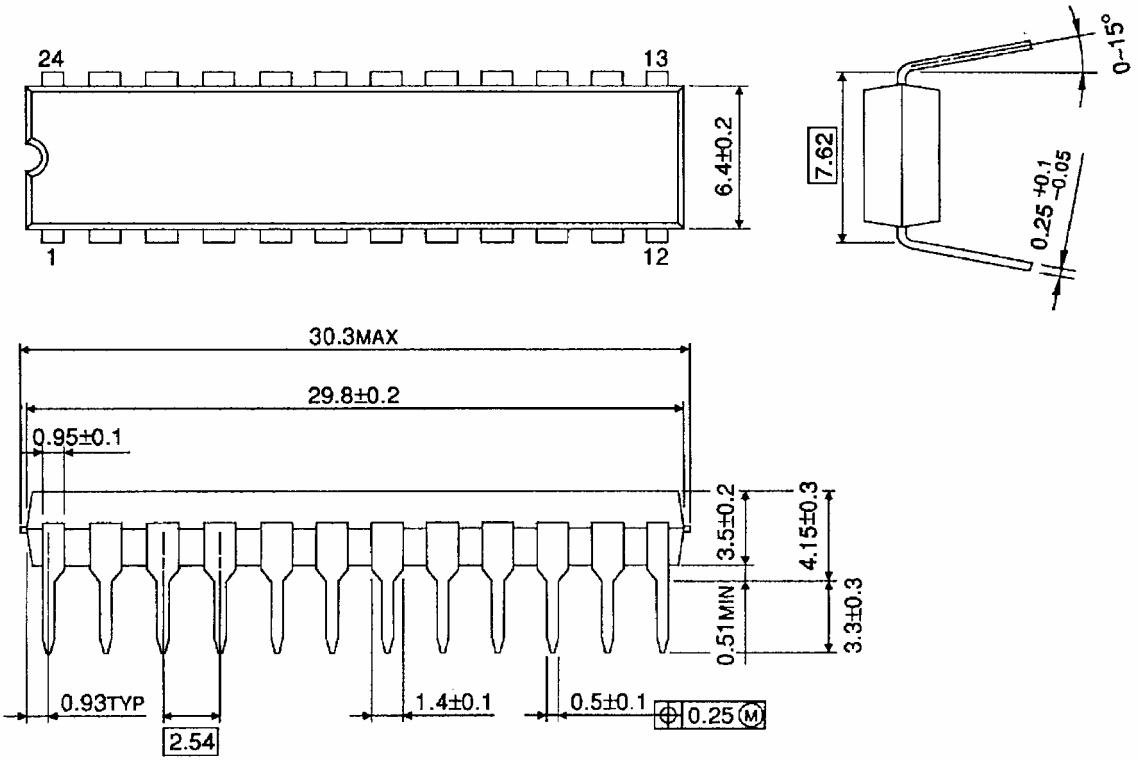
Note: C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.

Average operating current can be obtained by the equation:

$$I_{CC}\ (opr) = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$$

Package Dimensions

DIP24-P-300-2.54 Unit : mm



Weight: 1.50 g (typ.)

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20070701-EN GENERAL

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