

TC74HC191AP, TC74HC191AF

4 - BIT BINARY UP/DOWN COUNTER

The TC74HC191A are high speed CMOS 4-BIT UP/DOWN COUNTERs fabricated with silicon gate C²MOS technology. It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation. The TC74HC191A is 4-bit binary up/down counter.

They have a asynchronous load input (LOAD) which is active low.

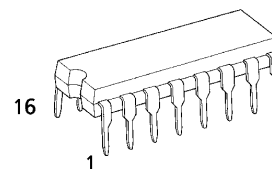
The direction of counting is determined by the level of DOWN/UP. When D/U is low, the counter counts up; when D/U is high, it counts down. Counting occurs on the positive going transition of the clock input.

Enable input (ENABLE) and two carry inputs (RIPPLE CLOCK OUT, MAX/MIN) are provided to permit easy cascading of the counters, which facilitates easy implementation of N-bit counters without using external gates.

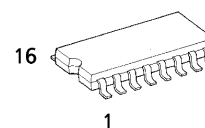
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES:

- High Speed..... $f_{MAX} = 48\text{MHz}$ (typ.)
at $V_{CC} = 5\text{V}$
- Low Power Dissipation..... $I_{CC} = 4\mu\text{A}$ (Max.) at $T_a = 25^\circ\text{C}$
- High Noise Immunity..... $V_{NIH} = V_{NIL} = 28\% V_{CC}$ (Min.)
- Output drive Capability.....10 LSTTL Loads
- Symmetrical Output Impedance... $|I_{OH}| = I_{OL} = 4\text{mA}$ (Min.)
- Balanced Propagation Delays..... $t_{PLH} \approx t_{PHL}$
- Wide Operating Voltage Range... V_{CC} (opr.) = $2\text{V} \sim 6\text{V}$
- Pin and Function Compatible with 74LS191

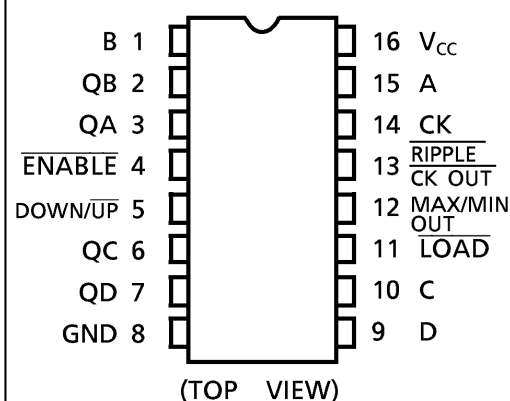


P (DIP16-P-300-2.54A)
Weight : 1.00g (Typ.)

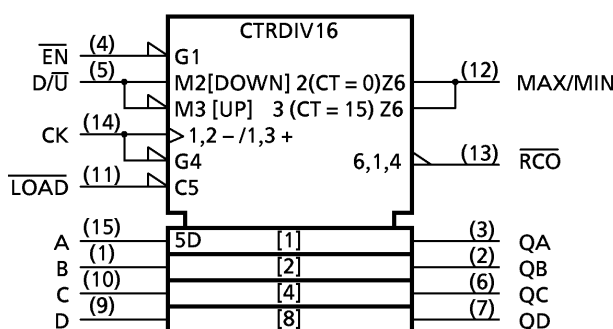


F (SOP16-P-300-1.27)
Weight : 0.18g (Typ.)

PIN ASSIGNMENT



IEC LOGIC SYMBOL

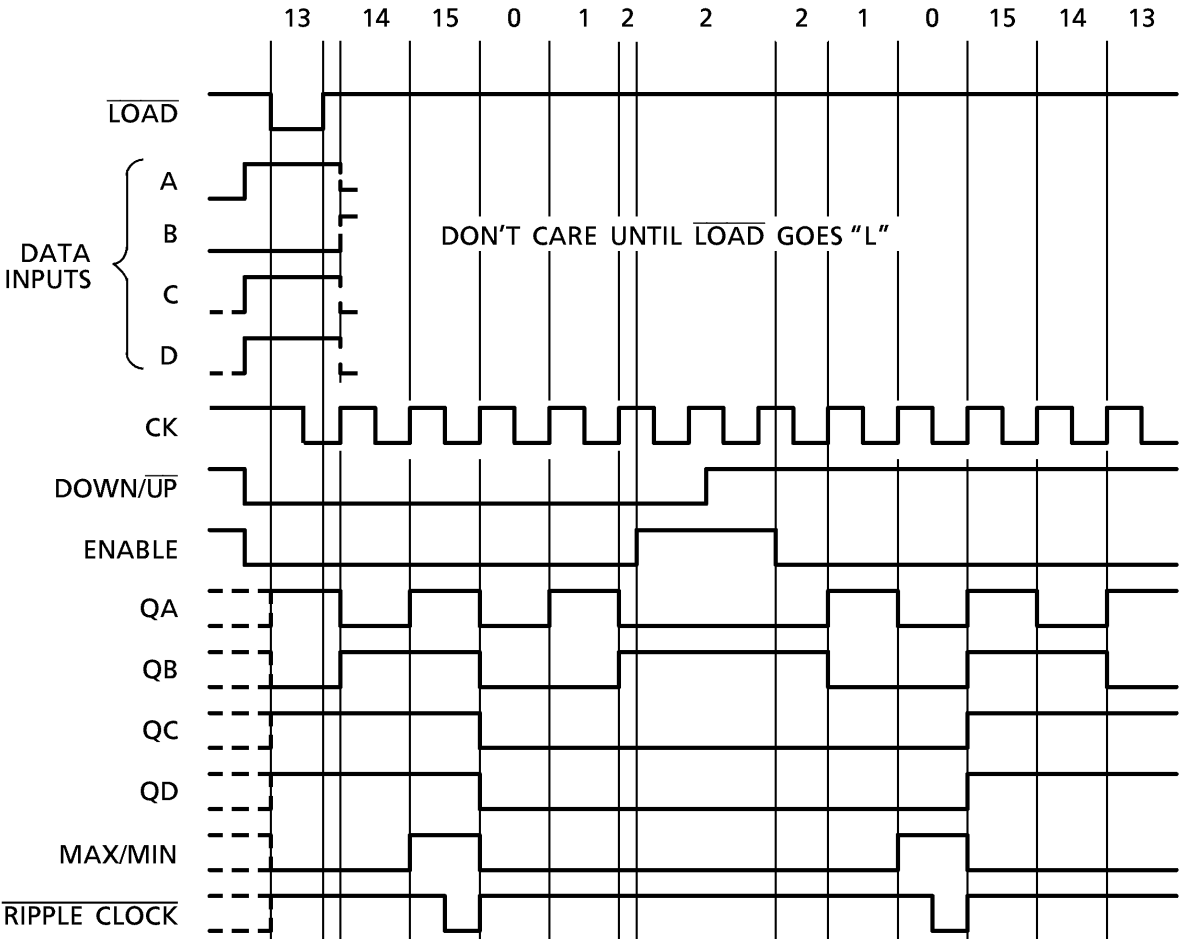


TRUTH TABLE

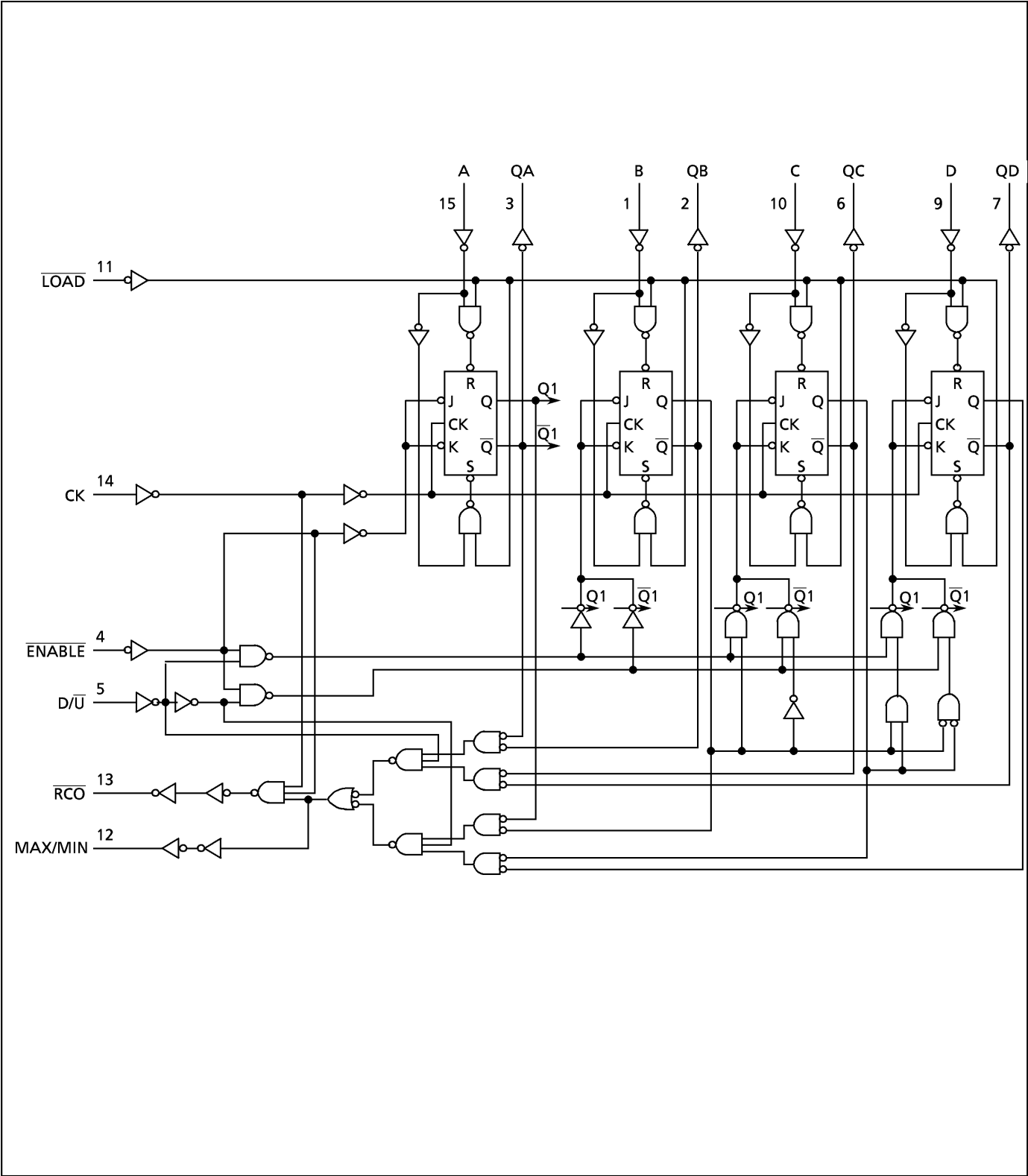
INPUTS				OUTPUTS				FUNCTION
LOAD	ENABLE	D/U	CK	QA	QB	QC	QD	
L	X	X	X	a	b	c	d	PRESET DATA
H	L	L	⬇	UP COUNT				UP COUNT
H	L	H	⬆	DOWN COUNT				DOWN COUNT
H	H	X	⬆	NO CHANGE				NO COUNT
H	X	X	⬇	NO CHANGE				NO COUNT

NOTE X : DON'T CARE
a ~ d : Inputs Level of A ~ D

TIMING CHART



SYSTEM DIAGRAM



ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	$-0.5 \sim 7$	V
DC Input Voltage	V_{IN}	$-0.5 \sim V_{CC} + 0.5$	V
DC Output Voltage	V_{OUT}	$-0.5 \sim V_{CC} + 0.5$	V
Input Diode Current	I_{IK}	± 20	mA
Output Diode Current	I_{OK}	± 20	mA
DC Output Current	I_{OUT}	± 25	mA
DC V_{CC} / Ground Current	I_{CC}	± 50	mA
Power Dissipation	P_D	500 (DIP)* / 180 (SOP)	mW
Storage Temperature	T_{stg}	$-65 \sim 150$	$^{\circ}\text{C}$

*500mW in the range of $T_a = -40^{\circ}\text{C} \sim 65^{\circ}\text{C}$. From $T_a = 65^{\circ}\text{C}$ to 85°C a derating factor of $-10\text{mW}/^{\circ}\text{C}$ shall be applied until 300mW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	$2 \sim 6$	V
Input Voltage	V_{IN}	$0 \sim V_{CC}$	V
Output Voltage	V_{OUT}	$0 \sim V_{CC}$	V
Operating Temperature	T_{opr}	$-40 \sim 85$	$^{\circ}\text{C}$
Input Rise and Fall Time	t_r, t_f	$0 \sim 1000 (V_{CC} = 2.0\text{V})$ $0 \sim 500 (V_{CC} = 4.5\text{V})$ $0 \sim 400 (V_{CC} = 6.0\text{V})$	ns

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION	V_{CC} (V)	$T_a = 25^{\circ}\text{C}$			$T_a = -40 \sim 85^{\circ}\text{C}$		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	
High - Level Input Voltage	V_{IH}		2.0 4.5 6.0	1.50 3.15 4.20	— — —	— — —	1.50 3.15 4.20	— — —	V
Low - Level Input Voltage	V_{IL}		2.0 4.5 6.0	— — —	— — —	0.50 1.35 1.80	— — —	0.50 1.35 1.80	V
High - Level Output Voltage	V_{OH}	$V_{IN} = V_{IH} \text{ or } V_{IL}$	$I_{OH} = -20\mu\text{A}$	2.0 4.5 6.0	1.9 4.4 5.9	2.0 4.5 6.0	— — —	1.9 4.4 5.9	V
			$I_{OH} = -4 \text{ mA}$	4.5 6.0	4.18 5.68	4.31 5.80	— —	4.13 5.63	
			$I_{OH} = -5.2 \text{ mA}$	6.0	5.68	—	5.63	—	
Low - Level Output Voltage	V_{OL}	$V_{IN} = V_{IH} \text{ or } V_{IL}$	$I_{OL} = 20\mu\text{A}$	2.0 4.5 6.0	— — —	0.0 0.0 0.0	0.1 0.1 0.1	— — —	V
			$I_{OL} = 4 \text{ mA}$	4.5 6.0	— —	0.17 0.18	0.26 0.26	— —	
			$I_{OL} = 5.2 \text{ mA}$	6.0	—	0.18	0.26	0.33 0.33	
Input Leakage Current	I_{IN}	$V_{IN} = V_{CC} \text{ or GND}$	6.0	—	—	± 0.1	—	± 1.0	μA
Quiescent Supply Current	I_{CC}	$V_{IN} = V_{CC} \text{ or GND}$	6.0	—	—	4.0	—	40.0	μA

TIMING REQUIREMENTS (Input $t_r = t_f = 6\text{ns}$)

PARAMETER	SYMBOL	TEST CONDITION	$V_{CC}(\text{V})$	$T_a = 25^\circ\text{C}$		$T_a = -40\sim 85^\circ\text{C}$	UNIT
				TYP.	LIMIT	LIMIT	
Minimum Pulse Width (CK)	$t_{W(H)}$ $t_{W(L)}$		2.0	—	100	125	ns
			4.5	—	20	25	
			6.0	—	17	21	
Minimum Pulse Width (LOAD)	$t_{W(L)}$		2.0	—	75	95	
			4.5	—	15	19	
			6.0	—	13	16	
Minimum Set-up Time ($\overline{\text{ENABLE}}$, D/ $\overline{\text{U}}$)	t_s		2.0	—	150	190	
			4.5	—	30	38	
			6.0	—	26	33	
Minimum Set-up Time (DATA—LOAD)	t_s		2.0	—	50	65	
			4.5	—	10	13	
			6.0	—	9	11	
Minimum Hold Time ($\overline{\text{ENABLE}}$, D/ $\overline{\text{U}}$)	t_h		2.0	—	0	0	
			4.5	—	0	0	
			6.0	—	0	0	
Minimum Hold Time (DATA—LOAD)	t_h		2.0	—	0	0	
			4.5	—	0	0	
			6.0	—	0	0	
Minimum Removal Time	t_{rem}		2.0	—	50	65	
			4.5	—	10	13	
			6.0	—	9	11	
Clock Frequency	f		2.0	—	5	4	MHz
			4.5	—	25	20	
			6.0	—	29	24	

AC ELECTRICAL CHARACTERISTICS ($C_L = 15\text{pF}$, $V_{CC} = 5\text{V}$, $T_a = 25^\circ\text{C}$, Input $t_r = t_f = 6\text{ns}$)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Output Transition Time	t_{TLH} t_{THL}		—	4	8	ns
Propagation Delay Time (CK—Q)	t_{PLH} t_{PHL}		—	18	31	
Propagation Delay Time (CK—RCO)	t_{PLH} t_{PHL}		—	10	20	
Propagation Delay Time (CK—MAX/MIN)	t_{PLH} t_{PHL}		—	23	42	
Propagation Delay Time (LOAD—Q)	t_{PLH} t_{PHL}		—	21	35	
Propagation Delay Time (DATA—Q)	t_{PLH} t_{PHL}		—	17	30	
Propagation Delay Time (ENABLE—RCO)	t_{PLH} t_{PHL}		—	11	17	
Propagation Delay Time (D/Ū—RCO)	t_{PLH} t_{PHL}		—	17	31	
Propagation Delay Time (D/Ū—MAX/MIN)	t_{PLH} t_{PHL}		—	15	27	
Maximum Clock Frequency	f_{MAX}		27	48	—	MHz

AC ELECTRICAL CHARACTERISTICS ($C_L = 50\text{pF}$, Input $t_r = t_f = 6\text{ns}$)

PARAMETER	SYMBOL	TEST CONDITION	$V_{CC}(\text{V})$	$T_a = 25^\circ\text{C}$			$T_a = -40\sim 85^\circ\text{C}$		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	
Output Transition Time	t_{TLH} t_{THL}		2.0	—	30	75	—	95	ns
			4.5	—	8	15	—	19	
			6.0	—	7	13	—	16	
Propagation Delay Time (CK—Q)	t_{pLH} t_{pHL}		2.0	—	88	180	—	225	
			4.5	—	22	36	—	45	
			6.0	—	19	31	—	38	
Propagation Delay Time (CK— $\overline{\text{RCO}}$)	t_{pLH} t_{pHL}		2.0	—	52	120	—	150	
			4.5	—	13	24	—	30	
			6.0	—	11	20	—	26	
Propagation Delay Time (CK—MAX/MIN)	t_{pLH} t_{pHL}		2.0	—	108	240	—	300	
			4.5	—	27	48	—	60	
			6.0	—	23	41	—	51	
Propagation Delay Time (LOAD—Q)	t_{pLH} t_{pHL}		2.0	—	100	205	—	255	
			4.5	—	25	41	—	51	
			6.0	—	22	35	—	43	
Propagation Delay Time (DATA—Q)	t_{pLH} t_{pHL}		2.0	—	84	175	—	220	
			4.5	—	21	35	—	44	
			6.0	—	18	30	—	37	
Propagation Delay Time (ENABLE— $\overline{\text{RCO}}$)	t_{pLH} t_{pHL}		2.0	—	56	105	—	130	
			4.5	—	14	21	—	26	
			6.0	—	12	18	—	22	
Propagation Delay Time ($\overline{\text{D/U}}$ — $\overline{\text{RCO}}$)	t_{pLH} t_{pHL}		2.0	—	84	180	—	225	
			4.5	—	21	36	—	45	
			6.0	—	18	31	—	38	
Propagation Delay Time ($\overline{\text{D/U}}$ —MAX/MIN)	t_{pLH} t_{pHL}		2.0	—	72	160	—	200	
			4.5	—	18	32	—	40	
			6.0	—	15	27	—	34	
Maximum Clock Frequency	f_{MAX}		2.0	5	11	—	4	—	MHz
			4.5	25	44	—	20	—	
			6.0	29	52	—	24	—	
Input Capacitance	C_{IN}			—	5	10	—	10	pF
Power Dissipation Capacitance	$C_{\text{PD}}(1)$			—	101	—	—	—	

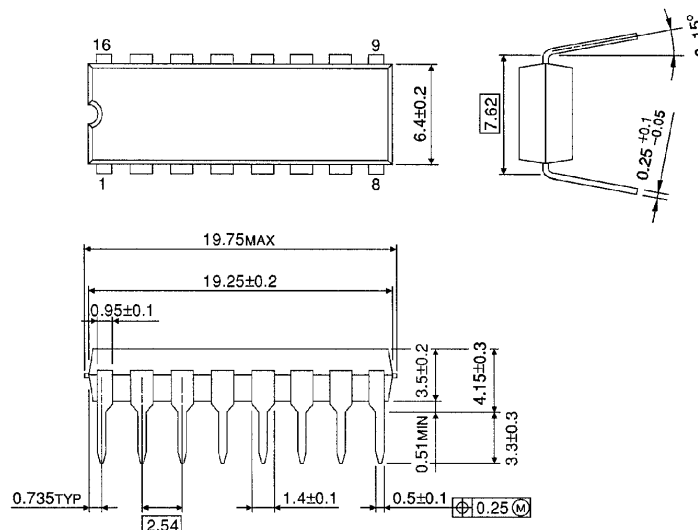
Note (1) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.

Average operating current can be obtained by the equation :

$$I_{\text{CC}}(\text{opr}) = C_{\text{PD}} \cdot V_{\text{CC}} \cdot f_{\text{IN}} + I_{\text{CC}}$$

DIP 16PIN PACKAGE DIMENSIONS (DIP16-P-300-2.54A)

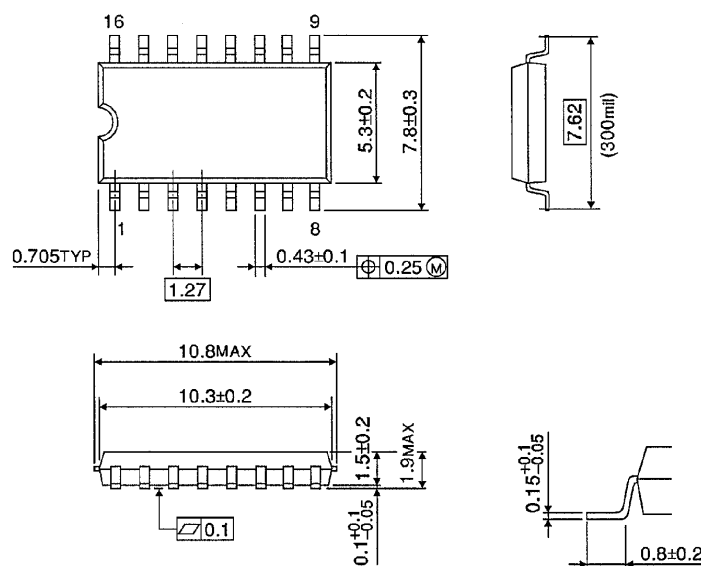
Unit in mm



Weight : 1.00g (Typ.)

SOP 16PIN (200mil BODY) PACKAGE DIMENSIONS (SOP16-P-300-1.27)

Unit in mm



Weight : 0.18g (Typ.)

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