

TOSHIBA CMOS Digital Integrated Circuit Silicon Monolithic

## TC74ACT161P,TC74ACT161F,TC74ACT161FN TC74ACT163P,TC74ACT163F,TC74ACT163FN

### Synchronous Presetable 4-Bit Binary Counter

TC74ACT161P/F/FN Asynchronous Clear

TC74ACT163P/F/FN Synchronous Clear

The TC74ACT161 and T163 are advanced high speed CMOS SYNCHRONOUS PRESETTABLE 4 BIT BINARY COUNTERs fabricated with silicon gate and double-layer metal wiring C<sup>2</sup>MOS technology.

They achieve the high speed operation similar to equivalent Bipolar Schottky TTL while maintaining the CMOS low power dissipation.

These devices may be used as a level converter for interfacing TTL or NMOS to High Speed CMOS. The inputs are compatible with TTL, NMOS and CMOS output voltage levels.

The CK input is active on the rising edge. Both LOAD and CLR inputs are active on low logic level.

Presetting of these IC's is synchronous to the rising edge of CK.

The clear function of the TC74ACT163 is synchronous to CK, while the TC74ACT161 are cleared asynchronously.

Two enable inputs (ENP and ENT) and CARRY OUTPUT are provided to enable easy cascading of counters, which facilitates easy implementation of n-bit counters without using external gates.

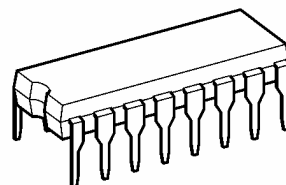
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

### Features

- High speed:  $f_{\max} = 110 \text{ MHz (typ.)}$  at  $V_{CC} = 5 \text{ V}$
- Low power dissipation:  $I_{CC} = 8 \mu\text{A (max)}$  at  $T_a = 25^\circ\text{C}$
- Compatible with TTL outputs:  $V_{IL} = 0.8 \text{ V (max)}$   
 $V_{IH} = 2.0 \text{ V (min)}$
- Symmetrical output impedance:  $|I_{OH}| = I_{OL} = 24 \text{ mA (min)}$   
Capability of driving  $50 \Omega$  transmission lines.
- Balanced propagation delays:  $t_{pLH} \approx t_{pHL}$
- Pin and function compatible with 74F161/163

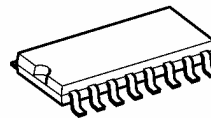
Note: xxxFN (JEDEC SOP) is not available in Japan.

TC74ACT161P, TC74ACT163P



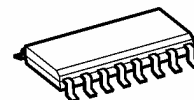
DIP16-P-300-2.54A

TC74ACT161F, TC74ACT163F



SOP16-P-300-1.27A

TC74ACT161FN, TC74ACT163FN

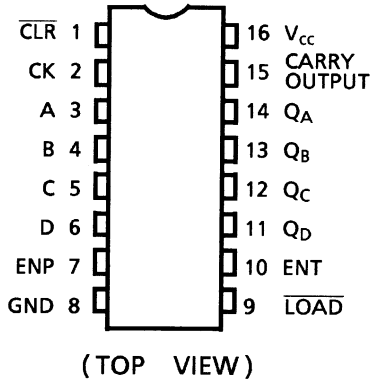


SOL16-P-150-1.27

#### Weight

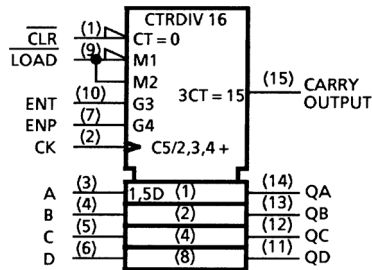
DIP16-P-300-2.54A	: 1.00 g (typ.)
SOP16-P-300-1.27A	: 0.18 g (typ.)
SOL16-P-150-1.27	: 0.13 g (typ.)

Pin Assignment

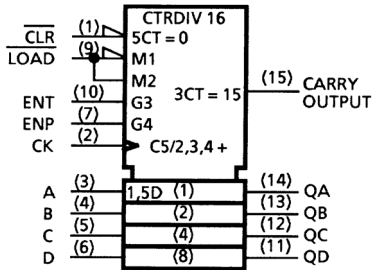


IEC Logic Symbol

TC74ACT161



TC74ACT163



Truth Table

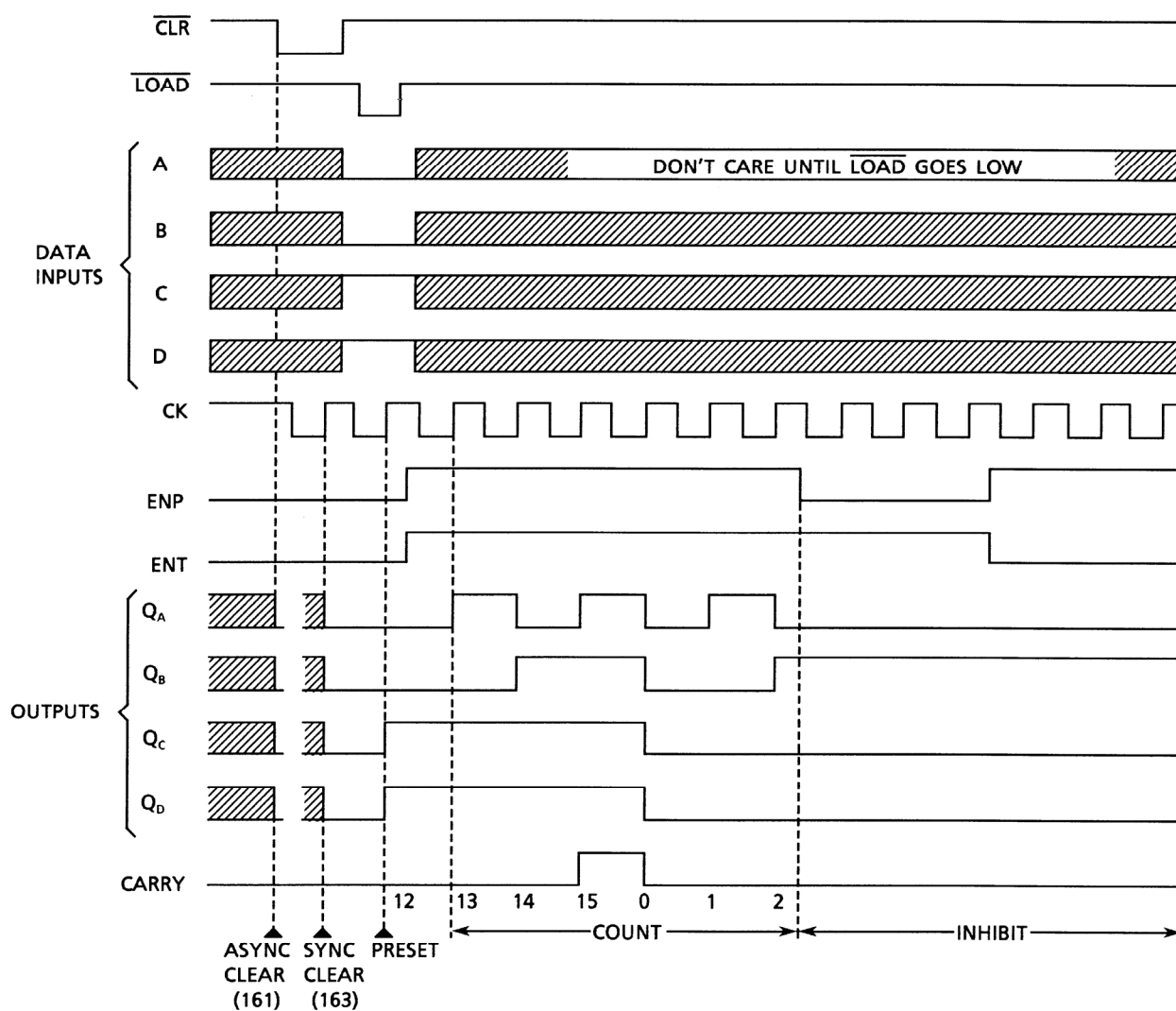
Inputs							Outputs				Function
CLR (161)	CLR (163)	LOAD	ENP	ENT	CK (161)	CK (163)	QA	QB	QC	QD	
L	L	X	X	X	X	↑	L	L	L	L	Reset to "0"
H	H	L	X	X	↑	↑	A	B	C	D	Preset Data
H	H	H	X	L	↑	↑	No Change				No Count
H	H	H	L	X	↑	↑	No Change				No Count
H	H	H	H	H	↑	↑	Count Up				Count
H	X	X	X	X	↓	↓	No Change				No Count

X: Don't care

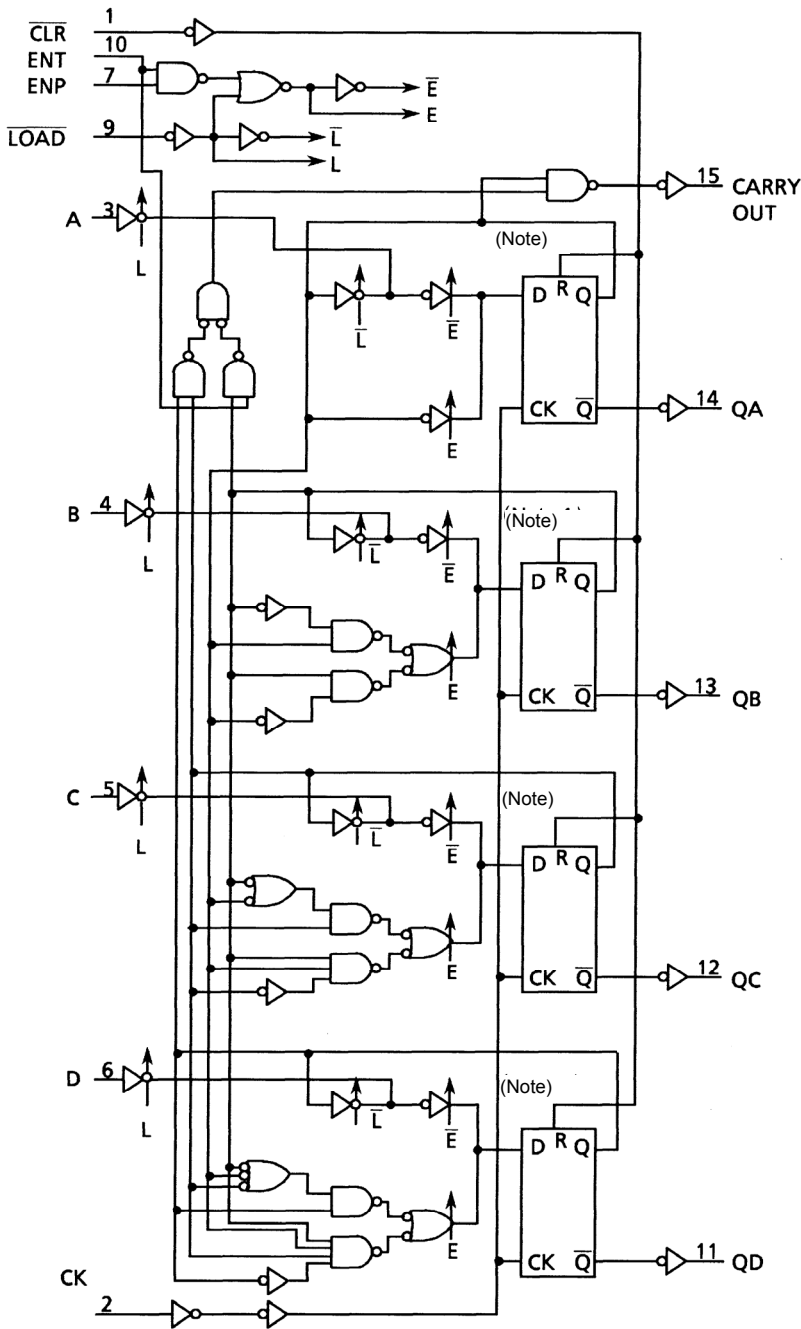
A, B, C, D: Logic level of data inputs

Carry: Carry = ENT · QA · QB · QC · QD

## Timing Chart



System Diagram (Note)



Note: Truth table of internal F/F

TC74ACT161					TC74ACT163				
D	CK	R	Q	$\bar{Q}$	D	CK	R	Q	$\bar{Q}$
X	X	H	L	H	X	$\uparrow$	H	L	H
L	$\uparrow$	L	L	H	L	$\uparrow$	L	L	H
H	$\uparrow$	L	H	L	X	$\uparrow$	L	H	L
X	$\downarrow$	L	No Change		X	$\downarrow$	L	No Change	

X: Don't care

**Absolute Maximum Ratings (Note 1)**

Characteristics	Symbol	Rating	Unit
Supply voltage range	$V_{CC}$	-0.5 to 7.0	V
DC input voltage	$V_{IN}$	-0.5 to $V_{CC} + 0.5$	V
DC output voltage	$V_{OUT}$	-0.5 to $V_{CC} + 0.5$	V
Input diode current	$I_{IK}$	$\pm 20$	mA
Output diode current	$I_{OK}$	$\pm 50$	mA
DC output current	$I_{OUT}$	$\pm 50$	mA
DC $V_{CC}$ /ground current	$I_{CC}$	$\pm 125$	mA
Power dissipation	$P_D$	500 (DIP) (Note 2)/180 (SOP)	mW
Storage temperature	$T_{stg}$	-65 to 150	°C

Note 1: Exceeding any of the absolute maximum ratings, even briefly, lead to deterioration in IC performance or even destruction.

Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings and the operating ranges.

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc.).

Note 2: 500 mW in the range of  $T_a = -40$  to  $65^\circ\text{C}$ . From  $T_a = 65$  to  $85^\circ\text{C}$  a derating factor of  $-10\text{ mW}/^\circ\text{C}$  should be applied up to 300 mW.

**Operating Ranges (Note)**

Characteristics	Symbol	Rating	Unit
Supply voltage	$V_{CC}$	4.5 to 5.5	V
Input voltage	$V_{IN}$	0 to $V_{CC}$	V
Output voltage	$V_{OUT}$	0 to $V_{CC}$	V
Operating temperature	$T_{opr}$	-40 to 85	°C
Input rise and fall time	$dt/dV$	0 to 10	ns/V

Note: The operating ranges must be maintained to ensure the normal operation of the device. Unused inputs must be tied to either VCC or GND.

**Electrical Characteristics**
**DC Characteristics**

Characteristics	Symbol	Test Condition			Ta = 25°C			Ta = −40 to 85°C		Unit	
				V <sub>CC</sub> (V)	Min	Typ.	Max	Min	Max		
High-level input voltage	V <sub>IH</sub>	—			4.5 to 5.5	2.0	—	—	2.0	—	V
Low-level input voltage	V <sub>IL</sub>	—			4.5 to 5.5	—	—	0.8	—	0.8	V
High-level output voltage	V <sub>OH</sub>	V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub>	I <sub>OH</sub> = −50 μA	4.5	4.4	4.5	—	4.4	—	V	
			I <sub>OH</sub> = −24 mA	4.5	3.94	—	—	3.80	—		
			I <sub>OH</sub> = −75 mA (Note)	5.5	—	—	—	3.85	—		
Low-level output voltage	V <sub>OL</sub>	V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub>	I <sub>OL</sub> = 50 μA	4.5	—	0.0	0.1	—	0.1	V	
			I <sub>OL</sub> = 24 mA	4.5	—	—	0.36	—	0.44		
			I <sub>OL</sub> = 75 mA (Note)	5.5	—	—	—	—	1.65		
Input leakage current	I <sub>IN</sub>	V <sub>IN</sub> = V <sub>CC</sub> or GND			5.5	—	—	±0.1	—	±1.0	μA
Quiescent supply current	I <sub>CC</sub>	V <sub>IN</sub> = V <sub>CC</sub> or GND			5.5	—	—	8.0	—	80.0	μA
	I <sub>C</sub>	Per input: V <sub>IN</sub> = 3.4 V Other input: V <sub>CC</sub> or GND			5.5	—	—	1.35	—	1.5	mA

Note: This spec indicates the capability of driving 50 Ω transmission lines.

One output should be tested at a time for a 10 ms maximum duration.

**Timing Requirements (input: t<sub>r</sub> = t<sub>f</sub> = 3 ns)**

Characteristics	Symbol	Test Condition		Ta = 25°C	Ta = -40 to 85°C	Unit
			VCC (V)	Limit	Limit	
Minimum pulse width (CK)	tW (L) tW (H)	Figure 1	5.0 ± 0.5	5.0	5.0	ns
Minimum pulse width ( $\overline{\text{CLR}}$ ) (Note1)	tW (L)	Figure 4	5.0 ± 0.5	5.0	5.0	ns
Minimum pulse width ( $\overline{\text{LOAD}}$ , ENP, ENT)	tS	Figure 2, Figure 3	5.0 ± 0.5	6.0	6.0	ns
Minimum set-up time (A, B, C, D)	tS	Figure 2	5.0 ± 0.5	4.0	4.0	ns
Minimum set-up time ( $\overline{\text{CLR}}$ ) (Note 2)	tS	Figure 5	5.0 ± 0.5	3.0	3.0	ns
Minimum hold time ( $\overline{\text{LOAD}}$ , ENP, ENT)	tH	Figure 2, Figure 3	5.0 ± 0.5	1.0	1.0	ns
Minimum hold time (A, B, C, D)	tH	Figure 2	5.0 ± 0.5	2.0	2.0	ns
Minimum hold time ( $\overline{\text{CLR}}$ ) (Note 2)	tH	Figure 5	5.0 ± 0.5	2.0	2.0	ns
Minimum removal time ( $\overline{\text{CLR}}$ ) (Note 1)	trem	Figure 4	5.0 ± 0.5	1.0	1.0	ns

Note 1: For TC74ACT161 only

Note 2: For TC74ACT163 only

## AC Characteristics (C<sub>L</sub> = 50 pF, R<sub>L</sub> = 500 Ω, input: t<sub>r</sub> = t<sub>f</sub> = 3 ns)

Characteristics	Symbol	Test Condition	Ta = 25°C				Ta = −40 to 85°C		Unit
			V <sub>CC</sub> (V)	Min	Typ.	Max	Min	Max	
Propagation delay time (CK-Q)	t <sub>pLH</sub> t <sub>pHL</sub>	Figure 1	5.0 ± 0.5	—	7.2	10.5	1.0	12.0	ns
Propagation delay time (CK-CARRY, count mode)	t <sub>pLH</sub> t <sub>pHL</sub>	Figure 1	5.0 ± 0.5	—	8.5	13.0	1.0	15.0	ns
Propagation delay time (CK-CARRY, preset mode)	t <sub>pLH</sub> t <sub>pHL</sub>	Figure 2	5.0 ± 0.5	—	9.7	15.0	1.0	17.0	ns
Propagation delay time (ENT-CARRY)	t <sub>pLH</sub> t <sub>pHL</sub>	Figure 6	5.0 ± 0.5	—	6.6	10.0	1.0	11.5	ns
Propagation delay time (Note 2) ( $\overline{\text{CLR}}$ -Q)	t <sub>pHL</sub>	Figure 4	5.0 ± 0.5	—	6.3	10.0	1.0	11.5	ns
Propagation delay time (Note 2) ( $\overline{\text{CLR}}$ -CARRY)	t <sub>pHL</sub>	Figure 4	5.0 ± 0.5	—	7.7	12.3	1.0	14.0	ns
Maximum clock frequency	f <sub>max</sub>	—	5.0 ± 0.5	70	100	—	60	—	MHz
Input capacitance	C <sub>IN</sub>	—	—	—	5	10	—	10	pF
Power dissipation capacitance	C <sub>PD</sub> (Note 1)	—	—	—	32	—	—	—	pF

Note 1: C<sub>PD</sub> is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.

Average operating current can be obtained by the equation:

$$I_{CC}(\text{opr}) = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$$

When the outputs drive a capacitive load, total current consumption is the sum of C<sub>PD</sub>, and ΔI<sub>CC</sub> which is obtained from the following formula:

$$\Delta I_{CC} = f_{CK} \cdot V_{CC} \left( \frac{C_{QA}}{2} + \frac{C_{QB}}{4} + \frac{C_{QC}}{8} + \frac{C_{QD}}{16} + \frac{C_{CO}}{16} \right)$$

C<sub>QA</sub>~C<sub>QD</sub> and C<sub>CO</sub> are the capacitances at QA~QD and CARRY OUT, respectively.

f<sub>CK</sub> is the input frequency of the CK.

Note 2: for TC74ACT161 only

## Switching Characteristics Test Waveform

### Count Mode

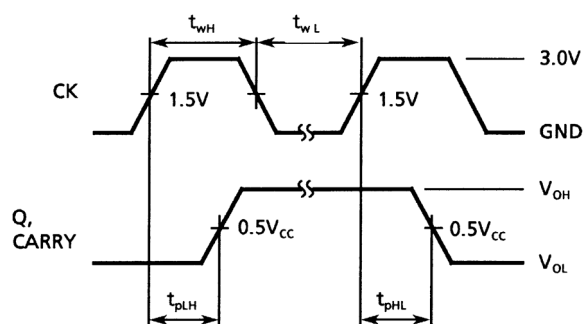


Figure 1

### Clear Mode (TC74ACT161)

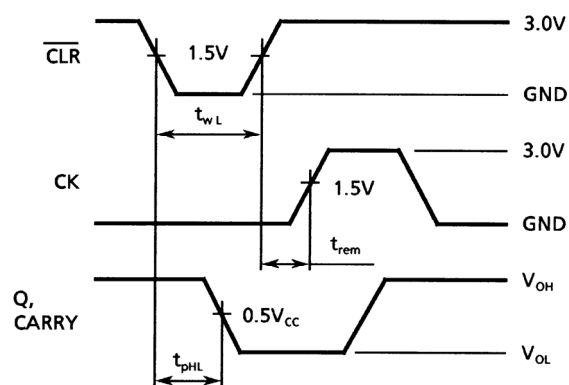


Figure 4

### Preset Mode

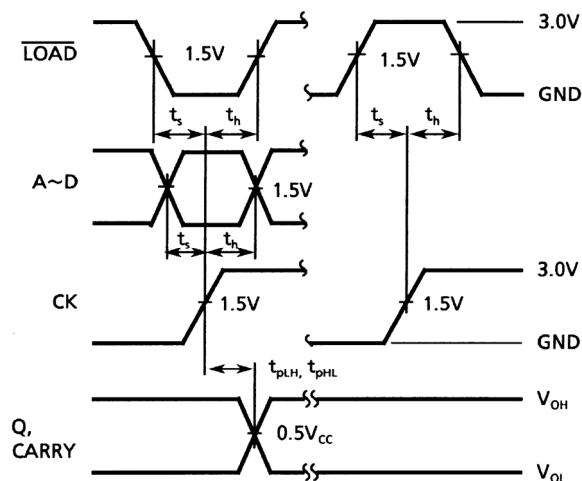


Figure 2

### Clear Mode (TC74ACT163)

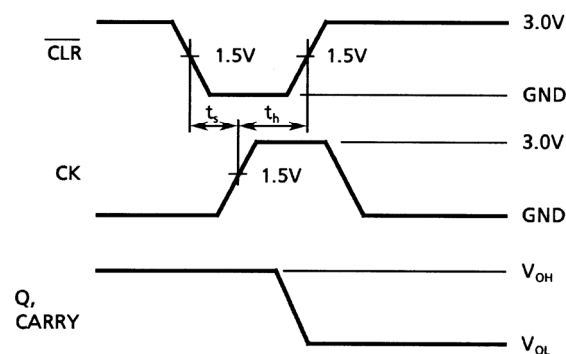


Figure 5

### Count Enable Mode

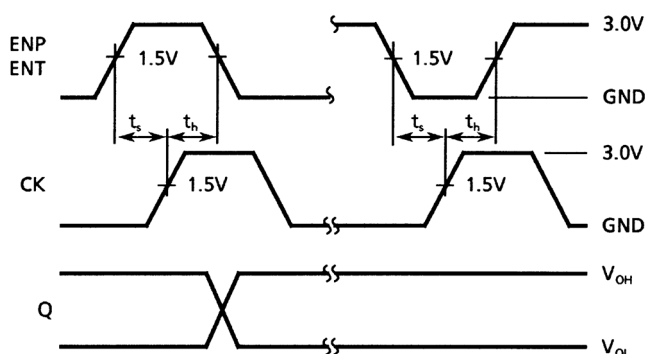


Figure 3

### Cascade Mode (fix maximum count)

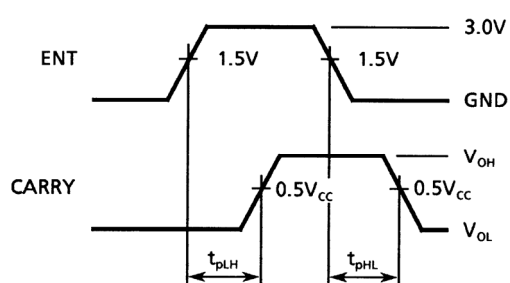
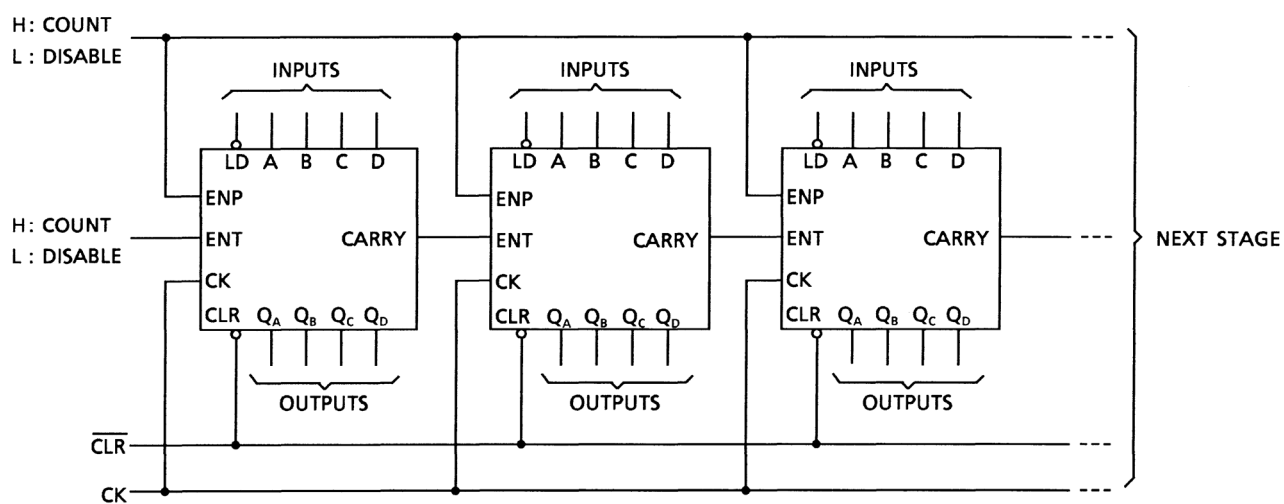


Figure 6

## Typical Application

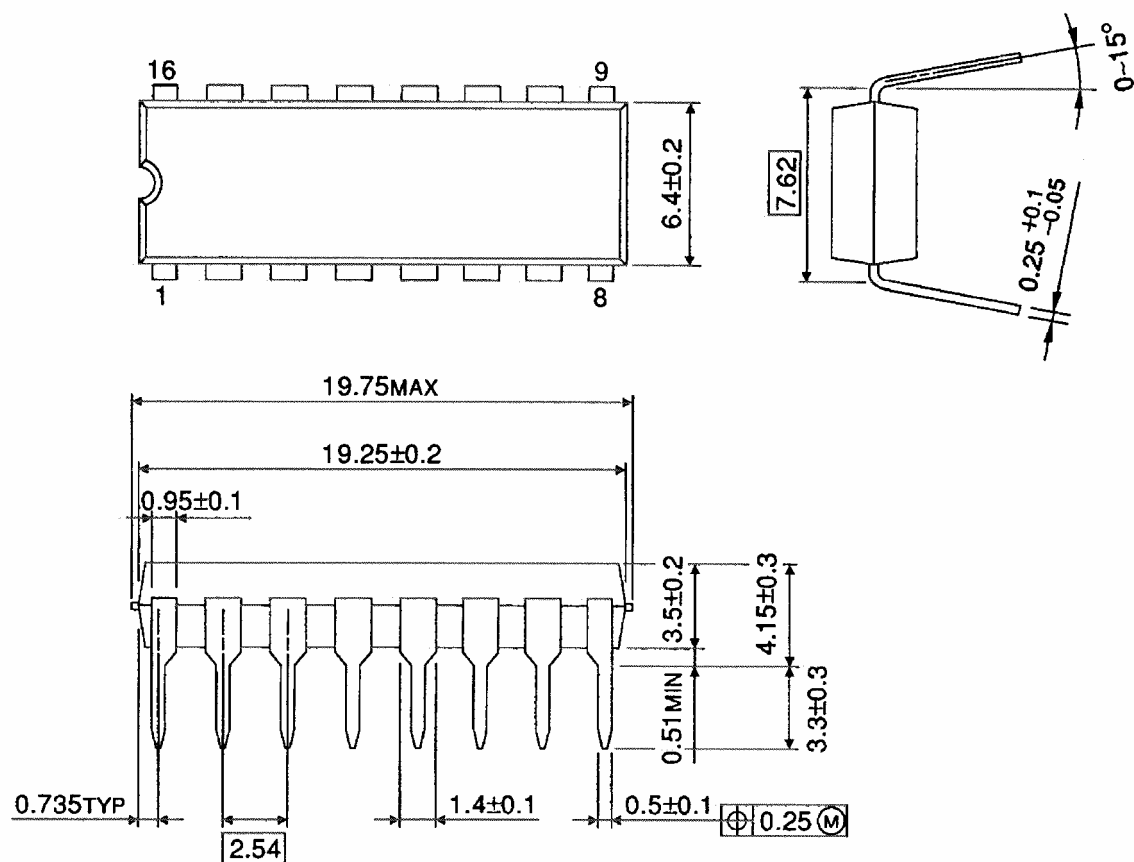
### Parallel Carry N-Bit Counter



## Package Dimensions

DIP16-P-300-2.54A

Unit : mm

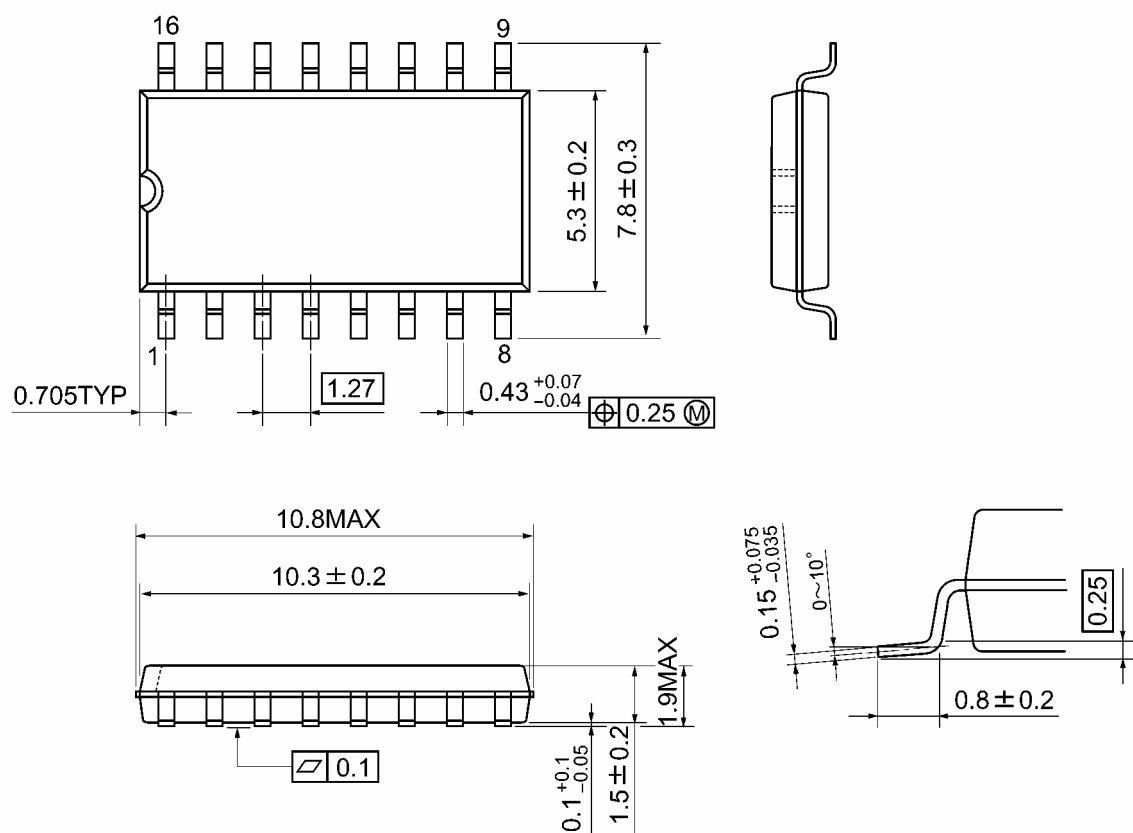


Weight: 1.00 g (typ.)

## Package Dimensions

SOP16-P-300-1.27A

Unit: mm

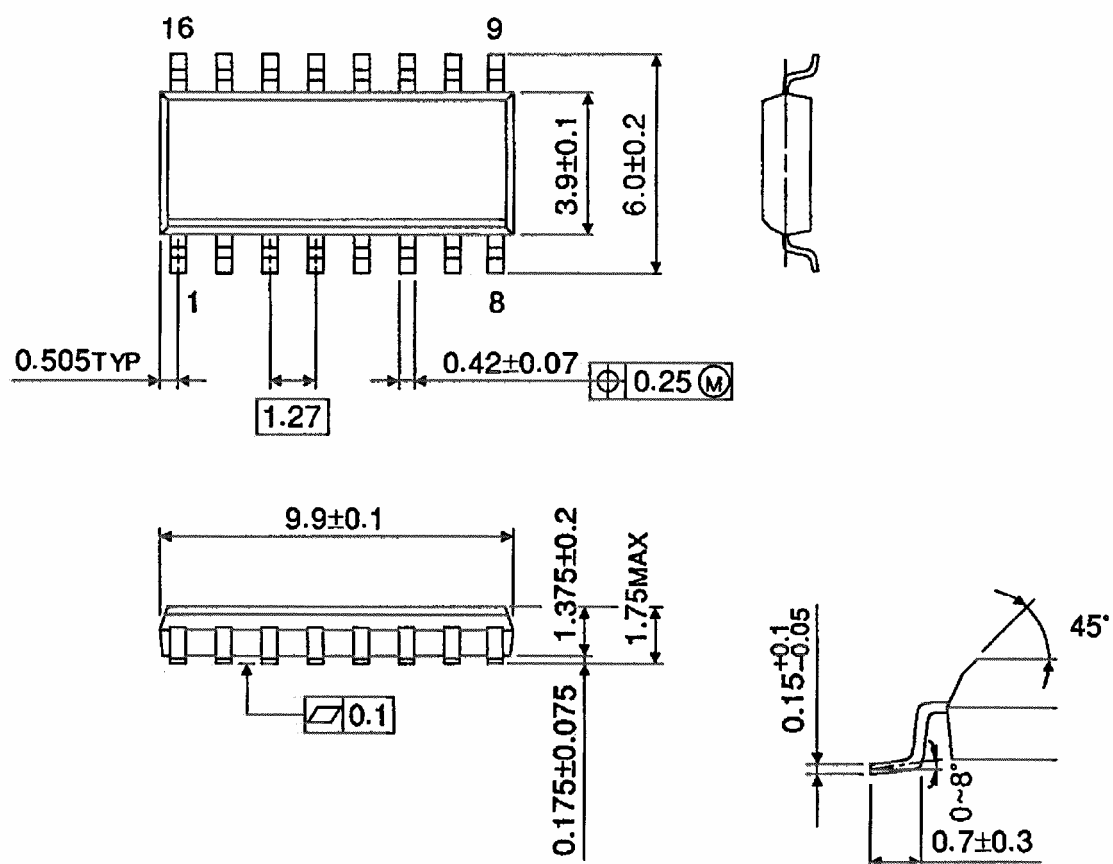


Weight: 0.18 g (typ.)

## Package Dimensions (Note)

SOL16-P-150-1.27

Unit : mm



Note: This package is not available in Japan.

Weight: 0.13 g (typ.)

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20070701-EN GENERAL

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