

## TC74AC390P, TC74AC390F, TC74AC390FN

### Dual Decade Counter

The TC74AC390 is an advanced high speed CMOS DUAL DECADE COUNTER fabricated with silicon gate and double-layer metal wiring C<sup>2</sup>MOS technology.

It achieves the high speed operation similar to equivalent Bipolar Schottky TTL while maintaining the CMOS low power dissipation.

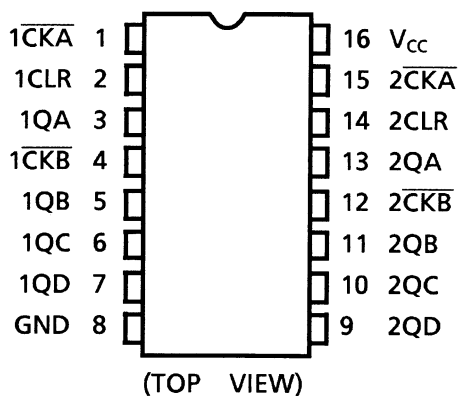
It consists of two independent 4-bit counters, each composed of a divide-by-two and a divide-by-five counter. The divide-by-two counter is incremented on the negative going transition of clock A ( $\overline{CKA}$ ). The divided-by-five counter is incremented on the negative going transition of clock B ( $\overline{CKB}$ ). The counter can be cascaded to form decade, bi-quinary, or various combinations up to a divide-by-100 counter. When the CLEAR input is set high, the Q outputs are set to low independent of the clock inputs.

All inputs are equipped with protection circuits against static discharge or transient excess voltage.

### Features

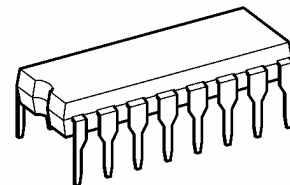
- High speed:  $f_{max} = 160$  MHz (typ.) at  $V_{CC} = 5$  V
- Low power dissipation:  $I_{CC} = 8$   $\mu$ A (max) at  $T_a = 25^\circ\text{C}$
- High noise immunity:  $V_{NIH} = V_{NIL} = 28\%$   $V_{CC}$  (min)
- Symmetrical output impedance:  $|I_{OH}| = I_{OL} = 24$  mA (min)  
Capability of driving 50  $\Omega$  transmission lines.
- Balanced propagation delays:  $t_{pLH} \approx t_{pHL}$
- Wide operating voltage range:  $V_{CC}$  (opr) = 2 to 5.5 V
- Pin and function compatible with 74HC390

### Pin Assignment



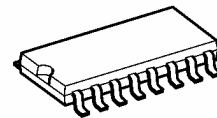
Note: xxxFN (JEDEC SOP) is not available in Japan.

TC74AC390P



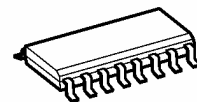
DIP16-P-300-2.54A

TC74AC390F



SOP16-P-300-1.27A

TC74AC390FN

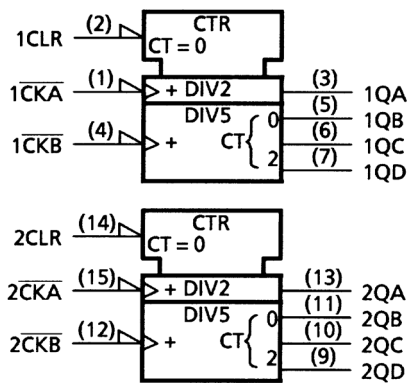


SOL16-P-150-1.27

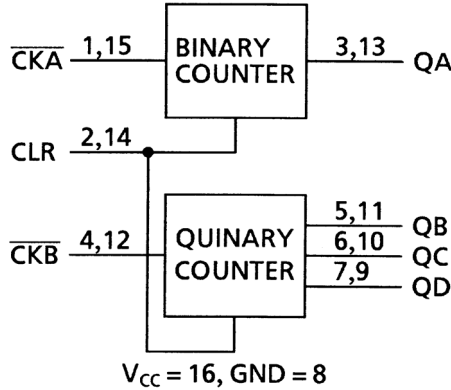
### Weight

DIP16-P-300-2.54A	: 1.00 g (typ.)
SOP16-P-300-1.27A	: 0.18 g (typ.)
SOL16-P-150-1.27	: 0.13 g (typ.)

IEC Logic Symbol



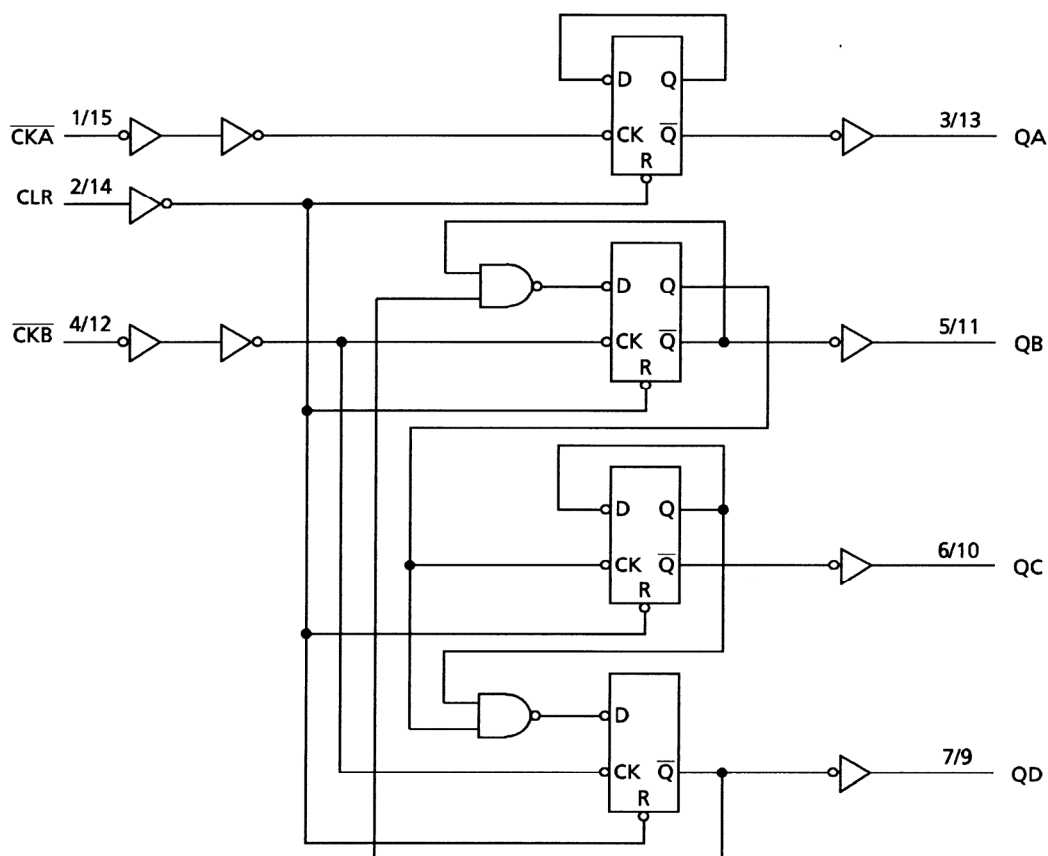
Block Daigram



Truth Table

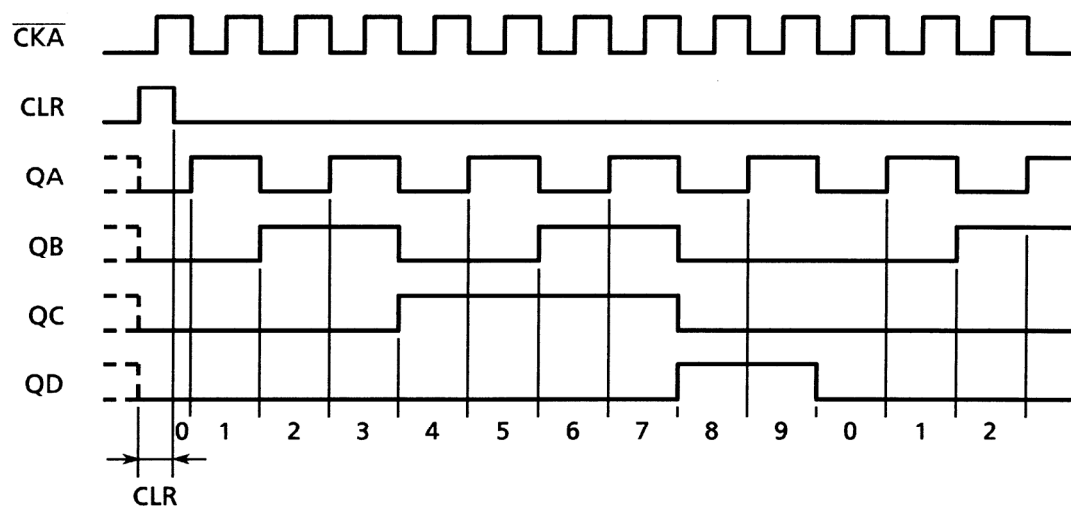
Inputs			Outputs			
CKA	CKB	CLR	QA	QB	QC	QD
X	X	H	L	L	L	L
	X	L	Binary Count Up			
X		L	Quinary Count Up			

## System Diagram



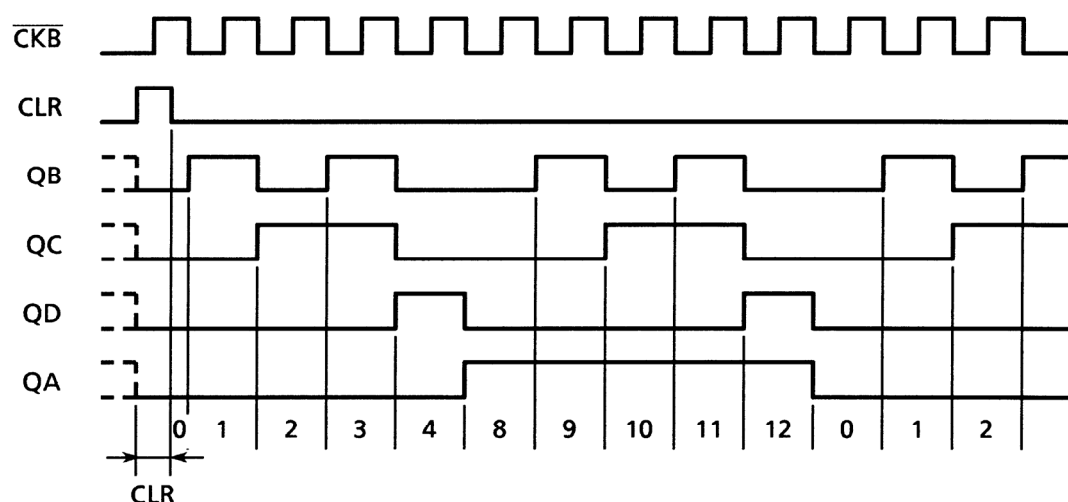
## Timing Chart

(1) BCD count sequence (Note)



Note:  $\text{QA}$  connected to  $\overline{\text{CKB}}$

## (2) Bi-quinary count sequence (Note)



Note: QD connected to  $\overline{CKA}$

## Absolute Maximum Ratings (Note 1)

Characteristics	Symbol	Rating	Unit
Supply voltage range	$V_{CC}$	-0.5 to 7.0	V
DC input voltage	$V_{IN}$	-0.5 to $V_{CC} + 0.5$	V
DC output voltage	$V_{OUT}$	-0.5 to $V_{CC} + 0.5$	V
Input diode current	$I_{IK}$	$\pm 20$	mA
Output diode current	$I_{OK}$	$\pm 50$	mA
DC output current	$I_{OUT}$	$\pm 50$	mA
DC $V_{CC}$ /ground current	$I_{CC}$	$\pm 200$	mA
Power dissipation	$P_D$	500 (DIP) (Note 2)/180 (SOP)	mW
Storage temperature	$T_{stg}$	-65 to 150	$^{\circ}\text{C}$

Note 1: Exceeding any of the absolute maximum ratings, even briefly, lead to deterioration in IC performance or even destruction.

Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings and the operating ranges.

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/Derating Concept and Methods) and individual reliability data (i.e. reliability test report and estimated failure rate, etc.).

Note 2: 500 mW in the range of  $T_a = -40$  to  $65^{\circ}\text{C}$ . From  $T_a = 65$  to  $85^{\circ}\text{C}$  a derating factor of  $-10$  mW/ $^{\circ}\text{C}$  should be applied up to 300 mW.

## Operating Ranges (Note)

Characteristics	Symbol	Rating	Unit
Supply voltage	$V_{CC}$	2.0 to 5.5	V
Input voltage	$V_{IN}$	0 to $V_{CC}$	V
Output voltage	$V_{OUT}$	0 to $V_{CC}$	V
Operating temperature	$T_{opr}$	-40 to 85	$^{\circ}\text{C}$
Input rise and fall time	$dt/dV$	0 to 100 ( $V_{CC} = 3.3 \pm 0.3$ V) 0 to 20 ( $V_{CC} = 5 \pm 0.5$ V)	ns/V

Note: The operating ranges must be maintained to ensure the normal operation of the device. Unused inputs must be tied to either  $V_{CC}$  or GND.

## Electrical Characteristics

## DC Characteristics

Characteristics	Symbol	Test Condition		Ta = 25°C			Ta = -40 to 85°C		Unit
				V <sub>CC</sub> (V)	Min	Typ.	Max	Min	Max
High-level input voltage	V <sub>IH</sub>	—		2.0 3.0 5.5	1.50 2.10 3.85	— — —	— — —	1.50 2.10 3.85	V
Low-level input voltage	V <sub>IL</sub>	—		2.0 3.0 5.5	— — —	— — —	0.50 0.90 1.65	— 0.90 1.65	V
High-level output voltage	V <sub>OH</sub>	V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub>	I <sub>OH</sub> = -50 µA	2.0 3.0 4.5	1.9 2.9 4.4	2.0 3.0 4.5	— — —	1.9 2.9 4.4	V
			I <sub>OH</sub> = -4 mA	3.0	2.58	—	—	2.48	
			I <sub>OH</sub> = -24 mA	4.5	3.94	—	—	3.80	
			I <sub>OH</sub> = -75 mA (Note)	5.5	—	—	—	3.85	
Low-level output voltage	V <sub>OL</sub>	V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub>	I <sub>OL</sub> = 50 µA	2.0 3.0 4.5	— — —	0.0 0.0 0.0	0.1 0.1 0.1	— — —	V
			I <sub>OL</sub> = 12 mA	3.0	—	—	0.36	—	
			I <sub>OL</sub> = 24 mA	4.5	—	—	0.36	—	
			I <sub>OL</sub> = 75 mA (Note)	5.5	—	—	—	—	
Input leakage current	I <sub>IN</sub>	V <sub>IN</sub> = V <sub>CC</sub> or GND		5.5	—	—	±0.1	—	µA
Quiescent supply current	I <sub>CC</sub>	V <sub>IN</sub> = V <sub>CC</sub> or GND		5.5	—	—	8.0	—	µA

Note: This spec indicates the capability of driving 50 Ω transmission lines.

One output should be tested at a time for a 10 ms maximum duration.

Timing Requirements (input: t<sub>r</sub> = t<sub>f</sub> = 3 ns)

Characteristics	Symbol	Test Condition	Ta = 25°C	Ta = -40 to 85°C	Unit
			V <sub>CC</sub> (V)	Limit	
Minimum pulse width ( $\overline{\text{CKA}}$ , $\overline{\text{CKB}}$ )	t <sub>W</sub> (H)	—	3.3 ± 0.3	7.0	ns
	t <sub>W</sub> (L)		5.0 ± 0.5	5.0	
Minimum pulse width (CLR)	t <sub>W</sub> (H)	—	3.3 ± 0.3	7.0	ns
			5.0 ± 0.5	5.0	
Minimum removal time	t <sub>rem</sub>	—	3.3 ± 0.3	7.0	ns
			5.0 ± 0.5	3.5	

**AC Characteristics ( $C_L = 50 \text{ pF}$ ,  $R_L = 500 \Omega$ , input:  $t_r = t_f = 3 \text{ ns}$ )**

Characteristics	Symbol	Test Condition	Ta = 25°C				Ta = -40 to 85°C		Unit
			V <sub>CC</sub> (V)	Min	Typ.	Max	Min	Max	
Propagation delay time ( $\overline{\text{CKA}}$ -QA)	t <sub>pLH</sub> t <sub>pHL</sub>	—	3.3 ± 0.3 5.0 ± 0.5	— —	8.2 5.5	14.0 8.4	1.0 1.0	16.0 9.6	ns
Propagation delay time ( $\overline{\text{CKA}}$ -QC)	t <sub>pLH</sub> t <sub>pHL</sub>	QA connected to $\overline{\text{CKB}}$	3.3 ± 0.3 5.0 ± 0.5	— —	17.0 10.5	30.0 17.5	1.0 1.0	34.0 20.0	ns
Propagation delay time ( $\overline{\text{CKB}}$ -QB, QD)	t <sub>pLH</sub> t <sub>pHL</sub>	—	3.3 ± 0.3 5.0 ± 0.5	— —	8.8 6.0	14.9 9.4	1.0 1.0	17.0 10.7	ns
Propagation delay time ( $\overline{\text{CKB}}$ -QC)	t <sub>pLH</sub> t <sub>pHL</sub>	—	3.3 ± 0.3 5.0 ± 0.5	— —	11.0 7.1	18.8 11.3	1.0 1.0	21.5 12.8	ns
Propagation delay time (CLR-Qn)	t <sub>pHL</sub>	—	3.3 ± 0.3 5.0 ± 0.5	— —	7.7 5.7	12.5 8.5	1.0 1.0	14.3 9.7	ns
Maximum clock frequency ( $\overline{\text{CKA}}$ )	f <sub>max</sub>	—	3.3 ± 0.3 5.0 ± 0.5	60 100	120 180	— —	60 100	— —	MHz
Maximum clock frequency ( $\overline{\text{CKB}}$ )	f <sub>max</sub>	—	3.3 ± 0.3 5.0 ± 0.5	45 90	90 140	— —	45 90	— —	MHz
Input capacitance	C <sub>IN</sub>	—		—	5	10	—	10	pF
Power dissipation capacitance	C <sub>PD</sub> (Note)	—		—	40	—	—	—	pF

Note:  $C_{\text{PD}}$  is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.

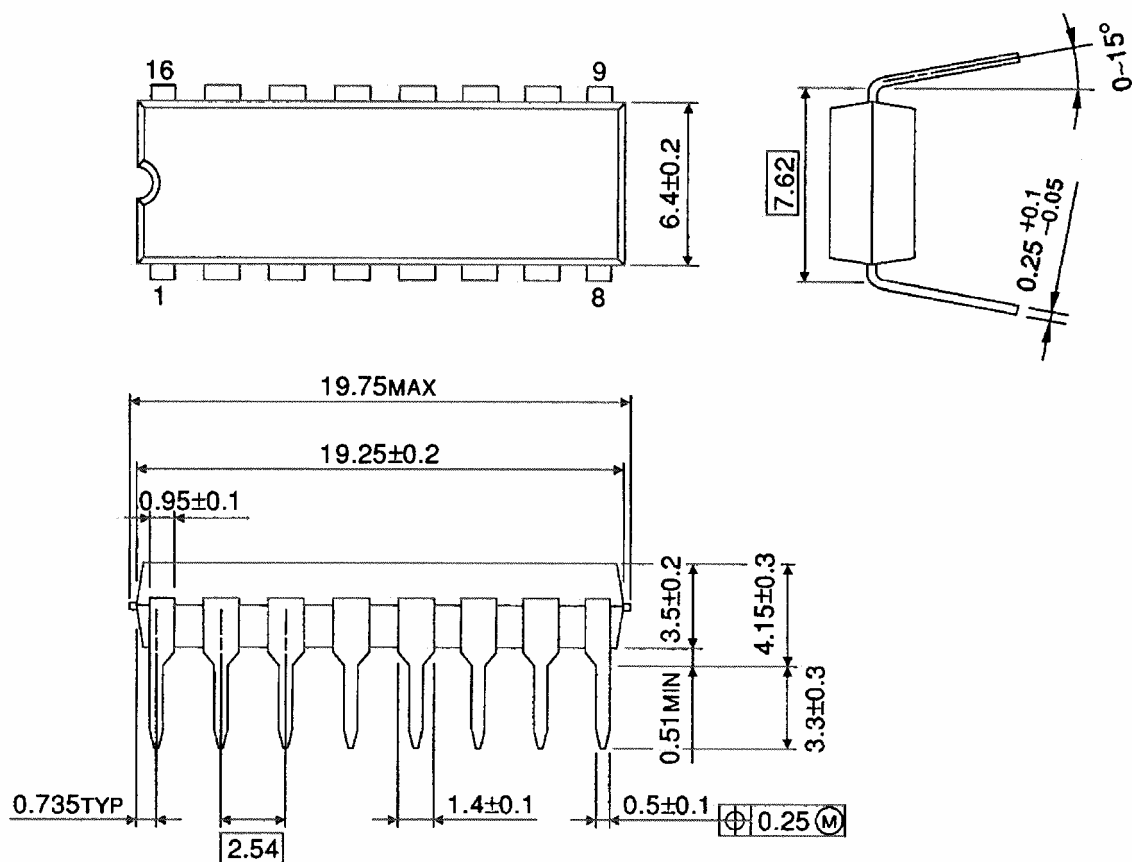
Average operating current can be obtained by the equation:

$$I_{\text{CC (opr)}} = C_{\text{PD}} \cdot V_{\text{CC}} \cdot f_{\text{IN}} + I_{\text{CC}}/2 \text{ (per counter)}$$

## Package Dimensions

DIP16-P-300-2.54A

Unit : mm

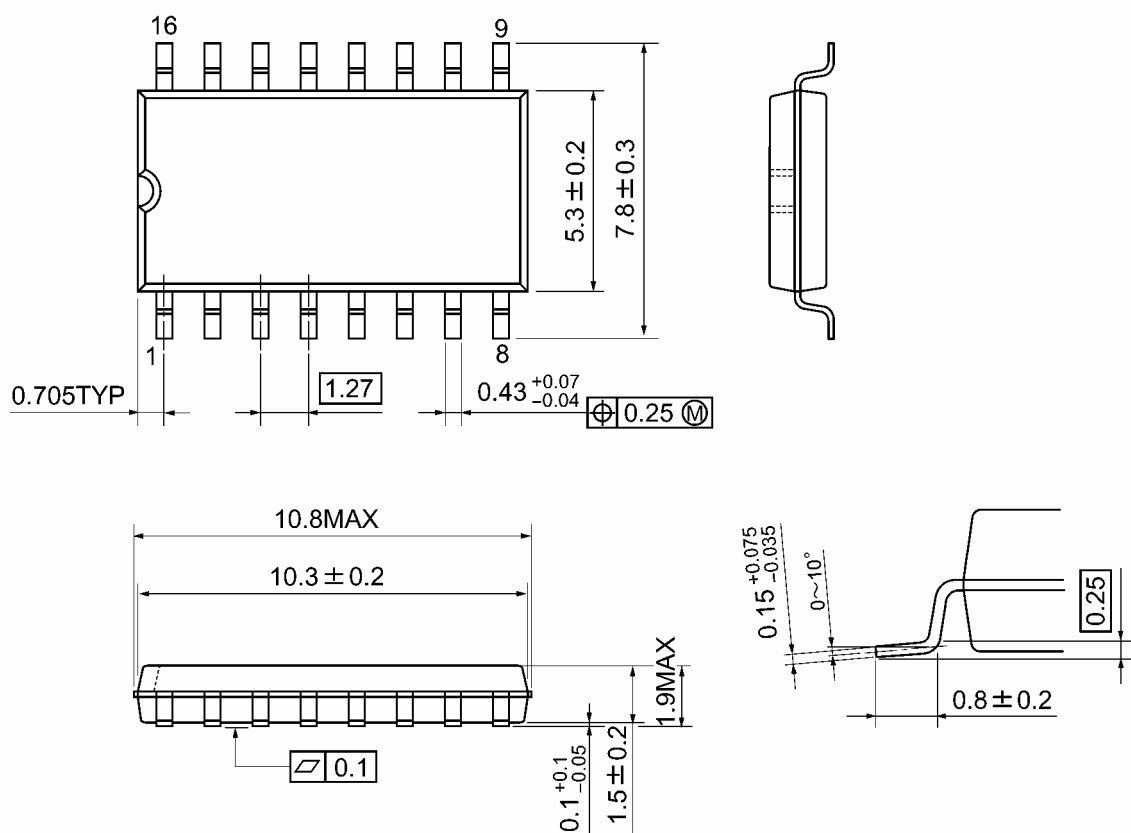


Weight: 1.00 g (typ.)

## Package Dimensions

SOP16-P-300-1.27A

Unit: mm



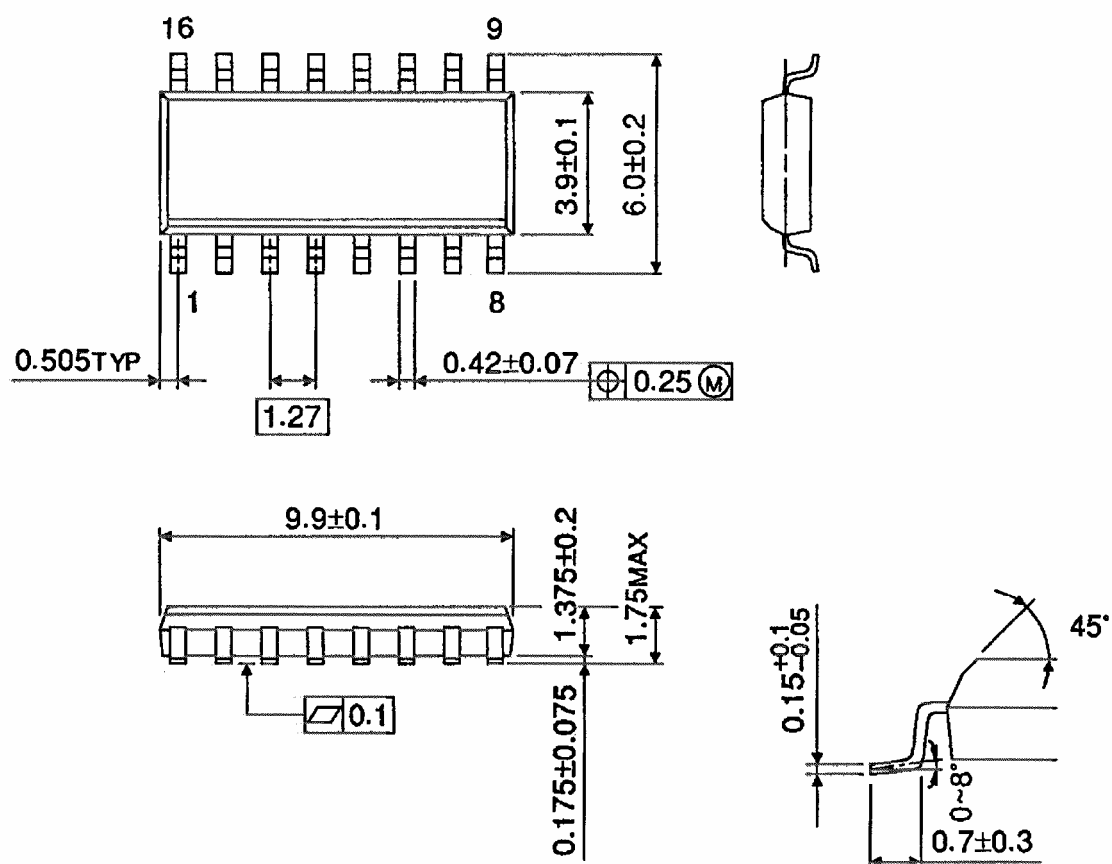
Weight: 0.18 g (typ.)



## Package Dimensions (Note)

SOL16-P-150-1.27

Unit : mm



Note: This package is not available in Japan.

Weight: 0.13 g (typ.)

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20070701-EN GENERAL

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