

TC74AC157P, TC74AC157F, TC74AC157FN, TC74AC157FT

QUAD 2-CHANNEL MULTIPLEXER

The TC74AC157 is an advanced high speed CMOS QUAD 2-CHANNEL MULTIPLEXER fabricated with silicon gate and double-layer metal wiring C²MOS technology.

It achieves the high speed operation similar to equivalent Bipolar Schottky TTL while maintaining the CMOS low power dissipation.

This device consists of four 2-input digital multiplexer with common select and strobe inputs.

When the **STROBE** input is held "H" level, selection of data is inhibited and all the outputs become "L" level.

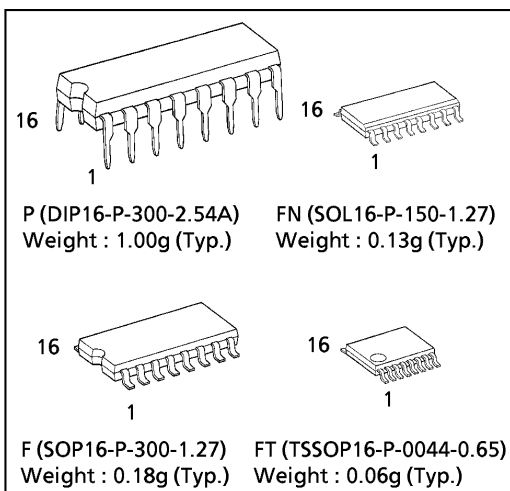
The **SELECT** decoding determines whether the A or B inputs get routed to their corresponding Y outputs.

All inputs are equipped with protection circuits against static discharge or transient excess voltage.

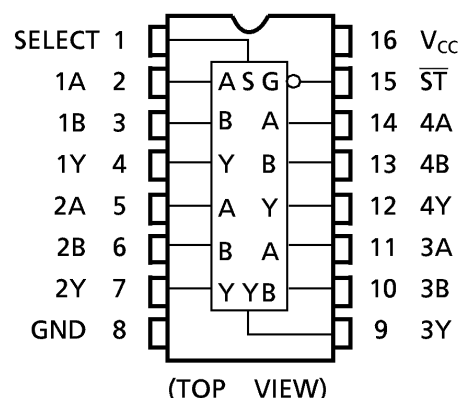
FEATURES:

- High Speed..... $t_{pd} = 4.5\text{ns}(\text{typ.})$ at $V_{CC} = 5\text{V}$
- Low Power Dissipation..... $I_{CC} = 8\mu\text{A}(\text{Max.})$ at $T_a = 25^\circ\text{C}$
- High Noise Immunity..... $V_{NIH} = V_{NIL} = 28\% V_{CC}(\text{Min.})$
- Symmetrical Output Impedance... $|I_{OH}| = I_{OL} = 24\text{mA}(\text{Min.})$
Capability of driving 50Ω transmission lines.
- Balanced Propagation Delays..... $t_{pLH} \approx t_{pHL}$
- Wide Operating Voltage Range... $V_{CC}(\text{opr}) = 2\text{V} \sim 5.5\text{V}$
- Pin and Function Compatible with 74F157

(Note) The JEDEC SOP (FN) is not available in Japan.



PIN ASSIGNMENT

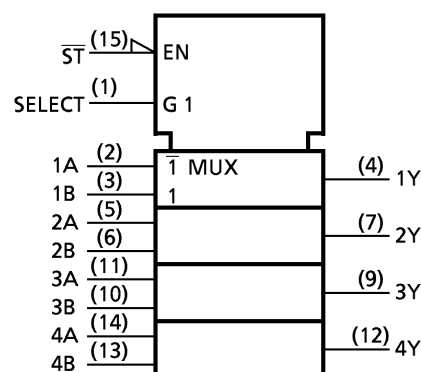


TRUTH TABLE

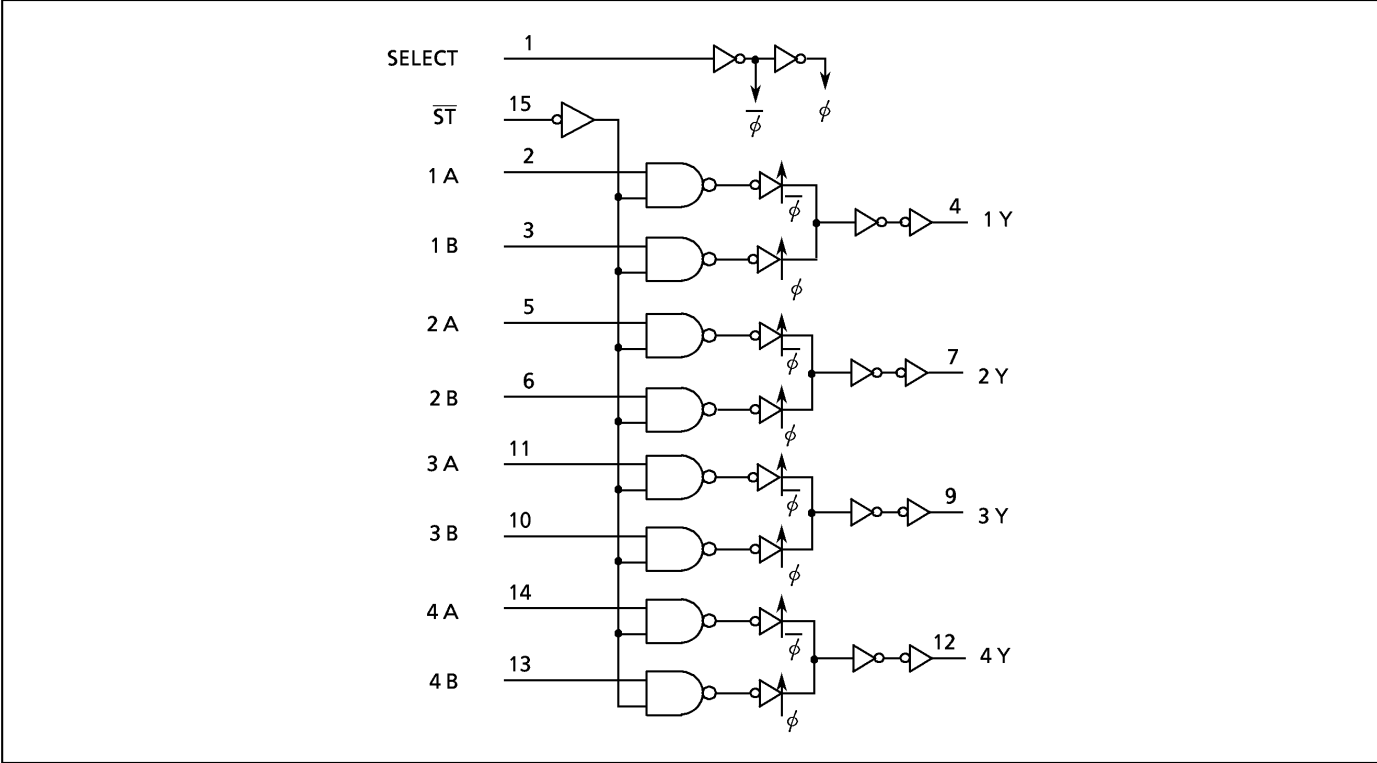
INPUTS				OUTPUTS
$\overline{ST}$	SELECT	A	B	Y
H	X	X	X	L
L	L	L	X	L
L	L	H	X	H
L	H	X	L	L
L	H	X	H	H

X : Don't Care

IEC LOGIC SYMBOL



SYSTEM DIAGRAM



ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	$-0.5 \sim 7.0$	V
DC Input Voltage	V_{IN}	$-0.5 \sim V_{CC} + 0.5$	V
DC Output Voltage	V_{OUT}	$-0.5 \sim V_{CC} + 0.5$	V
Input Diode Current	I_{IK}	± 20	mA
Output Diode Current	I_{OK}	± 50	mA
DC Output Current	I_{OUT}	± 50	mA
DC V_{CC} /Ground Current	I_{CC}	± 100	mA
Power Dissipation	P_D	500 (DIP)*/180 (SOP/TSSOP)	mW
Storage Temperature	T_{stg}	$-65 \sim 150$	$^{\circ}C$

*500mW in the range of $T_a = -40^{\circ}C \sim 65^{\circ}C$. From $T_a = 65^{\circ}C$ to $85^{\circ}C$ a derating factor of $-10mW/^{\circ}C$ should be applied up to 300mW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	2.0~5.5	V
Input Voltage	V_{IN}	0~ V_{CC}	V
Output Voltage	V_{OUT}	0~ V_{CC}	V
Operating Temperature	T_{opr}	$-40 \sim 85$	$^{\circ}C$
Input Rise and Fall Time	dt/dV	0~100 ($V_{CC} = 3.3 \pm 0.3V$) 0~20 ($V_{CC} = 5 \pm 0.5V$)	ns/V

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION	V _{CC} (V)	Ta = 25°C			Ta = -40~85°C		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	
High - Level Input Voltage	V _{IH}		2.0 3.0 5.5	1.50 2.10 3.85	— — —	— — —	1.50 2.10 3.85	— — —	V
Low - Level Input Voltage	V _{IL}		2.0 3.0 5.5	— — —	— — —	0.50 0.90 1.65	— — —	0.50 0.90 1.65	V
High - Level Output Voltage	V _{OH}	V _{IN} = V _{IH} or V _{IL}	I _{OH} = -50μA 3.0 4.5	2.0 2.9 4.4	2.0 3.0 4.5	— — —	1.9 2.9 4.4	— — —	V
				I _{OH} = -4mA	—	—	2.48	—	
				I _{OH} = -24mA	—	—	3.80	—	
				I _{OH} = -75mA*	—	—	3.85	—	
Low - Level Output Voltage	V _{OL}	V _{IN} = V _{IH} or V _{IL}	I _{OL} = 50μA 3.0 4.5	2.0 — —	0.0 0.0 0.0	0.1 0.1 0.1	— — —	0.1 0.1 0.1	V
				I _{OL} = 12mA	—	—	0.36	—	
				I _{OL} = 24mA	—	—	0.36	—	
				I _{OL} = 75mA*	—	—	—	—	
Input Leakage Current	I _{IN}	V _{IN} = V _{CC} or GND	5.5	—	—	± 0.1	—	± 1.0	μA
Quiescent Supply Current	I _{CC}	V _{IN} = V _{CC} or GND	5.5	—	—	8.0	—	80.0	

* : This spec indicates the capability of driving 50Ω transmission lines.
One output should be tested at a time for a 10ms maximum duration.

AC ELECTRICAL CHARACTERISTICS (C_L = 50pF, R_L = 500Ω, Input t_r = t_f = 3ns)

PARAMETER	SYMBOL	TEST CONDITION	V _{CC} (V)	Ta = 25°C			Ta = -40~85°C		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	
Propagation Delay Time (A, B-Y)	t _{pLH} t _{pHL}		3.3 ± 0.3	—	7.2	12.2	1.0	14.0	ns
			5.0 ± 0.5	—	5.5	7.9	1.0	9.1	
Propagation Delay Time (SELECT-Y)	t _{pLH} t _{pHL}		3.3 ± 0.3	—	8.5	14.5	1.0	16.7	
			5.0 ± 0.5	—	6.3	9.1	1.0	10.5	
Propagation Delay Time ($\overline{ST}$ -Y)	t _{pLH} t _{pHL}		3.3 ± 0.3	—	8.6	14.6	1.0	16.8	
			5.0 ± 0.5	—	6.4	9.2	1.0	10.6	
Input Capacitance	C _{IN}			—	5	10	—	10	pF
Power Dissipation Capacitance	C _{PD} (1)			—	93	—	—	—	

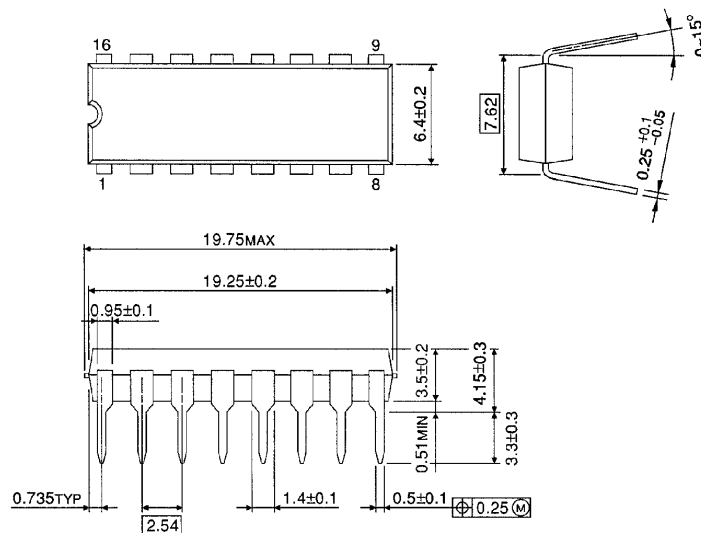
Note (1) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.

Average operating current can be obtained by the equation :

$$I_{CC}(\text{opr.}) = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/4 \text{ (per bit)}$$

DIP 16PIN PACKAGE DIMENSIONS (DIP16-P-300-2.54A)

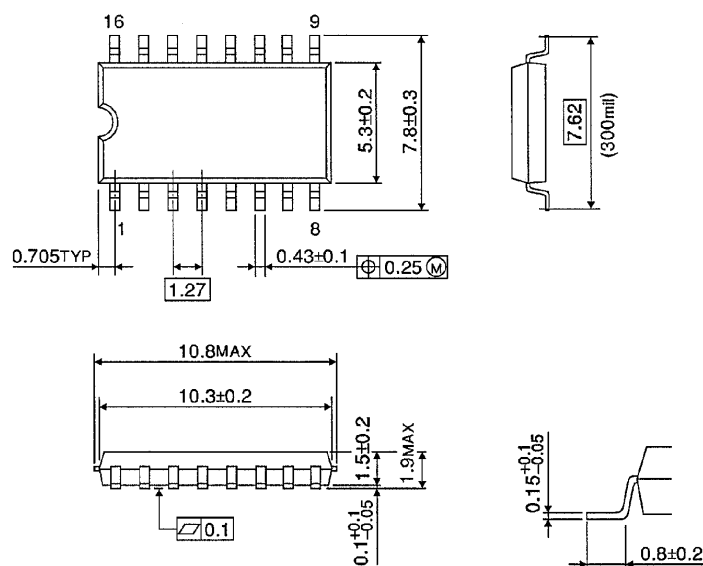
Unit in mm



Weight : 1.00g (Typ.)

SOP 16PIN (200mil BODY) PACKAGE DIMENSIONS (SOP16-P-300-1.27)

Unit in mm

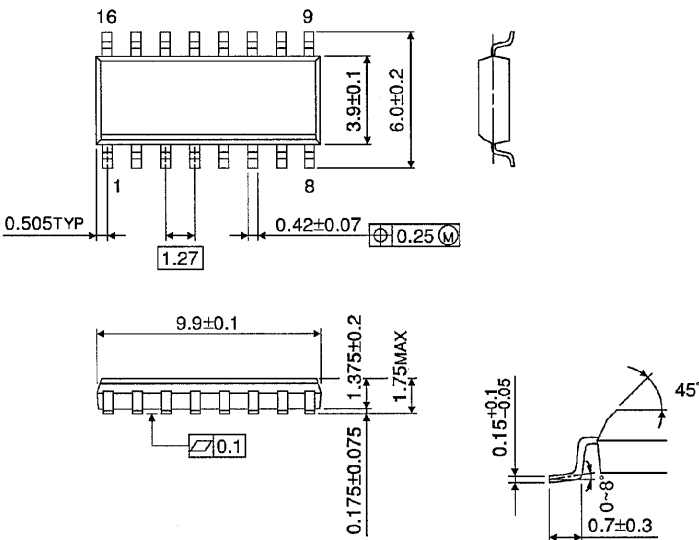


Weight : 0.18g (Typ.)

SOP 16PIN (150mil BODY) PACKAGE DIMENSIONS (SOL16-P-150 -1.27)

Unit in mm

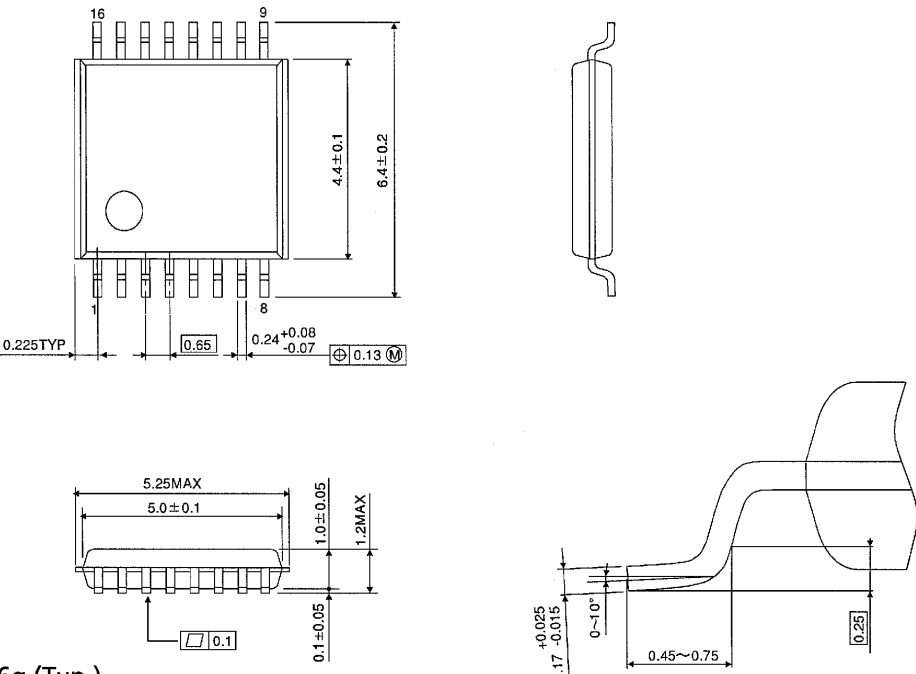
(Note) This package is not available in Japan.



Weight : 0.13g (Typ.)

TSSOP 16PIN PACKAGE DIMENSIONS (TSSOP16-P-0044-0.65)

Unit in mm



Weight : 0.06g (Typ.)

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