8-INPUT PECL DIFFERENTIAL MUX WITH TTL SELECTS

SY100S863

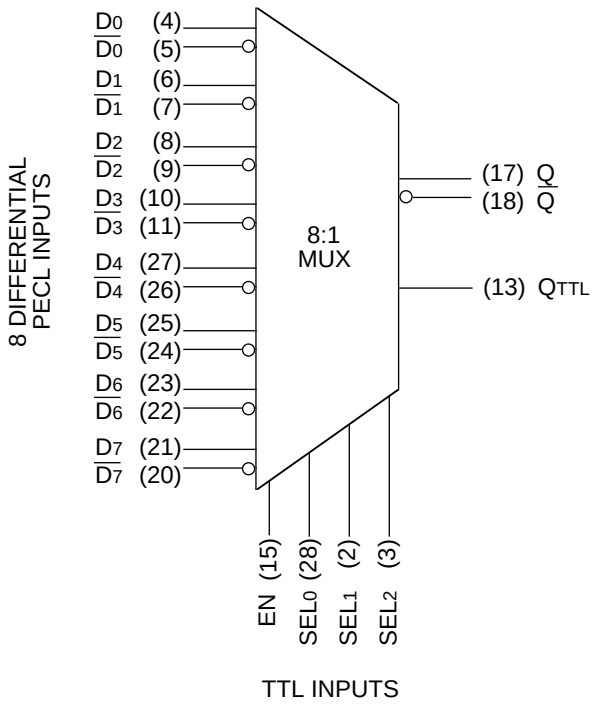
FEATURES

- **Low skew**
- **Differential PECL inputs**
- **Differential cut-off PECL outputs capable of driving 25Ω load for driving data bus**
- **Tri-state TTL output**
- **TTL select and enable input**
- **Internal 75KΩ PECL input pull-down resistors**
- **PECL I/O fully compatible with industry standard**
- **Available in 28-pin PLCC package**

DESCRIPTION

The SY100S863 is a PECL 8:1 multiplexer designed for use in new, high-performance PECL systems. It has differential PECL outputs and a standard TTL output. The TTL select inputs (SEL_0, SEL_1, SEL_2) determine which one of the eight differential PECL data inputs (D_0–D_7) is propagated to the outputs. The enable pin, EN, is provided for expansion. When EN is at a TTL logic one level, both PECL and TTL outputs are enabled. When the enable pin is set to TTL logic zero level, both PECL outputs of the differential pair are in cut-off and the TTL output is in a three-state condition.

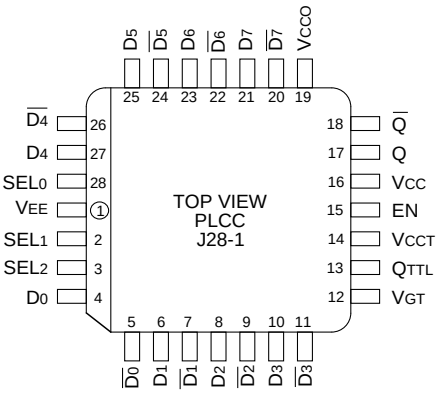
BLOCK DIAGRAM



PIN NAMES

Pin	Function
D_0, /D_0 – D_7, /D_7	Differential PECL Input Pairs
Q, /Q	Differential PECL Outputs
Q_{TTL}	TTL Output
EN	Enable Input
$SEL_{0,1,2}$	Select Inputs

PACKAGE/ORDERING INFORMATION



28-Pin PLCC (J28-1)

Ordering Information

Part Number	Package Type	Operating Range	Package Marking	Lead Finish
SY100S863JC	J28-1	Commercial	SY100S863JC	Sn-Pb
SY100S863JCTR[1]	J28-1	Commercial	SY100S863JC	Sn-Pb
SY100S863JZ[2]	J28-1	Commercial	SY100S863JZ with Pb-Free bar-line indicator	Matte-Sn
SY100S863JZTR[1, 2]	J28-1	Commercial	SY100S863JZ with Pb-Free bar-line indicator	Matte-Sn

Notes:

1. Tape and Reel.
2. Pb-Free package is recommended for new designs.

TRUTH TABLE

EN	SEL_2	SEL_1	SEL_0	Q	Q_{TTL}
H	L	L	L	D_0	D_0
H	L	L	H	D_1	D_1
H	L	H	L	D_2	D_2
H	L	H	H	D_3	D_3
H	H	L	L	D_4	D_4
H	H	L	H	D_5	D_5
H	H	H	L	D_6	D_6
H	H	H	H	D_7	D_7
L	X	X	X	Z	Z

PECL DC ELECTRICAL CHARACTERISTICS

$V_{CC} = V_{CCO} = V_{CCT} = 5.0V \pm 5\%$; $V_{EE} = V_{GT}$ = GND

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
V_{OH}	Output HIGH Voltage[1]	3.975	4.045	4.13	V	Loading with 25Ω to 3V (V_{CC}-2V)
V_{OL}	Output LOW Voltage[1]	3.17	3.295	3.38	V	Loading with 25Ω to 3V (V_{CC}-2V)
V_{OZ}	Cutoff Voltage[1]	—	3	3.10	V	Loading with 25Ω to 3V (V_{CC}-2V)
V_{IH}	Input HIGH Voltage	3.835	—	4.13	V	
V_{IL}	Input LOW Voltage	3.17	—	3.525	V	
I_{IH}	Input HIGH Current	—	—	350	µA	$V_{IN} = V_{IH}$ (Max.)
I_{IL}	Input LOW Current	0.50	—	—	µA	$V_{IN} = V_{IL}$ (Min.)
I_{CC}	V_{CC} Supply Current	—	73	88	mA	

Note:

1. Levels shown are for V_{CCO} = 5.0V and will vary 1:1 with powers.

TTL DC ELECTRICAL CHARACTERISTICS

$V_{CC} = V_{CCO} = V_{CCT} = 5.0V \pm 5\%$; $V_{EE} = V_{GT}$ = GND

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
V_{OH}	Output HIGH Voltage	2.4	2.9	—	V	I_{OH} = –3mA
V_{OL}	Output LOW Voltage	—	0.3	0.5	V	I_{OL} = 24mA
V_{IH}	Input HIGH Voltage	2.0	—	V_{CC}	V	
V_{IL}	Input LOW Voltage	0	—	0.8	V	
I_{IH}	Input HIGH Current	—	—	1.0	mA	V_{IN} = 2.7V
I_{IL}	Input LOW Current	–0.7	—	—	mA	V_{IN} = 0.5V
V_{IK}	Input Clamp Voltage	–1.2	—	—	V	I_{IN} = –18mA
I_{OS}	Output Short Circuit Current	–200	—	–60	mA	V_{OUT} = 0V, V_{CCT} = 5.5V
I_{OZHT}	Tri-state Current Output HIGH	—	—	70	µA	V_{OUT} = 2.7V
I_{OZLT}	Tri-state Current Output LOW	–700	—	—	µA	V_{OUT} = 0.5V

PECL AC ELECTRICAL CHARACTERISTICS

$V_{CC} = V_{CCO} = +5.0V \pm 5\%$; $V_{EE} = V_{GT} = GND$

Symbol	Parameter	$T_A = 0°C$			$T_A = +25°C$			$T_A = +85°C$			Unit	Condition
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.		
t_{PLH}	Propagation Delay[1],[2]										ps	
t_{PHL}	D to Q	500	—	900	500	—	900	500	—	900		
	SEL_0 to Q	300	—	2000	300	—	2000	300	—	2000		
	SEL_1 to Q	300	—	1750	300	—	1750	300	—	1750		
	SEL_2 to Q	300	—	1500	300	—	1500	300	—	1500		
t_{PZH}	EN to Q[3] (Cutoff to HIGH)	300	—	1750	300	—	1750	300	—	1750	ps	
t_{PHZ}	EN to Q[3]300 (HIGH to Cutoff)	—	1300	300	—	1300	300	—	1300			
t_r	Output Rise/Fall Times[2]	300	400	600	300	400	600	300	400	600	ps	
t_f	20% to 80%											

Notes:

1. Part-to-part skew is defined as Max. – Min. value at the given temperature.
2. $R_L = 50\Omega$
3. Figures 1 and 2

TTL AC ELECTRICAL CHARACTERISTICS

$V_{CC} = V_{CCO} = 5V \pm 5\%$; $V_{EE} = V_{GT} = GND$

Symbol	Parameter	$T_A = 0°C$			$T_A = +25°C$			$T_A = +85°C$			Unit	Condition
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.		
t_{PLH}	Propagation Delay[1][2]										ns	
t_{PHL}	D to Q_{TTL}	2.5	—	5.0	2.5	—	5.0	2.5	—	5.0		
	SEL_0 to Q_{TTL}	2.5	—	5.0	2.5	—	5.0	2.5	—	5.0		
	SEL_1 to Q_{TTL}	2.5	—	5.0	2.5	—	5.0	2.5	—	5.0		
	SEL_2 to Q_{TTL}	2.5	—	5.0	2.5	—	5.0	2.5	—	5.0		
t_{PZH}	EN to TTL Output[2]	2.5	—	5.0	2.5	—	5.0	2.5	—	5.0	ns	
t_{PZL}	(Enable Time)	2.5	—	5.0	2.5	—	5.0	2.5	—	5.0		
t_{PHZ}	EN to TTL Output[2]	2.5	—	5.0	2.5	—	5.0	2.5	—	5.0	ns	
t_{PLZ}	(Disable Time)	2.5	—	5.0	2.5	—	5.0	2.5	—	5.0		
t_r	Output Rise/Fall Time[3]										ns	
t_f	0.8V to 2.4V	0.3	—	1.6	0.3	—	1.6	0.3	—	1.6		
	0.8Vto 2.0V											

Notes:

1. Part-to-part skew is defined as Max. – Min. value at the given temperature.
2. Figures 3 and 4
3. $C_L = 25pF$

PECL-TO-PECL TEST CIRCUITRY

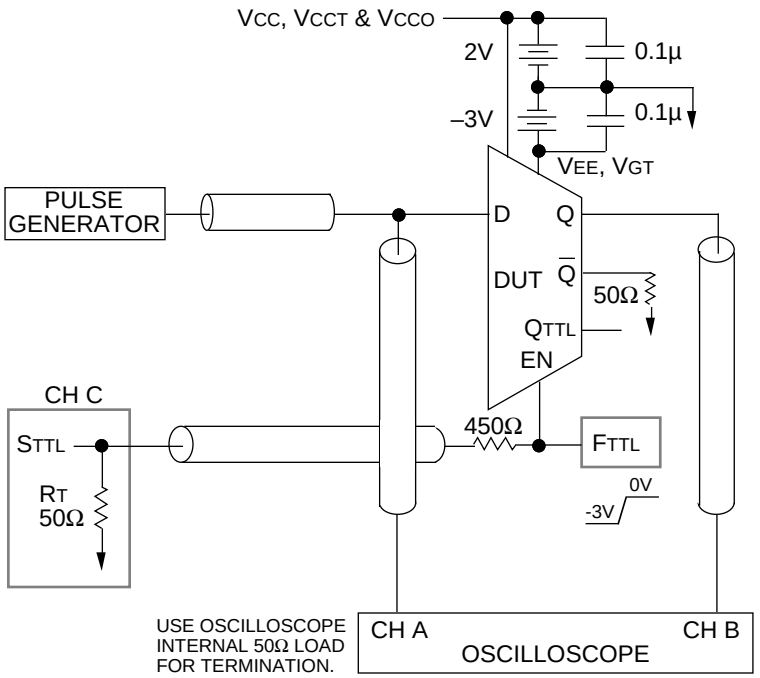


Figure 1. PECL-to-PECL AC Test Circuit

PECL-TO-PECL SWITCHING WAVEFORMS

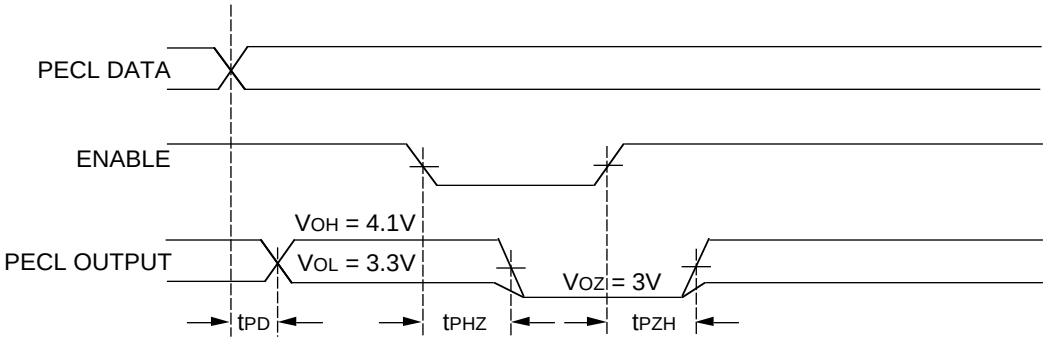


Figure 2. PECL-to-PECL Transition — Propagation Delay and Transition Times

PECL-TO-TTL TEST CIRCUITRY

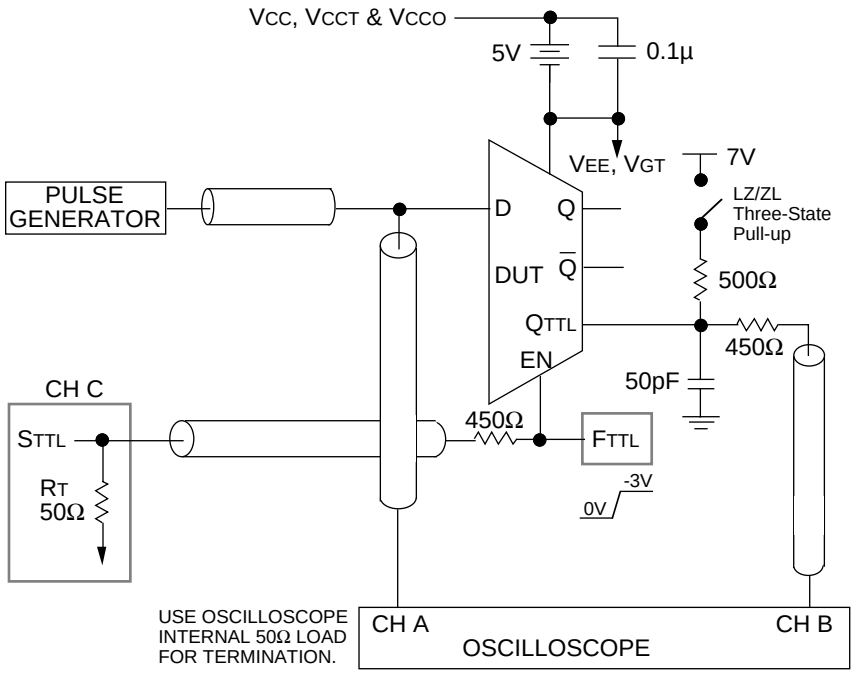


Figure 3. PECL-to-TTL AC Test Circuit

PECL-TO-TTL SWITCHING WAVEFORMS

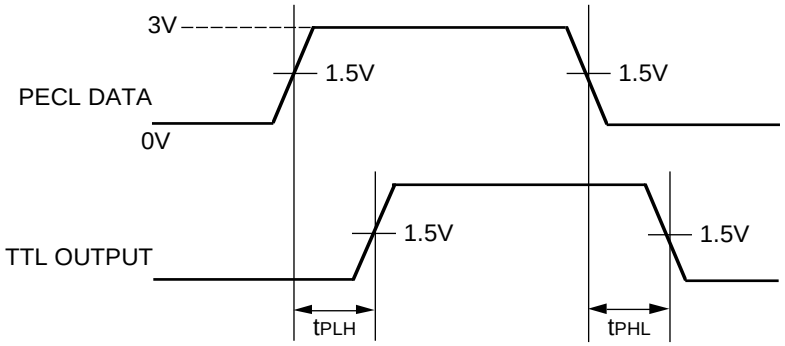


Figure 4a. PECL-to-TTL Transition, Data to TTL Output Delay

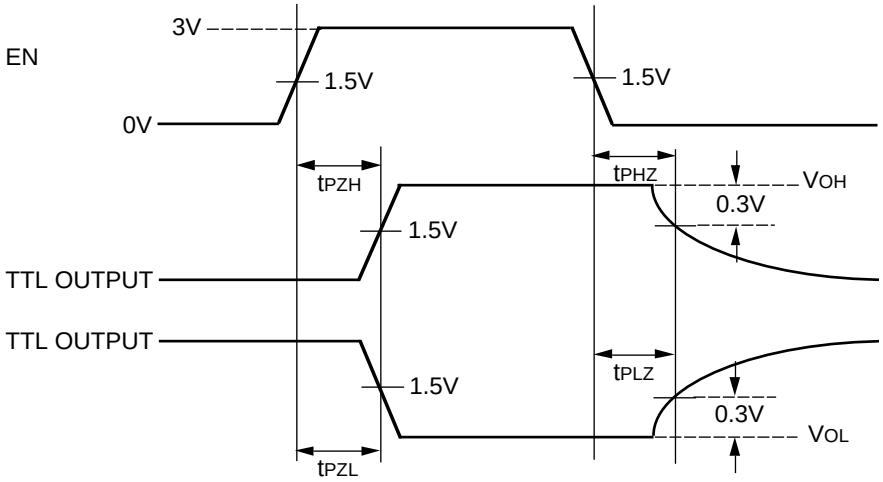
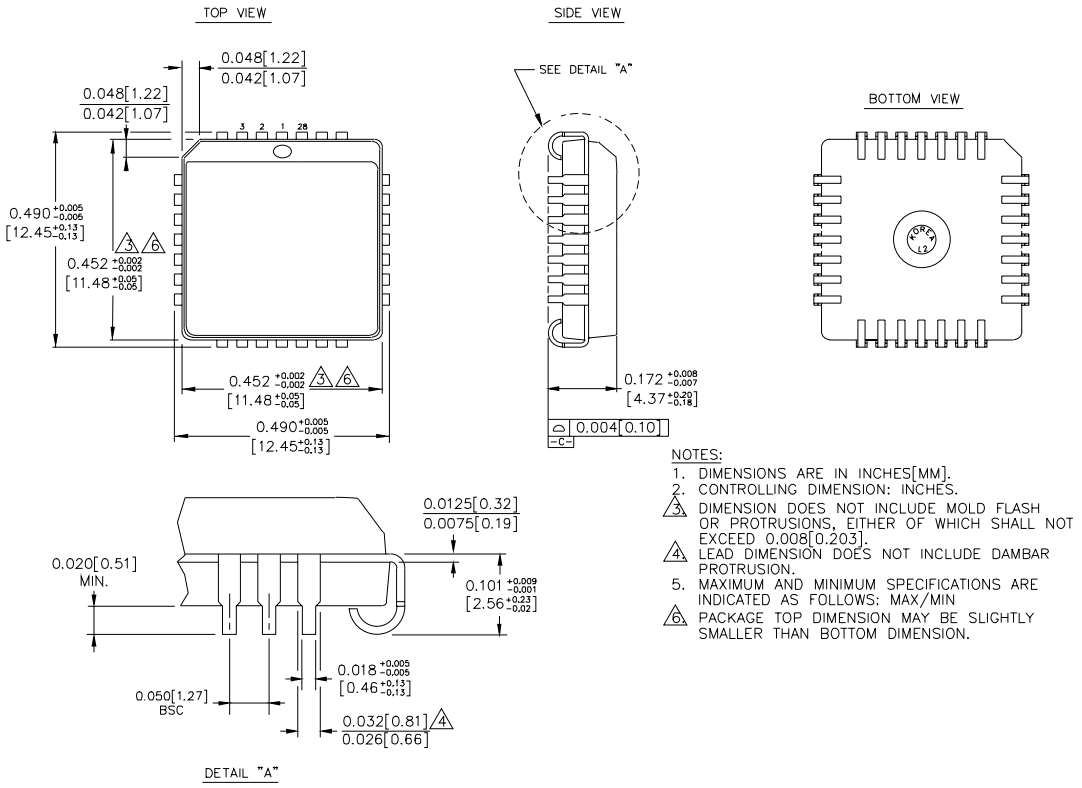


Figure 4b. EN to TTL Output Enable and Disable Times

28-PIN PLCC (J28-1)



NOTES:
1. DIMENSIONS ARE IN INCHES[MM].
2. CONTROLLING DIMENSION: INCHES.
3. DIMENSION DOES NOT INCLUDE MOLD FLASH OR PROTRUSIONS, EITHER OF WHICH SHALL NOT EXCEED 0.008[0.203].
4. LEAD DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION.
5. MAXIMUM AND MINIMUM SPECIFICATIONS ARE INDICATED AS FOLLOWS: MAX/MIN
6. PACKAGE TOP DIMENSION MAY BE SLIGHTLY SMALLER THAN BOTTOM DIMENSION.

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