

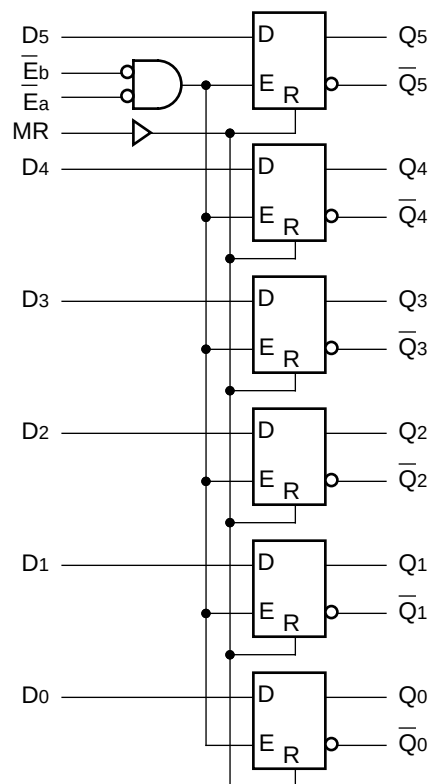
FEATURES

- Max. transparent propagation delay of 900ps
- Min. Master Reset and Enable pulse widths of 100ps
- IEE min. of -98mA
- Industry standard 100K ECL levels
- Extended supply voltage option:
VEE = -4.2V to -5.5V
- Voltage and temperature compensation for improved noise immunity
- Internal 75KΩ input pull-down resistors
- More than 40% faster than Fairchild
- Approximately 30% lower power than Fairchild
- Function and pinout compatible with Fairchild F100K
- Available in 24-pin CERPACK and 28-pin PLCC packages

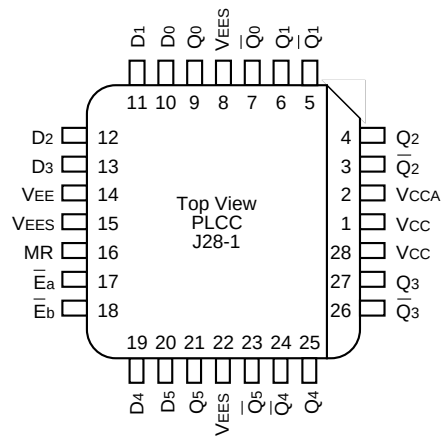
DESCRIPTION

The SY100S350 offers six high-speed D-Latches with both true and complement outputs, and is performance compatible for use with high-performance ECL systems. When both enable signals ($\bar{E}_a$ and $\bar{E}_b$) are at a logic LOW, the latches are transparent and the input signals (D_0 – D_5) appear at the outputs (Q_0 – Q_5) after a propagation delay. If either or both of the enable signals are at a logic HIGH, then the latches store the last valid data present on its inputs before $\bar{E}_a$ or $\bar{E}_b$ went to a logic HIGH. The Master Reset ($\overline{MR}$) overrides all other input signals and takes the outputs to a logic LOW state. All inputs have 75KΩ pull-down resistors.

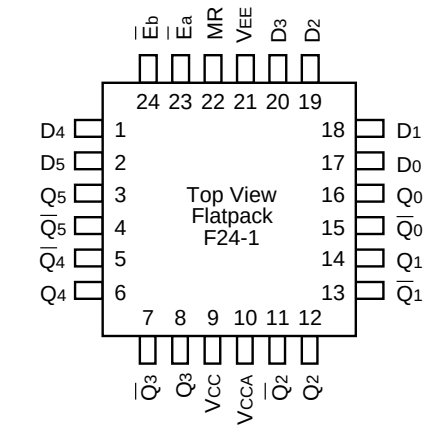
BLOCK DIAGRAM



PACKAGE/ORDERING INFORMATION



28-Pin PLCC (J28-1)



24-Pin Cerpack (F24-1)

Ordering Information

Part Number	Package Type	Operating Range	Package Marking	Lead Finish
SY100S350FC	F24-1	Commercial	SY100S350FC	Sn-Pb
SY100S350FCTR ⁽¹⁾	F24-1	Commercial	SY100S350FC	Sn-Pb
SY100S350JC	J28-1	Commercial	SY100S350JC	Sn-Pb
SY100S350JCTR ⁽¹⁾	J28-1	Commercial	SY100S350JC	Sn-Pb
SY100S350JZ ⁽²⁾	J28-1	Commercial	SY100S350JZ with Pb-Free bar-line indicator	Matte-Sn
SY100S350JZTR ^(1, 2)	J28-1	Commercial	SY100S350JZ with Pb-Free bar-line indicator	Matte-Sn

- Notes:
- 1. Tape and Reel.
 - 2. Pb-Free package is recommended for new designs.

PIN NAMES

Pin	Function
D ₀ — D ₅	Data Inputs
$\bar{E}_a$, $\bar{E}_b$	Common Enable Inputs (Active LOW)
MR	Asynchronous Master Reset Input
Q ₀ — Q ₅	Data Outputs
$\bar{Q}_0$ — $\bar{Q}_5$	Complementary Data Outputs
VEES	VEE Substrate
VCCA	Vcco for ECL Outputs

TRUTH TABLE⁽¹⁾

Each Latch

Inputs				Outputs		Operating Mode
D _n	$\bar{E}_a$	$\bar{E}_b$	MR	Q _n	$\bar{Q}_n$	
H	L	L	L	H	L	Latch
L	L	L	L	L	H	
X	X	H	L	Latched ⁽²⁾	Latched ⁽²⁾	
X	H	X	L	Latched ⁽²⁾	Latched ⁽²⁾	
X	X	X	H	L	H	Asynchronous

NOTES:

1. H = HIGH State
L = LOW State
X = Don't Care

2. Retains data that is present before $\bar{E}$ positive transition.

DC ELECTRICAL CHARACTERISTICS

VEE = -4.2V to -5.5V unless otherwise specified; VCC = VCCA = GND

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
I _{IH}	Input HIGH Current	—	—	250	μA	V _{IN} = V _{IH} (Max.)
	MR	—	—	250		
	D _n	—	—	250		
	$\bar{E}_a$, $\bar{E}_b$	—	—	250		
I _{EE}	Power Supply Current	-98	-78	-49	mA	Inputs Open

AC ELECTRICAL CHARACTERISTICS

CERPACK

$V_{EE} = -4.2V$ to $-5.5V$ unless otherwise specified; $V_{CC} = V_{CCA} = GND$

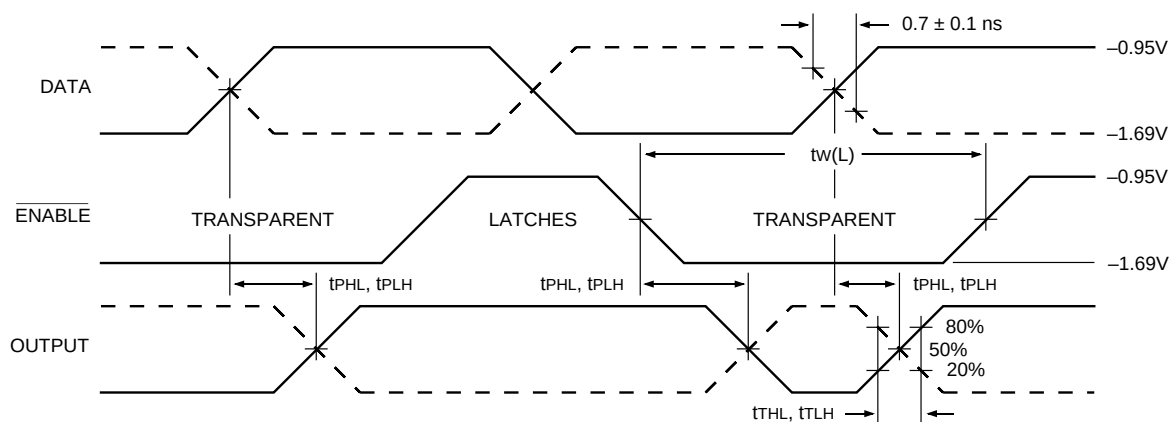
Symbol	Parameter	$T_A = 0^{\circ}C$		$T_A = +25^{\circ}C$		$T_A = +85^{\circ}C$		Unit	Condition
		Min.	Max.	Min.	Max.	Min.	Max.		
t _{PLH} t _{PHL}	Propagation Delay D _n to Output	300	1000	300	1000	300	1000	ps	
t _{PLH} t _{PHL}	Propagation Delay $\bar{E}_a$, $\bar{E}_b$ to Output	300	1100	300	1100	300	1100	ps	
t _{PLH} t _{PHL}	Propagation Delay MR to Output	300	1250	300	1250	300	1250	ps	
t _{TLH} t _{THL}	Transition Time 20% to 80%, 80% to 20%	300	900	300	900	300	900	ps	
t _s	Set-up Time, D _n to $\bar{E}_n$	500	—	500	—	500	—	ps	
t _H	Hold Time, D _n to $\bar{E}_n$	500	—	500	—	500	—	ps	
t _r	Release Time, MR to $\bar{E}_n$	1000	—	1000	—	1000	—	ps	
t _{PW} (L)	Pulse Width, $\bar{E}_a$, $\bar{E}_b$	1000	—	1000	—	1000	—	ps	
t _{PW} (H)	Pulse Width, MR	1000	—	1000	—	1000	—	ps	

PLCC

$V_{EE} = -4.2V$ to $-5.5V$ unless otherwise specified; $V_{CC} = V_{CCA} = GND$

Symbol	Parameter	$T_A = 0^{\circ}C$		$T_A = +25^{\circ}C$		$T_A = +85^{\circ}C$		Unit	Condition
		Min.	Max.	Min.	Max.	Min.	Max.		
t _{PLH} t _{PHL}	Propagation Delay D _n to Output	300	900	300	900	300	900	ps	
t _{PLH} t _{PHL}	Propagation Delay E _a , E _b to Output	300	1000	300	1000	300	1000	ps	
t _{PLH} t _{PHL}	Propagation Delay MR to Output	300	1200	300	1200	300	1200	ps	
t _{TLH} t _{THL}	Transition Time 20% to 80%, 80% to 20%	300	900	300	900	300	900	ps	
t _s	Set-up Time, D _n to E _n	500	—	500	—	500	—	ps	
t _H	Hold Time, D _n to E _n	500	—	500	—	500	—	ps	
t _r	Release Time, MR to E _n	1000	—	1000	—	1000	—	ps	
t _{PW} (L)	Pulse Width, E _a , E _b	1000	—	1000	—	1000	—	ps	
t _{PW} (H)	Pulse Width, MR	1000	—	1000	—	1000	—	ps	

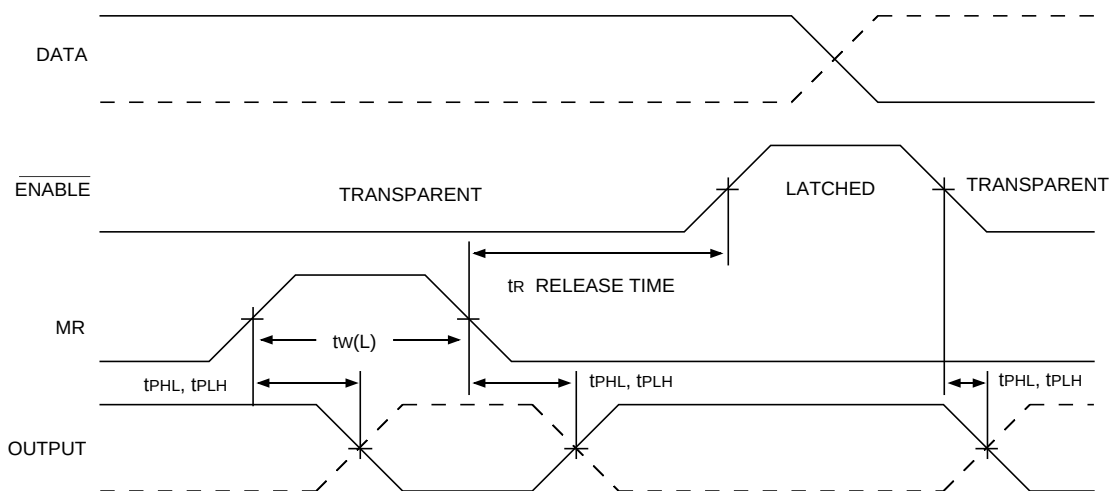
TIMING DIAGRAMS



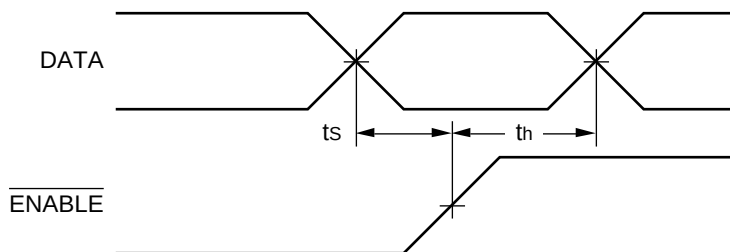
Enable Timing

Note:

$V_{EE} = -4.2V$ to $-5.5V$ unless otherwise specified; $V_{CC} = V_{CCA} = GND$



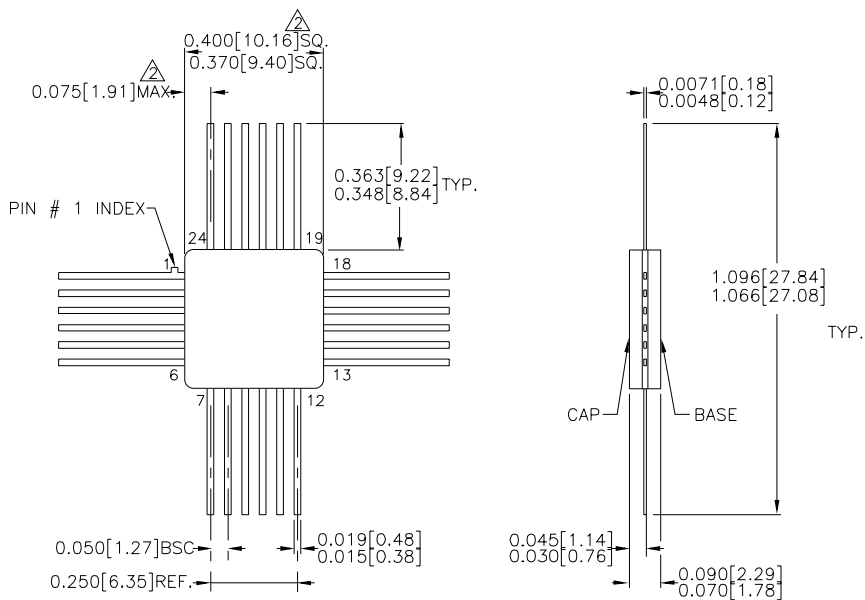
Reset Timing

TIMING DIAGRAMS**Data Set-up and Hold Times****Notes:**

t_s is the minimum time before the transition of the clock that information must be present at the data input.

t_h is the minimum time after the transition of the clock that information must remain unchanged at the data input.

24-PIN CERPACK (F24-1)

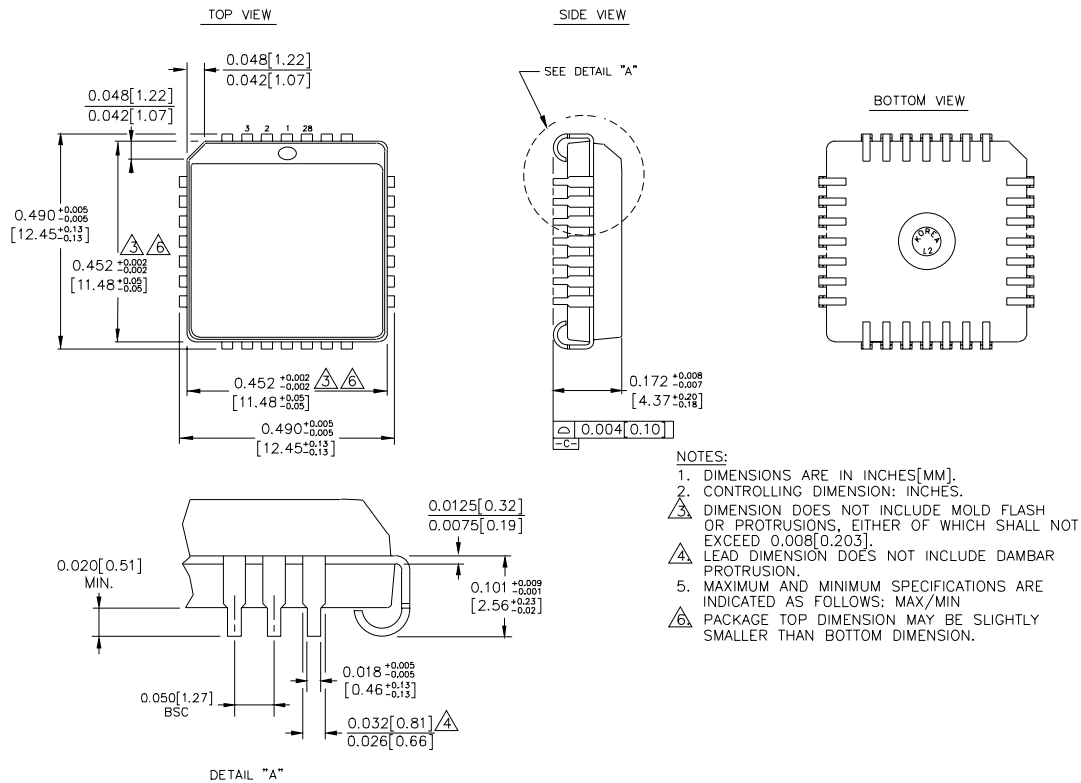


NOTES:

1. DIMENSIONS ARE IN INCHES[MM].
2. THIS DIMENSION INCLUDES GLASS PROTRUSION AND CAP TO BASE ALIGNMENT TOLERANCES.
3. DIMENSIONS SHOWN ARE MAX/MIN, WHERE NOTED.

Rev. 03

28-PIN PLCC (J28-1)



Rev. 03

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