SDLS182 - DECEMBER 1983 - REVISED MARCH 1988

5 CLKA

- 'LS56 Performs 50 to 1 Frequency Division (5 to 1, 5 to 1, and 10 to 1)
- 'LS57 Performs 60 to 1 Frequency Division (6 to 1, 5 to 1, and 10 to 1)
- Available in P or JG package (two P or JG Packages Fit in a Single 16-pin Socket)
- Maximum Clock Frequency 25 MHz Typical

SN54LS56, SN54LS57 . . . JG PACKAGE SN74LS56, SN74LS57 . . . JG OR P PACKAGE

(TOP VIEW) CLKB 1 8 QC VCC 2 7 QB QA 3 6 CLR

FOR CHIP CARRIER INFORMATION, CONTACT THE FACTORY

GND 4

description

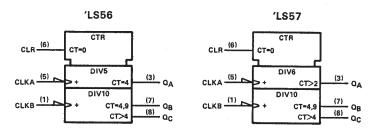
These frequency dividers are particularly useful in generating one second or one hour timing pulses from 50 Hz (European standard frequency) or 60 Hz (United States standard frequency). 50 to 1 frequency division is accomplished in the 'LS56 by connecting output Q_A to input CLKB. 60 to 1 frequency division in the 'LS57 is accomplished in the same way. More universal capabilities are evidenced by the 25 MHz typical fmax and the almost limitless frequency division possibilities when used in cascade. Two 'LS56 packages may be interconnected to give frequency division of 2500 to 1,625 to 1,100 to 1, etc. Two 'LS57 packages can be connected to generate frequency divisions of 3600 to 1, 1800 to 1, 900 to 1 etc.

The 'LS56 and 'LS57 frequency dividers consist of three separate counters, A, B, and C on a single monolithic substrate. The A counter divides by 5 to 1 in the 'LS56 and by 6 to 1 in the 'LS57. The B counter divides by 5 to 1 in both devices and is internally tied to the C counter which divides by 2 to 1. The resulting C counter output is 10 to 1. Both the 'LS56 and 'LS57 feature a clear pin which is common to all three counters, A, B, and C. When the clear pin is low, the counters are enabled. When the clear is high, the counters are disabled and their outputs are set to a low-level.

All three counters, A, B, and C trigger on the high-to-low transition of the clock input. All output waveforms are symmetrical except for the 5 to 1 outputs (A and B of the 'LS56 and B of the 'LS57). See the output waveform drawings below.

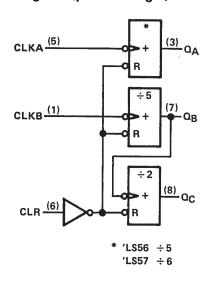
input and output waveforms

logic symbols†

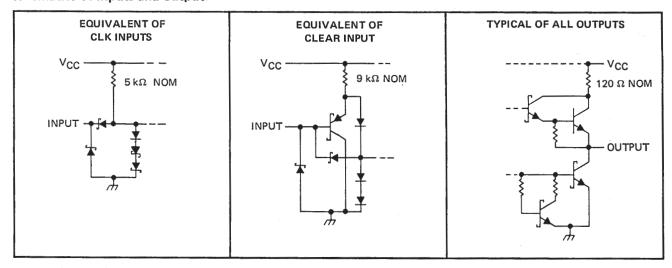


[†]These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



schematics of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, VCC (see Note 1)		7 V
Input voltage: CLR	***************************************	7 V
CLKA, CLKB	***************************************	5.5 V
Operating free-air temperature range:	SN54LS'	55°C to 125°C
	SN74LS'	0°C to 70°C
Storage temperature range	***************************************	65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

		SN54LS'			SN74LS'			
		MIN	NOM	MAX	MIN	МОИ	MAX	UNIT
Vcc	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
VIH	High-level input voltage	2			2			V
VIL	Low-level input voltage			0.7			0.8	V
ЮН	High-level output current			-1			-1	mA
IOL	Low-level output current			8			16	mA
fclock	Clock frequency	0		15	0		15	MHz
t _r , t _f	Rise and fall time of clock			50			50	ns
t _W	Pulse width of clock or clear	30			30			ns
t _{su}	Clear inactive state set-up time	25			25			ns
TA	Operating free-air temperature	-55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		SN54LS'			SN74LS'				
						TYP‡	MAX	MIN	TYP‡	MAX	UNIT
VIK		V _{CC} = MIN,	I _I = 18 mA				– 1.5			– 1.5	V
V _{OH}		V _{CC} = MIN, V _{IL} = MAX	V _{IH} = 2 V,	I _{OH} = -1 mA	2,5	3.4		2.7	3,4		٧
VOL		V _{CC} = MIN,	V _{IH} = 2 V,	I _{OL} = 8 mA		0.25	0.4		0,25	0.4	
-01		VIL = MAX		I _{OL} = 16 mA					0.35	0.5	V .
Ц	CLKA, CLKB	Vcc = MAX		V ₁ = 5.5 V			0,2			0,2	
٠١	CLR	ACC - MAY		V ₁ = 7 V			0.1			0.1	mA
Lea	CLKA, CLKB	\/ _ NAA\/			-		80			80	-
ΙΗ	CLR	V _{CC} = MAX,	V ₁ = 2.7 V				20			20	μΑ
1	CLKA, CLKB	.,					- 3,2			- 3,2	
!IL	CLR	V _{CC} = MAX,	$CLR = 0 V, \qquad V_{\parallel} = 0.4$	$V_1 = 0.4 V$			- 0.2			- 0.2	mA
los§		V _{CC} = MAX,	CLR = 0 V,	V _O = 0 V	- 20		- 100	- 20		- 100	mA
Icc		V _{CC} = MAX,	See Note 2	<u> </u>		17	30		• 17	30	mA

[†] For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

switching characteristics, VCC = 5 V, TA = 25°C (see note 3)

PARAMETER	FROM	то	TEST CONDITIONS -			'LS56			'LS57			
	(INPUT)	(OUTPUT)			MIN	TYP	MAX	MIN	TYP	MAX	UNIT	
f _{max}	CLKA	QA			15	25		15	25		MHz	
f _{max}	CLKB	α _B , α _C	Ī		15	25		15	25		MHz	
^t PLH	CLKB	0-				8	15		8	15	ns	
^t PHL	CLNB	σB				14	- 25		14	25	ns	
t _{PLH} ¶	CLKB	0				18	30		18	30	ns	
t _{PHL} ¶	CLKb	σ_{C}	чС	R _L = 1 kΩ,	$C_L = 30 pF$		24	35		24	35	ns
t _{PLH}	CLKA					12	20		14	25	ns	
^t PHL	CLKA	QA				14	25		18	30	ns	
tPHL -	CLR	QA				17	30		17	30	ns	
^t PHL	CLR	α_{B}				17	30		17	30	ns	
^t PHL	CLR	QC				17	30		17	30	ns	

 \P Times measured from CLKB to output Q_C are taken with output Q_B unloaded. NOTE 3: Load circuits and voltage waveforms are shown in Section 1.



[‡] All typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25 ^{\circ} \text{C}$.

[§] Not more than one output should be shorted at a time and the duration of the short-circuit should not exceed one second.

NOTE 2: I_{CC} is measured by applying 4.5 V to the CLR pin with all other inputs grounded and the outputs open.

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Following are URLs where you can obtain information on other Texas Instruments products and application solutions:

Products		Applications	
Amplifiers	amplifier.ti.com	Audio	www.ti.com/audio
Data Converters	dataconverter.ti.com	Automotive	www.ti.com/automotive
DSP	dsp.ti.com	Broadband	www.ti.com/broadband
Interface	interface.ti.com	Digital Control	www.ti.com/digitalcontrol
Logic	logic.ti.com	Military	www.ti.com/military
Power Mgmt	power.ti.com	Optical Networking	www.ti.com/opticalnetwork
Microcontrollers	microcontroller.ti.com	Security	www.ti.com/security
Low Power Wireless	www.ti.com/lpw	Telephony	www.ti.com/telephony
		Video & Imaging	www.ti.com/video
		Wireless	www.ti.com/wireless





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PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
SN74LS56P	OBSOLETE	PDIP	Р	8	TBD	Call TI	Call TI
SN74LS57P	OBSOLETE	PDIP	Р	8	TBD	Call TI	Call TI
SN74LS57P	OBSOLETE	PDIP	Р	8	TBD	Call TI	Call TI

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS) or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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