



DESCRIPTION

PT6909 is a fixed frequency PWM controller IC designed to control high brightness LED driver using a single-stage PFC boost-buck topology. It can achieve a well power factor and a higher dc-bus voltage. This topology allows reducing the filter capacitors and using non-electrolytic capacitors to improve reliability. The PT6909 uses open-loop peak current control technique eliminates a need for loop compensation, limits the input inrush current, and is inherently protected from input under-voltage condition.

PT6909 provides a low frequency PWM dimming input that can accept an external control signal with a duty cycle of 0-100% and a frequency of between 100Hz and a few KHz. The PWM dimming capability enables PT6909 phase control solutions that can work with standard TRIAC.

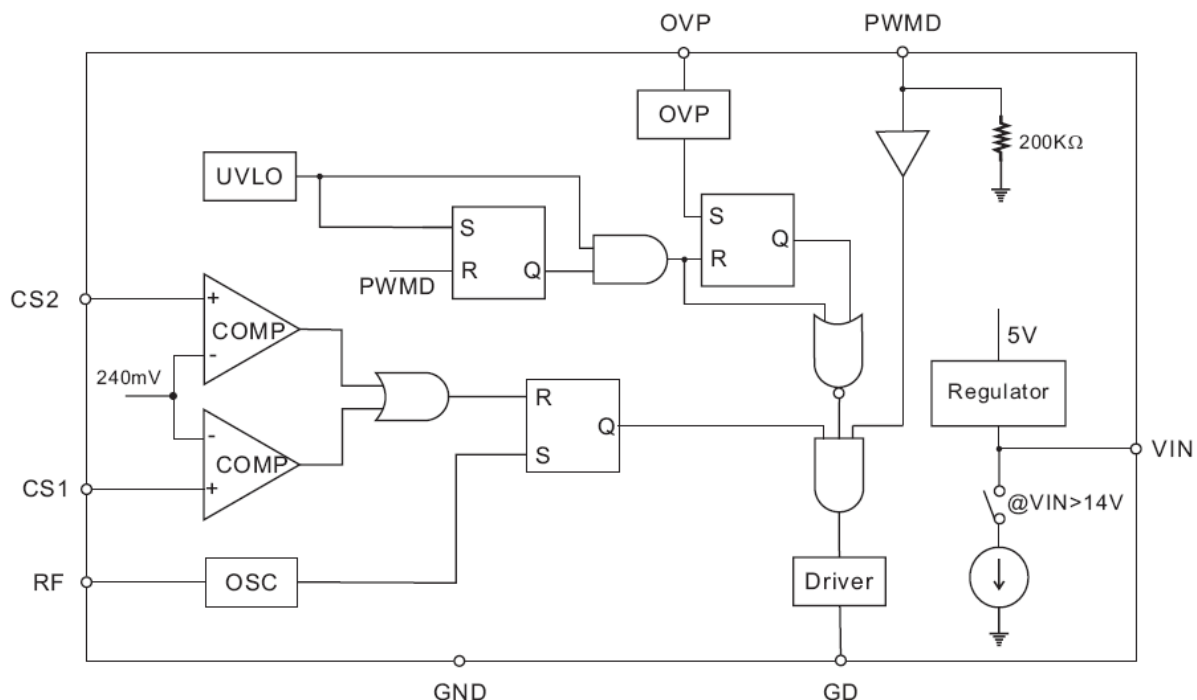
FEATURES

- Simple power factor correction Integrated
- Low start-up current
- 8V to 12V input range
- Constant-current driver
- Programmable fixed frequency operation
- Input and output current sensing
- Input current limit
- Boost circuit over-voltage protection(LED open protection)
- Input voltage limitation
- Low Input current harmonic distortion
- PWM Low-frequency dimming and phase Dimming compatible

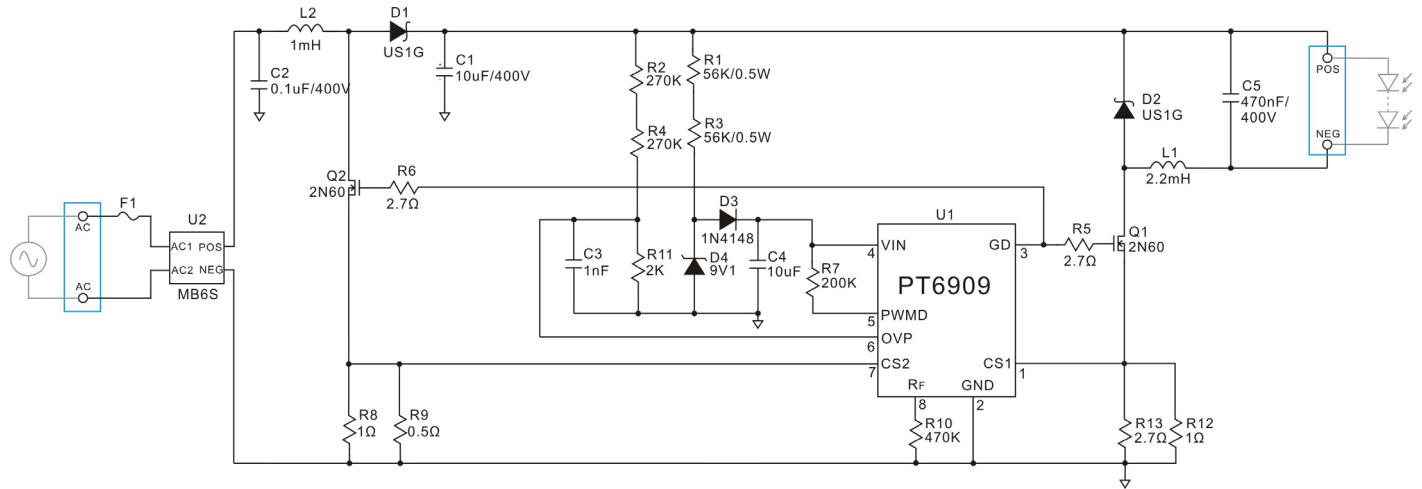
APPLICATIONS

- LED replacement tube
- AC/DC LED driver
- LED Lamp with phase dimmable
- Street lamps
- Traffic signals

BLOCK DIAGRAM



TYPICAL APPLICATION



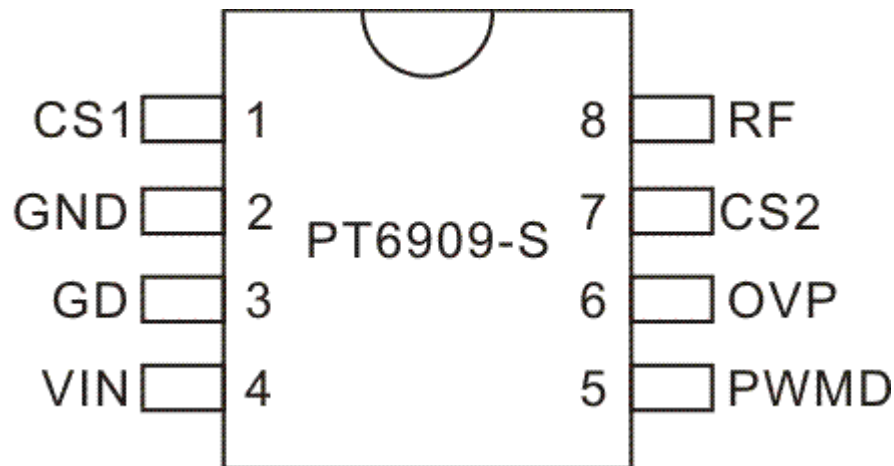
Typical 110V/AC 8W LED Tube With PFC Application



ORDER INFORMATION

Valid Part Number	Package Type	Top Code
PT6909-S	8 Pins, SOP, 150MIL	PT6909-S

PIN CONFIGURATION



PIN DESCRIPTION

Pin Name	Description	Pin No.
CS1	Input or Output Current Sense	1
GND	Ground	2
GD	Drives the Gate of External MOSFET	3
VIN	Input Voltage 8V-12V DC	4
PWMD	Low Frequency PWM Dimming pin, also Enable pin	5
OVP	Over Voltage Detection	6
CS2	Input or Output Current Sense	7
RF	Oscillator Frequency Setting	8

FUNCTION DESCRIPTION

POWER TOPOLOGY

PT6909 is optimized to drive non-isolated topology, cascading an input PFC boost stage and an output buck converter power stage. This power converter topology offers numerous advantages useful for driving high-brightness LED. These advantages include power factor correction, low harmonic distortion of the input AC line current. The power converter topology also permits reducing the size of a filter capacitor needed, enabling use of non-electrolytic capacitors. The latter advantage greatly improves reliability of the overall solution.

PT6909 is a peak current-mode controller that is specifically designed to drive a constant current buck power converter. PT6909 controls two identical current sense comparators for detecting input and output current. One of the comparators regulates the output LED current, while the other is used for sensing the input inductor current. The comparator sensing the input inductor current is mainly responsible for the converter start-up. The control scheme can achieve a low inrush current, also avoid a high input current while the AC input is under-voltage.

OVER VOLTAGE DETECTION

PT6909 includes output over voltage detection function. The OVP pin is used for sensing the output voltage of boost stage. The PT6909 will latch the GD output at shutdown state when the output voltage reaches OVP threshold voltage. In the typical application circuit, the system will go into hiccup mode if the LED load is open. When the LED load is disconnected, the output voltage rises as the output capacitor C1 starts charging. When the PT6909 detects an over voltage condition and turns off the converter. The PT6909's power supply VIN drops under UVLO threshold voltage and goes into low current start-up status. The PT6909 restarts and turns on the converter. The system starts another cycle until the LED load is re-connected.

INPUT VOLTAGE LIMITATION

PT6909 built-in power-supply clamped circuit. In the typical application circuit, when the VIN voltage rises higher than 14V typically, it will be clamped at this level with internal 5mA current sink capability.

SETTING INPUT AND OUTPUT CURRENT

Two current sense comparators are included in the PT6909. Both comparators have their inverting inputs internally connected to 240mV. The CS1 and CS2 inputs are non-inverting inputs of the comparators. When either the CS1 or CS2 pin voltage rises up 240mV, the GD pulse is terminated. A leading edge blanking delay of 300ns(typ) is added. The GD voltage becomes high again upon receiving the next clock pulse of the oscillator circuit.

Referring to the Typical Application Diagram, the CS1 comparator is responsible for regulating output current. The output LED current can be programmed using the following equation:

$$I_{LED} = \frac{0.24}{R_{CS1}} - \frac{1}{2} \Delta I_{L1}$$

Where ΔI_{L1} is the peak-to-peak current ripple in L1. The CS2 comparator limits the current in the input inductor L2. Therefore, the PT6909 starts-up in the input current limiting mode. The CS2 voltage sensing must be programmed such that no input current limiting occurs in normal steady-state operation. The L2 current sensing resistor R_{CS2} can be programmed using the following equation:

$$R_{CS2} < \frac{0.24}{I_{L2P}}$$

Where, I_{L2P} is the maximum peak current in L2.



PWM DIMMING AND TRAIC DIMMING

PWM dimming scheme can be implemented by external low frequency PWM signal to the PWMD pin. When the PWMD pin is pulled high, the gate driver is enabled and the circuit operates normally. When the PWMD pin is left open or connected to GND, the gate driver is disabled and the external MOSFET turns off. By using the duty cycle of the PWM control method that can change the working and the closing time, and the light output can be adjusted between zero and the internal set. In addition, the PWM dimming method is limited because the output current cannot be exceeded the internal set.

The power topology does not require filter capacitance at the output side of rectifier bridge. Therefore, sampling the phase-controlled voltage waveform of TRAIC connects PT6909's PWMD pin can realize TRAIC dimming.

OSCILLATOR

Connecting an external resistor from RF pin to GND programs switching frequency:

$$F_{osc} = \frac{2.6 \times 10^{10}}{R_{RF}}$$



ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating	Unit
VIN to GND		-0.3 ~ +16	V
CS1,CS2 to GND		-0.3 ~ +6	V
GD to GND		-0.3 ~ +16	V
PWMD to GND		-0.3 ~ +16	V
OVP to GND		-0.3 ~ +6	V
RF to GND		-0.3 ~ +6	V
Operating temperature	Topr	-40 ~ +85	°C
Storage temperature	Tstg	-65 ~ +150	°C

ELECTRICAL CHARACTERISTICS

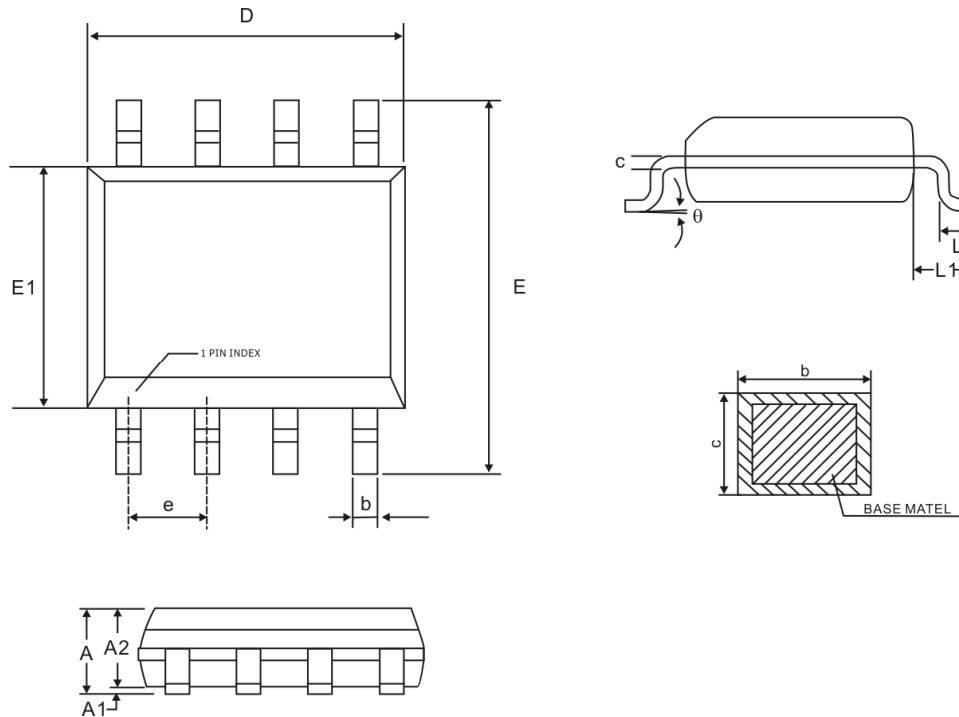
(Unless otherwise specified, Ta=25°C)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Input DC supply voltage	VIN	DC input voltage	8	9	12	V
VIN clamped voltage	VCLP	PWMD=VIN		14		V
Current sink capability at VIN	ICLP	PWMD=VIN			5	mA
Start-up current	I _{START}	PWMD=GND, VIN rising			30	uA
Active supply current	I _{INAC}	VIN=12V, PWMD=VIN, VCS1=VCS2=0.5V		0.56	0.7	mA
Stand-by supply current	I _{INST}	VIN=12V, PWMD=VIN, VCS1=VCS2=GND		0.46	0.6	mA
VIN start voltage	VST	VIN rising	6.5	7.0	7.5	V
VIN under voltage lockout hysteresis	VHYS	VIN falling	0.6	0.9	1.2	V
Pin PWMD input low voltage	V _{ENL}	VIN=8~12V			1.2	V
Pin PWMD input high voltage	V _{ENH}	VIN=8~12V	2.5			V
Pin PWMD pull-down resistance	R _{EN}	VPWMD=5V	170	200	230	KΩ
Current sense threshold voltage	V _{CS}	VIN=8~12V	220	240	260	mV
Over voltage protection threshold voltage	VOVP	VIN=8~12V		1.21		V
RF voltage	VRF	VIN=8~12V, R _{RF} =270KΩ	1.18	1.21	1.24	V
Oscillator frequency	FOSC	R _{RF} =270KΩ	75	95	115	KHz
Maximum oscillator PWM duty cycle	D _{MAX}	R _{RF} =270KΩ, CS1= CS2=GND			100	%
Current sense blanking internal	T _{BLANK}	VCS1=VCS2=0.5V	200	300	400	ns
GD high output voltage	V _{GDH}	ISource=10mA	VIN-0.3			V
GD low output voltage	V _{GDL}	ISink=10mA			0.2	V
GD output rise time	T _{RISE}	CGD=560pF		30	50	ns
GD output fall time	T _{FALL}	CGD=560pF		30	50	ns



PACKAGE INFORMATION

8 PINS, SOP, 150MIL



Symbol	Millimeter		
	Min.	Nom.	Max.
A	1.35	1.60	1.77
A1	0.08	0.15	0.28
A2	1.20	1.40	1.65
b	0.33	-	0.51
c	0.17	-	0.26
D	4.70	4.90	5.10
E	5.80	6.00	6.20
E1	3.70	3.90	4.10
e	1.27BSC		
L	0.38	0.60	1.27
θ	0°	-	8°

Notes:

1. All dimensions are in millimeter
2. Refer to JEDEC MS-012 AA



IMPORTANT NOTICE

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