PRELIMINARY

RoboClock®
CY7B9945V

High Speed Multi-phase PLL Clock Buffer

Features

- 500 ps max Total Timing Budget™ (TTB™) window
- 24–200 MHz input and output operation
- Low output-output skew < 200 ps
- 10 + 1 LVTTL outputs driving 50W terminated lines
- Dedicated feedback output
- Phase adjustments in 625/1300 ps steps up to +10.4 ns
- 3.3V LVTTL/LVPECL, fault tolerant, and hot insertable reference inputs
- Multiply or divide ratios of 1–6, 8, 10, and 12
- Individual output bank disable
- Output high impedance option for testing purposes
- Integrated phase locked loop (PLL) with lock indicator
- Low cycle-cycle jitter (<100 ps peak-peak)
- 3.3V operation
- Industrial temperature range: –40°C to +85°C
- 52-pin 1.4 mm TQFP package

Functional Description

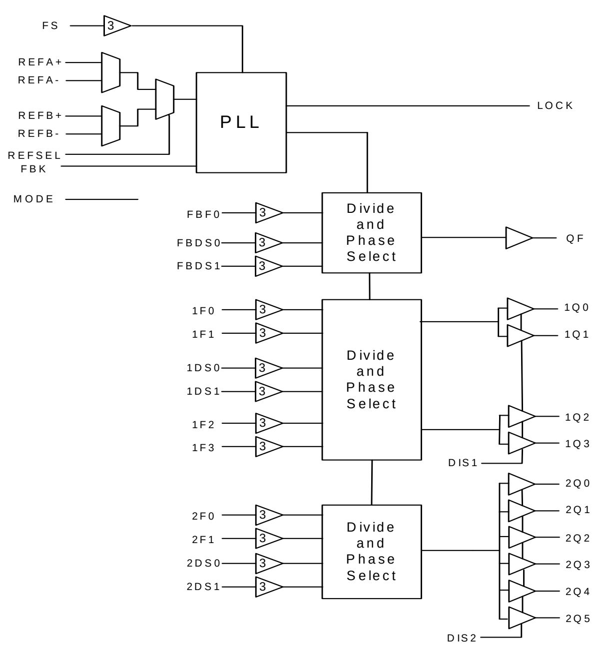
The CY7B9945V high speed multi-phase PLL clock buffer offers user selectable control over system clock functions. This multiple output clock driver provides the system integrator with functions necessary to optimize the timing of high performance computer and communication systems.

The device features a guaranteed maximum TTB window specifying all occurrences of output clocks. This includes the input reference clock across variations in output frequency, supply voltage, operating temperature, input edge rate, and process.

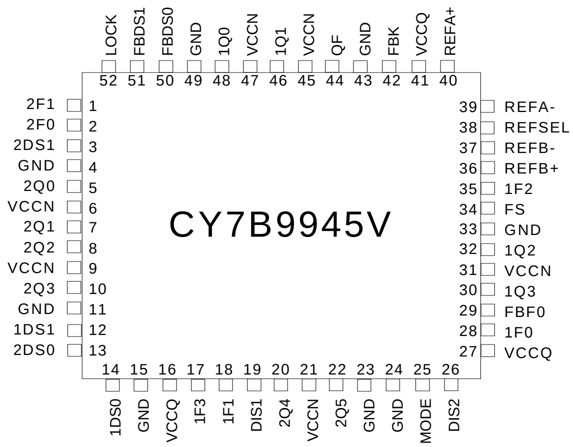
Ten configurable outputs each drive terminated transmission lines with impedances as low as 50W while delivering minimal and specified output skews at LVTTL levels. The outputs are arranged in two banks of four and six outputs. These banks enable a divide function of 1 to 12, with phase adjustments in 625 ps–1300 ps increments up to ±10.4 ns. The dedicated feedback output enables divide-by functionality from 1 to 12 and limited phase adjustments. However, if needed, any one of the ten outputs can be connected to the feedback input as well as driving other inputs.

Selectable reference input is a fault tolerant feature that enables smooth change over to a secondary clock source when the primary clock source is not in operation. The reference inputs and feedback inputs are configurable to accommodate both LVTTL or Differential (LVPECL) inputs. The completely integrated PLL reduces jitter and simplifies board layout.

Logic Block Diagram



Pin Configuration



Pin Definitions

Pin	Name	IO	Type	Description
34	FS	Input	Three level Input	**Frequency Select**. This input must be set according to the nominal frequency (f_{NOM}). See *Table 1*.
40,39, 36,37	REFA+, REFA- REFB+, REFB-	Input	LVTTL/ LVDIFF	**Reference Inputs**. These inputs can operate as differential PECL or single-ended TTL reference inputs to the PLL. When operating as a single-ended LVTTL input, the complementary input is left open.
38	REFSEL	Input	LVTTL	**Reference Select Input**. The REFSEL input controls the configuration of reference input When LOW, it uses the REFA pair as the reference input. When HIGH, it uses the REFB pair as the reference input. This input has an internal pull down.
42	FBK	Input	LVTTL	**Feedback Input Clock**. The PLL operates such that the rising edges of the reference and feedback signals are aligned in phase and frequency. This pin provides the clock output QF feedback to the phase detector.
28,18, 35,17,2, 1	1F[0:3], 2F[0:1]	Input	Three level Input	**Output Phase Function Select**. Each pair determines the phase of the respective bank of outputs. See *Table 3*.
19,26	DIS[1:2]	Input	LVTTL	**Output Disable**. Each input controls the state of the respective output bank. When HIGH, the output bank is disabled to HOLD-OFF or High-Z state; the disable state is determined by MODE. When LOW, outputs 1Q[0:3] and 2Q[0:5] are enabled. See *Table 5*.
14,12, 13,3	[1:2]DS[0:1]	Input	Three level Input	**Output Divider Function Select**. Each pair determines the divider ratio of the respective bank of outputs. See *Table 4*.
29	FBF0	Input	Three level Input	**Feedback Output Phase Function Select**. This input determines the phase of the QF output. See *Table 3*.
50,51	FBDS[0:1]	Input	Three level Input	**Feedback Output Divider Function Select**. This input determines the divider ratio of the QF output. See *Table 4*.
48,46, 32,30, 5,7,8,10, 20,22	1Q[0:3], 2Q[0:5]	Output	LVTTL	**Clock Outputs with Adjustable Phases and f_{NOM} Divide Ratios**. The output frequencies and phases are determined by [1:2]DS[0:1], and 1F[0:3] and 2F[0:1], respectively. See *Table 3* and *Table 4*.
44	QF	Output	LVTTL	**Feedback Clock Output**. This output is connected to the FBK input. The output frequency and phase are determined by FBDS[0:1] and FBF0, respectively. *See Table 3 and Table 4.*
52	LOCK	Output	LVTTL	**PLL Lock Indicator**. When HIGH, this output indicates that the internal PLL is locked to the reference signal. When LOW, it indicates that the PLL is attempting to acquire lock
25	MODE	Input	Three level Input	**This pin determines the clock outputs' disable state**. When this input is HIGH, the clock outputs disables to high impedance state (High-Z). When this input is LOW, the clock outputs disables to HOLD-OFF mode. When in MID, the device enters factory test mode.
6,9,21, 31, 45, 47	VCCN		PWR	**Power Supply for the Output Buffers**
16,27, 41	VCCQ		PWR	**Power Supply for the Internal Circuitry**
4,11,15, 23,24, 33,43,49	GND		PWR	**Device Ground**

Block Diagram Description

The PLL adjusts the phase and the frequency of its output signal to minimize the delay between the reference (REFA/B+, REFA/B-) and the feedback (FB) input signals.

The CY7B9945V has a flexible REF input scheme. These inputs enable the use of either differential LVPECL or single ended LVTTL inputs. To configure as single ended LVTTL inputs, leave the complementary pin open (internally pulled to 1.5V), then the other input pin is used as a LVTTL input. The REF inputs are also tolerant to hot insertion.

The REF inputs are changed dynamically. When changing from one reference input to the other reference input of the same frequency, the PLL is optimized to ensure that the clock outputs period is not less than the calculated system budget (tMIN = tREF (nominal reference period) – tCCJ (cycle-cycle jitter) – tPDEV (max. period deviation)) while reacquiring lock.

The FS control pin setting determines the nominal operational frequency range of the divide by one output (fNOM) of the device. fNOM is directly related to the VCO frequency. The FS setting for the device is shown in *Table 1*. For CY7B9945V, the upper fNOM range extends from 96 MHz to 200 MHz.

Table 1. Frequency Range Select

FS[1]	f_{NOM} (MHz)	
	Min	**Max**
LOW	24	52
MID	48	100
HIGH	96	200

Time Unit Definition

Selectable skew is in discrete increments of time unit (t_U). The value of a t_U is determined by the FS setting and the maximum nominal output frequency. The equation determines the t_U value as follows:

$t_U = 1/(f_{NOM}*N)$.

N is a multiplication factor that is determined by the FS setting. f_{NOM} is nominal frequency of the device. N is defined in *Table 2*.

Table 2. N Factor Determination

FS	CY7B9945V	
	N	**f_{NOM} (MHz) at which t_U = 1.0 ns**
LOW	32	31.25
MID	16	62.5
HIGH	8	125

Divide and Phase Select Matrix

The Divide Select Matrix is comprised of three independent banks: two of clock outputs and one for feedback. The Phase Select Matrix, enables independent phase adjustments on 1Q[0:1], 1Q[2:3] and 2Q[0:5]. The frequency of 1Q[0:3] is controlled by 1DS[0:1] while the frequency of 2Q[0:5] is controlled by 2DS[0:1]. The phase of 1Q[0:1] is controlled by 1F[0:1], that of 1Q[2:3] is controlled by 1F[2:3] and that of 2Q[0:5] is controlled by 2F[0:1].

The high fanout feedback output buffer (QF) connects to the feedback input (FBK).This feedback output has one phase function select input (FBF0) and two divider function selects FBDS[0:1].

The phase capabilities that are chosen by the phase function select pins are shown in *Table 3*. The divide capabilities for each bank are shown in *Table 4*.

Table 3. Output Phase Select

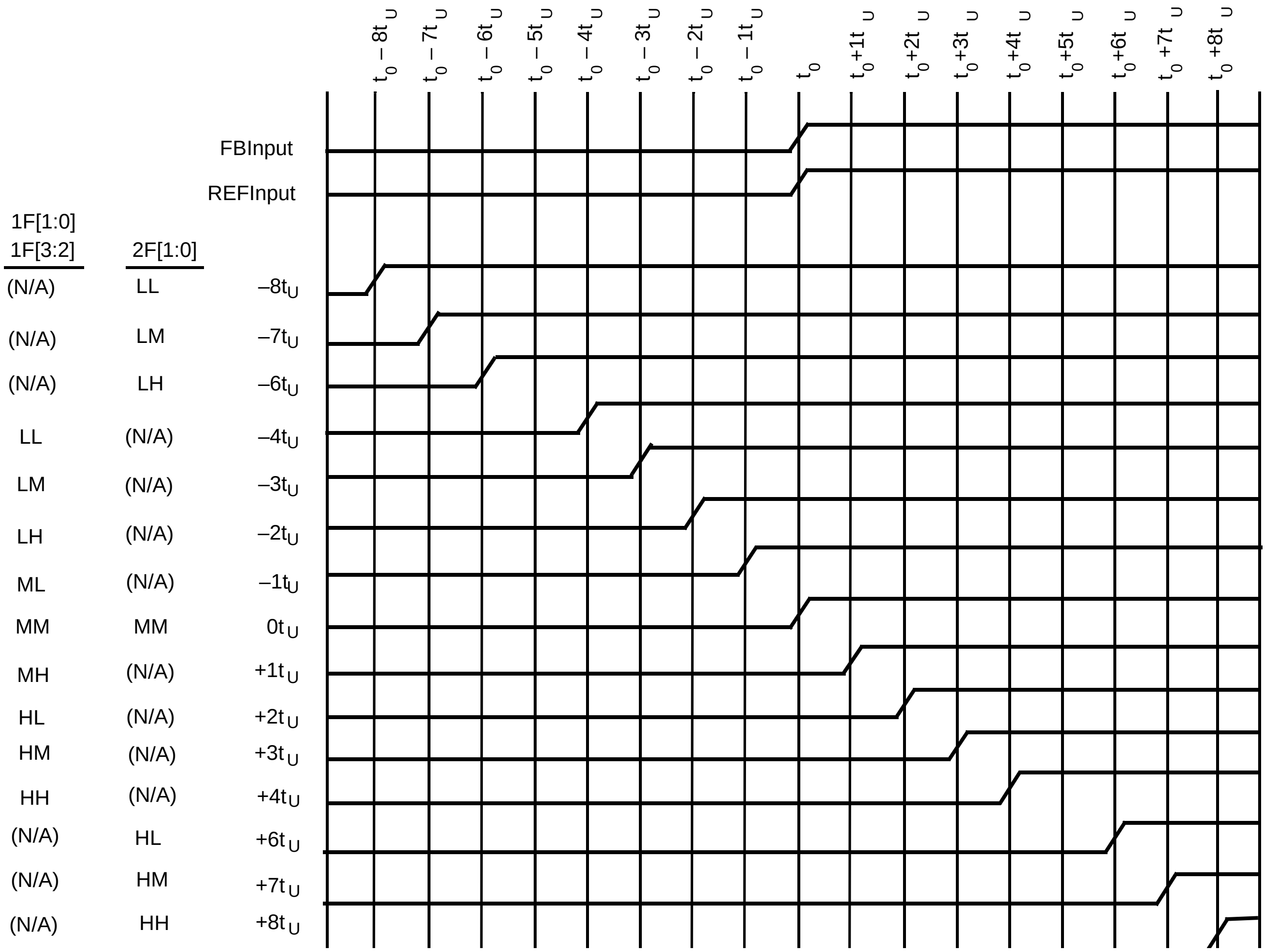
Control Signal		Output Phase Function			
1F1	**1F0**	**1Q[0:1]**			
1F3	**1F2**		**1Q[2:3]**		
2F1	**2F0**			**2Q[0:5]**	
	FBF0				**QF**
LOW	LOW	$-4t_U$	$-4t_U$	$-8t_U$	$-4t_U$
LOW	MID	$-3t_U$	$-3t_U$	$-7t_U$	N/A
LOW	HIGH	$-2t_U$	$-2t_U$	$-6t_U$	N/A
MID	LOW	$-1t_U$	$-1t_U$	BK1Q[0:1][2]	N/A
MID	MID	$0t_U$	$0t_U$	$0t_U$	$0t_U$
MID	HIGH	$+1t_U$	$+1t_U$	BK1Q[2:3][2]	N/A
HIGH	LOW	$+2t_U$	$+2t_U$	$+6t_U$	N/A
HIGH	MID	$+3t_U$	$+3t_U$	$+7t_U$	N/A
HIGH	HIGH	$+4t_U$	$+4t_U$	$+8t_U$	$+4t_U$

Table 4. Output Divider Select

Control Signal		Output Divider Function		
[1:2]DS1 and FBDS1	[1:2]DS0 and FBDS0	Bank1	Bank2	Feedback
LOW	LOW	/ 1	/ 1	/ 1
LOW	MID	/ 2	/ 2	/ 2
LOW	HIGH	/ 3	/ 3	/ 3
MID	LOW	/ 4	/ 4	/ 4
MID	MID	/ 5	/ 5	/ 5
MID	HIGH	/ 6	/ 6	/ 6
HIGH	LOW	/ 8	/ 8	/ 8
HIGH	MID	/ 10	/ 10	/ 10
HIGH	HIGH	/ 12	/ 12	/ 12

Figure 1 shows the timing relationship of programmable skew outputs. All times are measured with respect to REF with the output used for feedback programmed with $0t_U$ skew. The PLL naturally aligns the rising edge of the FB input and REF input. If the output used for feedback is programmed to another skew position, then the whole t_U matrix shifts with respect to REF. For example, if the output used for feedback is programmed to shift –4tU, then the whole matrix is shifted forward in time by 4tU. Thus an output programmed with 4tU of skew gets effectively be skewed $8t_U$ with respect to REF.

Figure 1. Typical Outputs with FB Connected to a Zero-Skew Output[3]



Output Disable Description

The output of each output bank can be independently put into a HOLD OFF or high impedance state. The combination of the MODE and DIS[1:2] inputs determines the clock outputs' state for each bank. When the DIS[1:2] is LOW, the outputs of the corresponding banks are enabled. When DIS[1:2] is HIGH, the outputs for that bank are disabled to a high impedance (HI-Z) or HOLD OFF state. *Table 5* defines the disabled outputs functions.

The HOLD OFF state is a power saving feature. An output bank is disabled to the HOLD OFF state in a maximum of six output clock cycles from the time the disable input is HIGH. When disabled to the HOLD OFF state, outputs are driven to a logic LOW state on their falling edges. This makes certain that the output clocks are stopped without a glitch. When a bank of outputs is disabled to HI-Z state, the respective bank of outputs go HI-Z immediately.

Table 5. DIS[1:2] Functionality

MODE	DIS[1:2]	1Q[0:3], 2Q[0:5]
HIGH/LOW	LOW	ENABLED
HIGH	HIGH	HI-Z
LOW	HIGH	HOLD-OFF
MID	X	FACTORY TEST

Notes
1. FB connected to an output selected for "Zero" skew (i.e., FBF0 = MID or XF[1:0] = MID).
2. The level set on FS is determined by the "nominal" operating frequency (f_{NOM}) of the V_{CO} and Phase Generator. f_{NOM} always appears on an output when the output is operating in the undivided mode. The REF and FB are at f_{NOM} when the output connected to FB is undivided.
3. BK1Q denotes following the skew setting of indicated Bank1 outputs.
4. These inputs are normally wired to V_{CC}, GND, or left unconnected (actual threshold voltages vary as a percentage of V_{CC}). Internal termination resistors hold the unconnected inputs at $V_{CC}/2$. If these inputs are switched, the function and timing of the outputs may glitch and the PLL may require an additional t_{LOCK} time before all data sheet limits are achieved.
5. This is for non-three level inputs.

Lock Detect Output Description

The LOCK detect output indicates the lock condition of the integrated PLL. Lock detection is accomplished by comparing the phase difference between the reference and feedback inputs. Phase error is declared when the phase difference between the two inputs is greater than the specified device propagation delay limit t_{PD}.

When in the locked state, after four or more consecutive feedback clock cycles with phase errors, the LOCK output is forced LOW to indicate out-of-lock state.

When in the out-of-lock state, 32 consecutive phase errorless feedback clock cycles are required to enable the LOCK output to indicate lock condition (LOCK = HIGH).

If the feedback clock is removed after LOCK has gone HIGH, a “Watchdog” circuit is implemented to indicate the out-of-lock condition after a time-out period by deasserting LOCK LOW. This time out period is based upon a divided down reference clock.

This assumes that there is activity on the selected REF input. If there is no activity on the selected REF input then the LOCK detect pin does not accurately reflect the state of the internal PLL.

Factory Test Mode Description

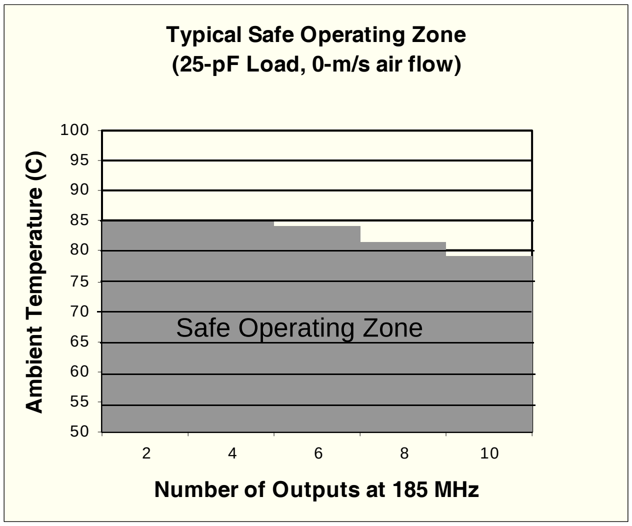
The device enters factory test mode when the MODE is driven to MID. In factory test mode, the device operates with its internal PLL disconnected; input level supplied to the reference input is used in place of the PLL output. In TEST mode the FB input is tied LOW. All functions of the device remain operational in factory test mode except the internal PLL and output bank disables. The MODE input is designed as a static input. Dynamically toggling this input from LOW to HIGH temporarily causes the device to go into factory test mode (when passing through the MID state).

When in the test mode, the device is reset to a deterministic state by driving the DIS2 input HIGH. Doing so disables all outputs and, after the selected reference clock pin has five positive transitions, all internal finite state machines (FSM) are set at a deterministic state. The states depend on the configurations of the divide, skew and frequency selection. All clock outputs stay in High-Z mode and all FSMs stay in the deterministic state until DIS2 is deasserted. This causes the device to reenter factory test mode.

Safe Operating Zone

Figure 2 shows the operating condition of the device not exceeding its allowable maximum junction temperature of 150°C. *Figure 2* shows the maximum number of outputs that can operate at 185 MHz (with 25 pF load and no air flow) or 200 MHz (with 10-pF load and no air flow) at various ambient temperatures. At the limit line, all other outputs are configured to divide-by-two (i.e., operating at 92.5 MHz) or lower frequencies. The device operates below maximum allowable junction temperature of 150°C when its configuration (with the specified constraints) falls within the shaded region (safe operating zone). *Figure 2* shows that at 85°C, the maximum number of outputs that can operate at 200 MHz is 6.

Figure 2. Typical Safe Operating Zone



Absolute Maximum Conditions

Operating outside these boundaries may affect the performance and life of the device. These user guidelines are not tested.

Storage Temperature .... –40°C to +125°C

Ambient Temperature with Power Applied.................................... –40°C to +125°C

Supply Voltage to Ground Potential................–0.5V to +4.6V

DC Input Voltage ....–0.3V to V_{CC}+0.5V

Output Current into Outputs (LOW)............................. 40 mA

Static Discharge Voltage.. > 1100V (MIL-STD-883, Method 3015)

Latch up Current..> ± 200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	3.3V ±10%
Industrial	–40°C to +85°C	3.3V ±10%

Electrical Characteristics Over the Operating Range

Description		Test Conditions	Min	Max	Unit
LVTTL HIGH Voltage	(QF, 1Q[0:3], 2Q[0:5])	V_{CC} = Min, I_{OH} = –30 mA	2.4	–	V
	LOCK	I_{OH} = –2 mA, V_{CC} = Min	2.4	–	V
LVTTL LOW Voltage	(QF, 1Q[0:3], 2Q[0:5])	V_{CC} = Min, I_{OL}= 30 mA	–	0.5	V
	LOCK	I_{OL}= 2 mA, V_{CC} = Min	–	0.5	V
High impedance State Leakage Current			–100	100	µA
LVTTL Input HIGH		Min ≤ V_{CC} ≤ Max	2.0	V_{CC} + 0.3	V
LVTTL Input LOW		Min. ≤ V_{CC} ≤ Max.	–0.3	0.8	V
LVTTL V_{IN} >V_{CC}		V_{CC} = GND, V_{IN} = 3.63V	–	100	µA
LVTTL Input HIGH Current		V_{CC} = Max, V_{IN} = V_{CC}	–	500	µA
LVTTL Input LOW Current		V_{CC} = Max, V_{IN} = GND	–500	–	µA
Three level Input HIGH[4]		Min ≤ V_{CC} ≤ Max	0.87 * V_{CC}	–	V
Three level Input MID[4]		Min ≤ V_{CC} ≤ Max	0.47 * V_{CC}	0.53 * V_{CC}	V
Three level Input LOW[4]		Min ≤ V_{CC} ≤ Max	–	0.13 * V_{CC}	V
Three level Input HIGH Current	FS[0:2],IF[0:3],FBDS[0:1]	V_{IN} = V_{CC}	–	200	µA
	2F[0:1],[1:2]DS[0:1],FBFO		–	400	µA
Three level Input MID Current	FS[0:2],IF[0:3],FBDS[0:1]	V_{IN} = V_{CC}/2	–50	50	µA
	2F[0:1],[1:2]DS[0:1],FBFO		–100	100	µA
Three level Input LOW Current	FS[0:2],IF[0:3],FBDS[0:1]	V_{IN} = GND	–200	–	µA
	2F[0:1],[1:2]DS[0:1],FBFO		–400	–	µA
Input Differential Voltage			400	V_{CC}	mV
Highest Input HIGH Voltage			1.0	V_{CC}	V
Lowest Input LOW Voltage			GND	V_{CC} – 0.4	V
Common Mode Range (Crossing Voltage)			0.8	V_{CC} – 0.2	V
Internal Operating Current	CY7B9945V	V_{CC} = Max, f_{MAX}[5]	–	250	mA
Output Current Dissipation/Pair[4]	CY7B9945V	V_{CC} = Max, C_{LOAD} = 25 pF, R_{LOAD} = 50Ω at V_{CC}/2, f_{MAX}	–	40	mA

Capacitance

Parameter	Description	Test Conditions	Min	Max	Unit
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 3.3V	–	5	pF

Switching Characteristics

Over the Operating Range [5, 7, 8, 9, 10]

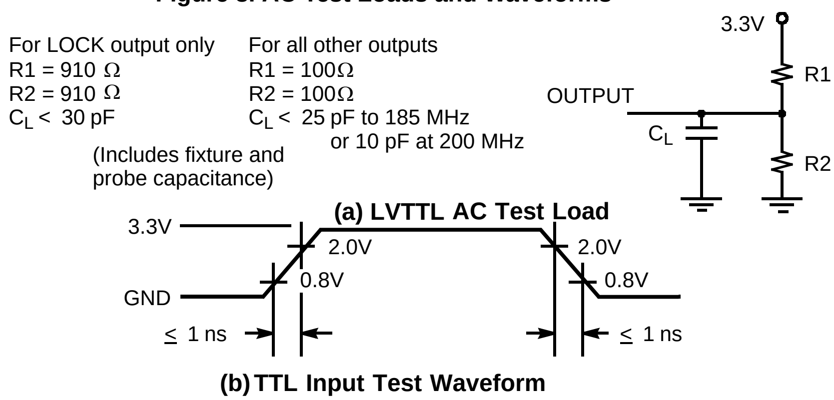
Parameter	Description	CY7B9945V-2		CY7B9945V-5		Unit
		Min	Max	Min	Max	
f_{in}	Clock Input Frequency	24	200	24	200	MHz
f_{out}	Clock Output Frequency	24	200	24	200	MHz
t_{SKEWPR}	Matched Pair Skew[12, 13],1Q[0:1],1Q[2:3],2Q[0:1],2Q[2:3],2Q[4:5]	–	200	–	200	ps
$t_{SKEWBNK}$	Intrabank Skew[12, 13]	–	250	–	250	ps
t_{SKEW0}	Output-Output Skew (same frequency and phase, rise to rise, fall to fall)[12, 13]	–	250	–	550	ps
t_{SKEW1}	Output-Output Skew (same frequency and phase, other banks at different frequency, rise to rise, fall to fall)[12, 13]	–	250	–	650	ps
t_{SKEW2}	Output-Output Skew (all output configurations outside of t_{SKEW0} and t_{SKEW1})[10, 11]	–	500	–	800	ps
t_{CCJ1-3}	Cycle-to-Cycle Jitter (divide by 1 output frequency, FB = divide by 1, 2, 3)	–	150	–	150	ps Peak-Peak
$t_{CCJ4-12}$	Cycle-to-Cycle Jitter (divide by 1 output frequency, FB = divide by 4, 5, 6, 8, 10, 12)	–	100	–	100	ps Peak-Peak
t_{PD}	Propagation Delay, REF to FB Rise	–250	250	–500	500	ps
TTB	Total Timing Budget window (same frequency and phase)[14, 15]	–	500	–	700	ps
$t_{PDDELTA}$	Propagation Delay difference between two devices[16]	–	200	–	200	ps
t_{REFpwh}	REF input (Pulse Width HIGH)[5]	2.0	–	2.0	–	ns
t_{REFpwl}	REF input (Pulse Width LOW)[5]	2.0	–	2.0	–	ns
t_r/t_f	Output Rise/Fall Time[17]	0.15	2.0	0.15	2.0	ns
t_{LOCK}	PLL Lock TIme From Power Up	–	10	–	10	ms
$t_{RELOCK1}$	PLL Relock Time (from same frequency, different phase) with Stable Power Supply	–	500	–	500	µs
$t_{RELOCK2}$	PLL Re-lock Time (from different frequency, different phase) with Stable Power Supply[16]	–	1000	–	1000	µs
t_{ODCV}	Output duty cycle deviation from 50%[11]	–1.0	1.0	–1.0	1.0	ns
t_{PWH}	Output HIGH time deviation from 50%[19]	–	1.5	–	1.5	ns
t_{PWL}	Output LOW time deviation from 50%[19]	–	2.0	–	2.0	ns
t_{PDEV}	Period deviation when changing from reference to reference[20]	–	0.025	–	0.025	UI
t_{OAZ}	DIS[1:2] HIGH to output high-impedance from ACTIVE[12, 21]	1.0	10	1.0	10	ns
t_{OZA}	DIS[1:2] LOW to output ACTIVE from output is high impedance[21, 22]	0.5	14	0.5	14	ns

Notes

6. Assumes 25 pF Maximum Load Capacitance up to 185 MHz. At 200 MHz the maximum load is 10 pF.
7. Both outputs of pair must be terminated, even if only one is being used.
8. Each package must be properly decoupled.
9. AC parameters are measured at 1.5V, unless otherwise indicated.
10. Test Load C_L= 25 pF, terminated to $V_{CC}/2$ with 50Ω up to185 MHz and 10 pF load to 200 MHz.
11. SKEW is defined as the time between the earliest and the latest output transition among all outputs for which the same phase dellay has been selected when all outputs are loaded with 25 pF and properly terminated up to 185 MHz. At 200 MHz the max load is 10 pF.
12. Tested initially and after any design or process changes that affect these parameters.
13. TTB is the window between the earliest and the latest output clocks with respect to the input reference clock across variations in output frequency, supply voltage, operating temperature, input clock edge rate, and process. The measurements are taken with the AC test load specified and include output-output skew, cycle-cycle jitter, and dynamic phase error. TTB is equal to or smaller than the maximum specified value at a given output frequency.

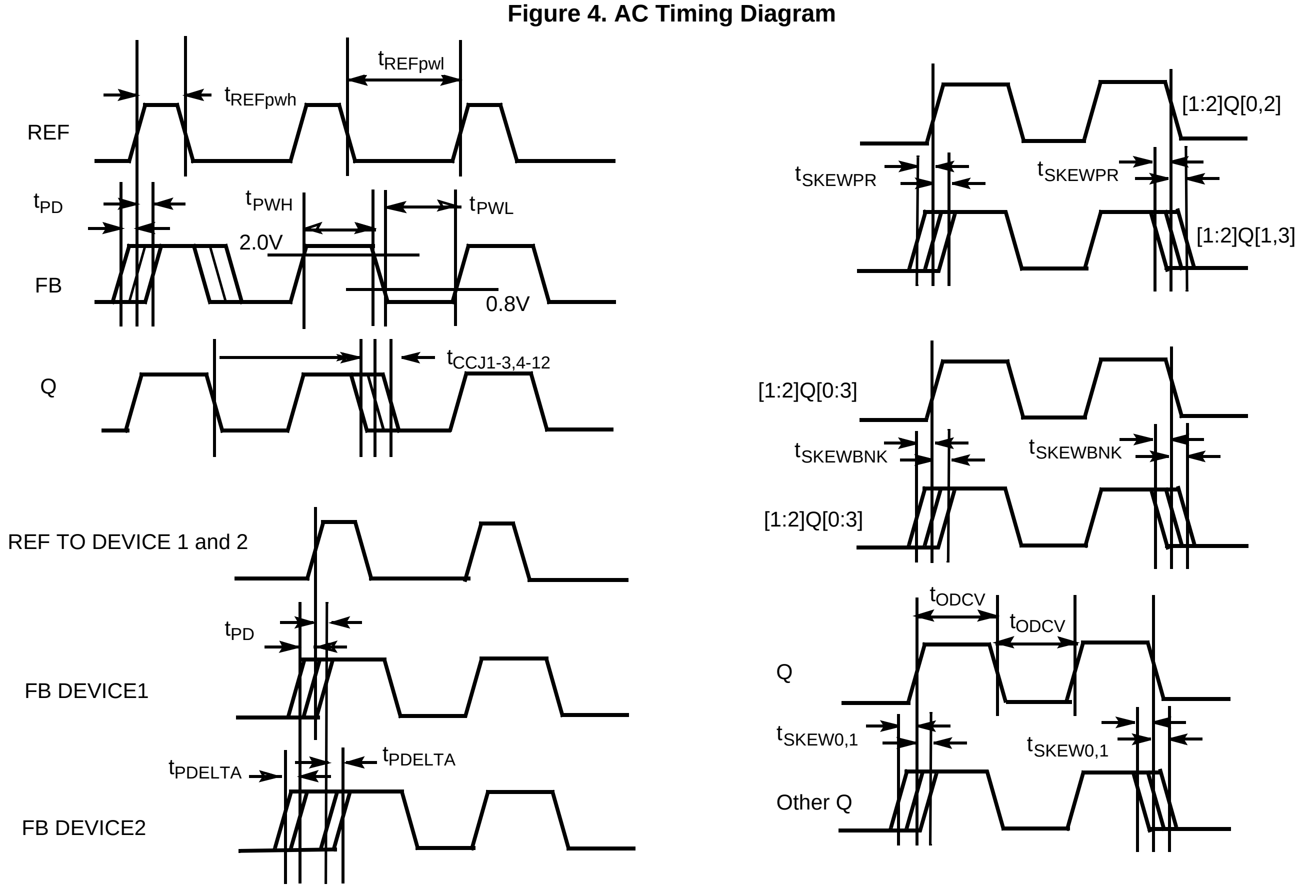
AC Test Loads and Waveform

Figure 3. AC Test Loads and Waveforms [22]



AC Timing Diagram

Figure 4. AC Timing Diagram



Notes

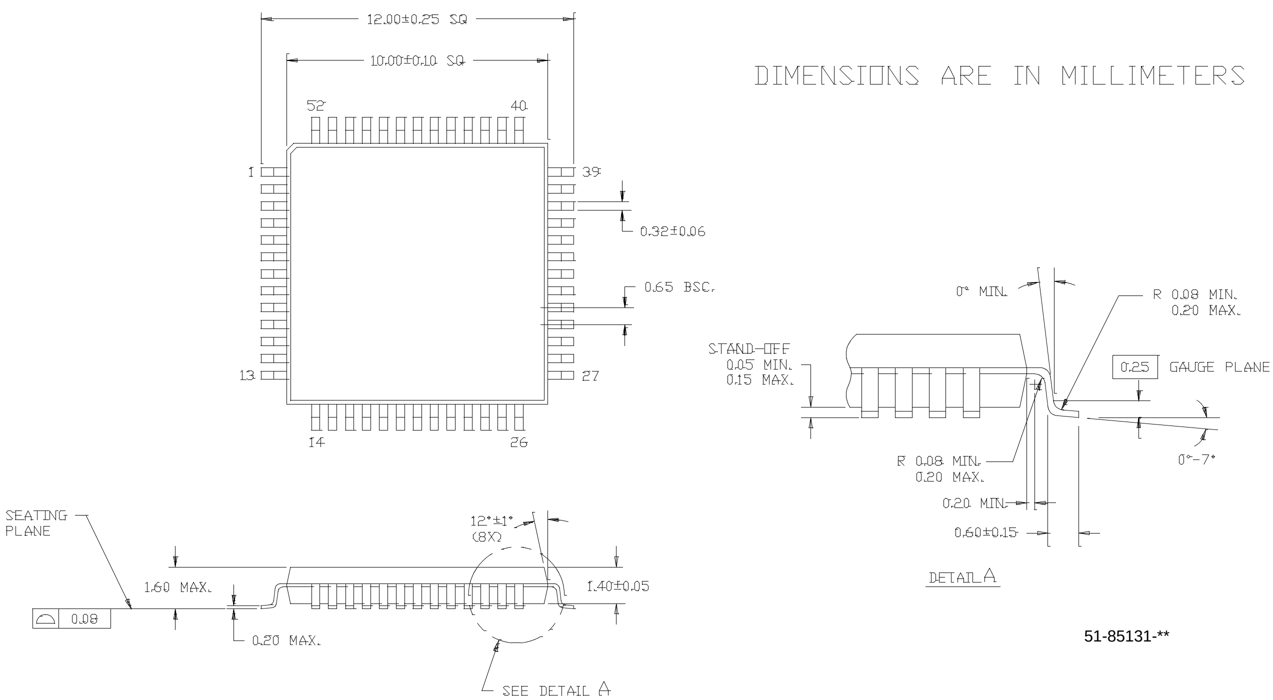
14. Guaranteed by statistical correlation. Tested initially and after any design or process changes that affects these parameters.
15. Rise and fall times are measured between 2.0V and 0.8V.
16. f_{NOM} must be within the frequency range defined by the same FS state.
17. t_{PWH} is measured at 2.0V. t_{PWL} is measured at 0.8V.
18. UI = unit interval. Examples: 1 UI is a full period. 0.1UI is 10% of period.
19. Measured at 0.5V deviation from starting voltage.
20. For t_{OZA} minimum, C_L = 0 pF. For t_{OZA} maximum, C_L= 25 pF to 185 MHz or 10 pF to 200 MHz
21. These figures are for illustration purposes only. The actual ATE loads may vary.

Ordering Information

Propagation Delay (ps)	Max. Speed (MHz)	Ordering Code	Package Name	Package Type	Operating Range
250	200	CY7B9945V-2AC	A52	52-Pb TQFP	Commercial
500	200	CY7B9945V-5AC	A52	52-Pb TQFP	Commercial
250	200	CY7B9945V-2AI	A52	52-Pb TQFP	Industrial
	200	CY7B9945V-2AIT	A52	52-PbTQFP	Industrial
500	200	CY7B9945V-5AI [22.]	A52	52-Pb TQFP	Industrial
Pb-free					
250	200	CY7B9945V-2AXC	AZ52	52-Pb TQFP	Commercial
	200	CY7B9945V-2AXCT	AZ52	52-Pb TQFP – Tape and Reel	Commercial
250	200	CY7B9945V-2AXI	AZ52	52-PbTQFP	Industrial
	200	CY7B9945V-2AXIT	AZ52	52-PbTQFP – Tape and Reel	Industrial
500	200	CY7B9945V-5AXC	AZ52	52-Pb TQFP	Commercial
	200	CY7B9945V-5AXCT	AZ52	52-Pb TQFP – Tape and Reel	Commercial

Package Diagram

Figure 5. 52 - Pin Thin Plastic Quad Flat Pack (10 x 10 x 1.4 mm) A52 and AZ52



Note
22. Not for new designs.

Document History Page

REV.	ECN NO.	Issue Date	Orig. of Change	Description of Change
Document Title: CY7B9945V RoboClock® High Speed Multi-phase PLL Clock Buffer Document Number: 38-07336				
**	111747	03/04/02	CTK	New Data Sheet
*A	116572	09/05/02	HWT	Added TTB Features
*B	119078	10/16/02	HWT	Corrected the following items in the Electrical Characteristics table: I_{IIL},I_{IIH},I_{IIM} specifications from: three level input pins excluding FBFO to FS[0:2],IF[0:3],FBDS[0:1] and FBFO to 2F[0:1],[1:2]DS[0:1],FBFO Common Mode Range (V_{COM}) from V_{CC} to V_{CC}–0.2 Corrected typo TQFP to LQFP in Features
*C	124645	03/20/03	RGL	Corrected typo LQFP to TQFP in Features
*D	128464	07/25/03	RGL	Added clock input frequency (f_{in}) specifications in the switching characteristics table.
*E	272075	See ECN	RGL	Minor Change: Fixed the Typical Outputs (Fig. 1) diagram
*F	1187144	See ECN	KVM	Updated Ordering Information table, primarily to add Pb-free devices