

16-Mbit (2M x 8) Static RAM

Features

- **High speed**
— $t_{AA} = 10 \text{ ns}$
- **Low active power**
— 990 mW (max.)
- **Operating voltages of $3.3 \pm 0.3\text{V}$**
- **2.0V data retention**
- **Automatic power-down when deselected**
- **TTL-compatible inputs and outputs**
- **Available in Pb-free and non Pb-free 54-pin TSOP II package**

Functional Description

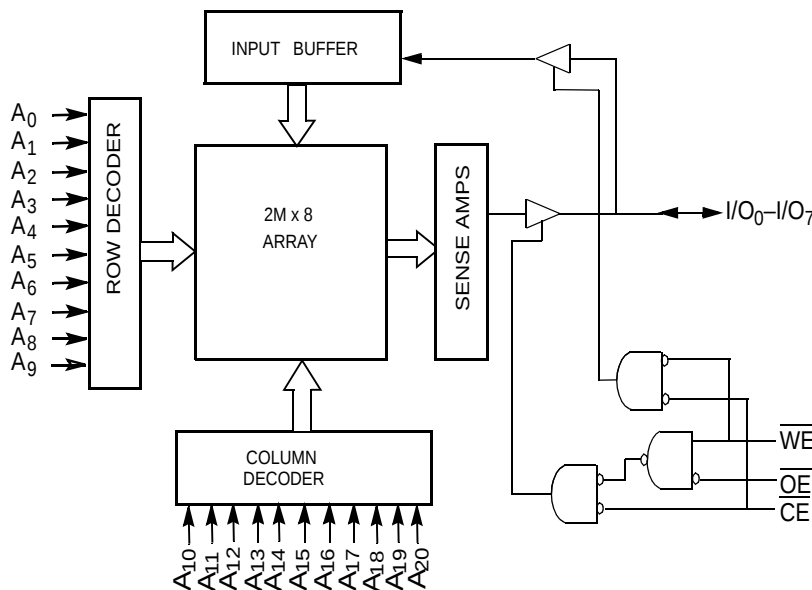
The CY7C1069BV33 is a high-performance CMOS Static RAM organized as 2,097,152 words by 8 bits. Writing to the device is accomplished by enabling the chip (by taking $\overline{\text{CE}}$ LOW) and Write Enable ($\overline{\text{WE}}$) inputs LOW.

Reading from the device is accomplished by enabling the chip ($\overline{\text{CE}}$ LOW) as well as forcing the Output Enable ($\overline{\text{OE}}$) LOW while forcing the Write Enable ($\overline{\text{WE}}$) HIGH. See the truth table at the back of this data sheet for a complete description of Read and Write modes.

The input/output pins (I/O_0 through I/O_7) are placed in a high-impedance state when the device is deselected ($\overline{\text{CE}}$ HIGH), the outputs are disabled ($\overline{\text{OE}}$ HIGH), or during a Write operation ($\overline{\text{CE}}$ LOW and $\overline{\text{WE}}$ LOW).

The CY7C1069BV33 is available in a 54-pin TSOP II package with center power and ground (revolutionary) pinout.

Logic Block Diagram



Pin Configurations^[1, 2]

54-pin TSOP II (Top View)

NC	1	54	NC
V _{CC}	2	53	V _{SS}
NC	3	52	NC
I/O ₆	4	51	I/O ₅
V _{SS}	5	50	V _{CC}
I/O ₇	6	49	I/O ₄
A ₄	7	48	A ₅
A ₃	8	47	A ₆
A ₂	9	46	A ₇
A ₁	10	45	A ₈
A ₀	11	44	A ₉
NC	12	43	NC
$\overline{\text{CE}}$	13	42	$\overline{\text{OE}}$
V _{CC}	14	41	V _{SS}
$\overline{\text{WE}}$	15	40	DNU/V _{SS}
DNU/V _{CC}	16	39	A ₂₀
A ₁₉	17	38	A ₁₀
A ₁₈	18	37	A ₁₁
A ₁₇	19	36	A ₁₂
A ₁₆	20	35	A ₁₃
A ₁₅	21	34	A ₁₄
I/O ₀	22	33	I/O ₃
V _{CC}	23	32	V _{SS}
I/O ₁	24	31	I/O ₂
NC	25	30	NC
V _{SS}	26	29	V _{CC}
NC	27	28	NC

Notes:

1. DNU/V_{CC} Pin (#16) has to be left floating or connected to V_{CC} and DNU/V_{SS} Pin (#40) has to be left floating or connected to V_{SS} to ensure proper application.
2. NC - No Connect Pins are not connected to the die.

Selection Guide

		-10	-12	Unit
Maximum Access Time		10	12	ns
Maximum Operating Current	Commercial	275	260	mA
	Industrial	275	260	
Maximum CMOS Standby Current	Commercial/Industrial	50	50	mA

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature -65°C to +150°C

Ambient Temperature with Power Applied -55°C to +125°C

Supply Voltage on V_{CC} to Relative GND^[3] -0.5V to +4.6V

DC Voltage Applied to Outputs in High-Z State^[3] -0.5V to $V_{CC} + 0.5V$

DC Input Voltage^[3] -0.5V to $V_{CC} + 0.5V$

Current into Outputs (LOW) 20 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	3.3V ± 0.3V
Industrial	-40°C to +85°C	

DC Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions	-10		-12		Unit
			Min.	Max.	Min.	Max.	
V_{OH}	Output HIGH Voltage	$V_{CC} = \text{Min.}, I_{OH} = -4.0 \text{ mA}$	2.4		2.4		V
V_{OL}	Output LOW Voltage	$V_{CC} = \text{Min.}, I_{OL} = 8.0 \text{ mA}$		0.4		0.4	V
V_{IH}	Input HIGH Voltage		2.0	$V_{CC} + 0.3$	2.0	$V_{CC} + 0.3$	V
V_{IL}	Input LOW Voltage ^[3]		-0.3	0.8	-0.3	0.8	V
I_{IX}	Input Leakage Current	$GND \leq V_I \leq V_{CC}$	-1	+1	-1	+1	μA
I_{OZ}	Output Leakage Current	$GND \leq V_{OUT} \leq V_{CC}$, Output Disabled	-1	+1	-1	+1	μA
I_{CC}	V_{CC} Operating Supply Current	$V_{CC} = \text{Max.}, f = f_{MAX} = 1/t_{RC}$		275		260	mA
		Comm'l		275		260	
I_{SB1}	Automatic CE Power-down Current — TTL Inputs	Max. V_{CC} , $CE \geq V_{IH}$ $V_{IN} \geq V_{IH}$ or $V_{IN} \leq V_{IL}$, $f = f_{MAX}$		70		70	mA
I_{SB2}	Automatic CE Power-down Current — CMOS Inputs	Max. V_{CC} , $CE \geq V_{CC} - 0.3V$, $V_{IN} \geq V_{CC} - 0.3V$, or $V_{IN} \leq 0.3V$, $f = 0$		50		50	mA

Capacitance^[4]

Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	$T_A = 25^\circ\text{C}, f = 1 \text{ MHz}, V_{CC} = 3.3V$	6	pF
C_{OUT}	I/O Capacitance		8	pF

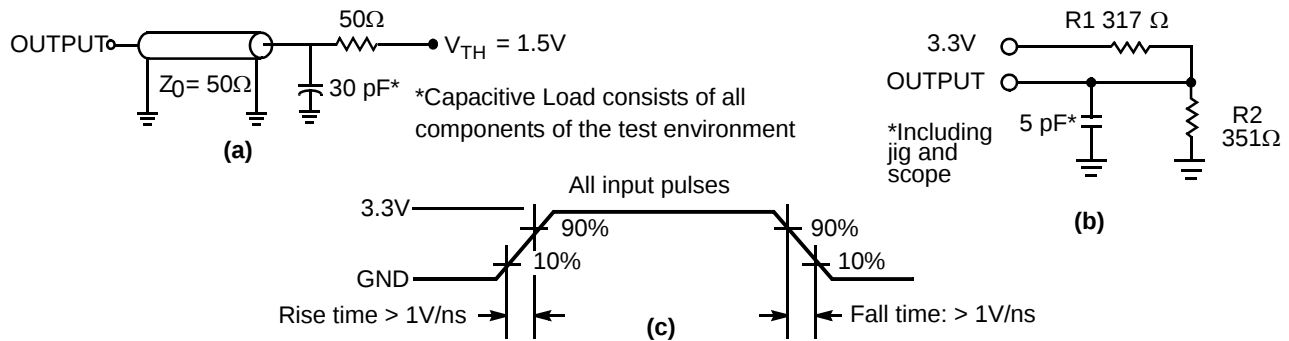
Thermal Resistance^[4]

Parameter	Description	Test Conditions	TSOP-II	Unit
Θ_{JA}	Thermal Resistance (Junction to Ambient)	Test conditions follow standard test methods and procedures for measuring thermal impedance, per EIA/JESD51.	49.95	°C/W
Θ_{JC}	Thermal Resistance (Junction to Case)		3.34	°C/W

Notes:

- $V_{IL}(\text{min.}) = -2.0V$ and $V_{IH}(\text{max.}) = V_{CC} + 0.5V$ for pulse durations of less than 20 ns.
- Tested initially and after any design or process changes that may affect these parameters.

AC Test Loads and Waveforms^[5]



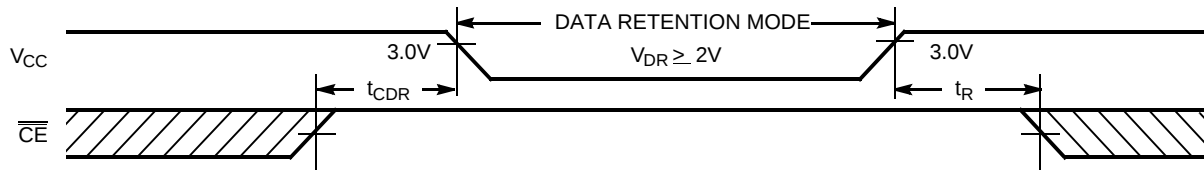
AC Switching Characteristics Over the Operating Range^[6]

Parameter	Description	−10		−12		Unit
		Min.	Max.	Min.	Max.	
Read Cycle						
t _{power}	V _{CC} (typical) to the First Access ^[7]	1		1		ms
t _{RC}	Read Cycle Time	10		12		ns
t _{AA}	Address to Data Valid		10		12	ns
t _{OHA}	Data Hold from Address Change	3		3		ns
t _{ACE}	$\overline{\text{CE}}$ LOW to Data Valid		10		12	ns
t _{DOE}	$\overline{\text{OE}}$ LOW to Data Valid		5		6	ns
t _{LZOE}	$\overline{\text{OE}}$ LOW to Low-Z ^[8]	1		1		ns
t _{HZOE}	$\overline{\text{OE}}$ HIGH to High-Z ^[8]		5		6	ns
t _{LZCE}	$\overline{\text{CE}}$ LOW to Low-Z ^[8]	3		3		ns
t _{HZCE}	$\overline{\text{CE}}$ to High-Z ^[8]		5		6	ns
t _{PU}	$\overline{\text{CE}}$ to Power-up ^[9]	0		0		ns
t _{PD}	$\overline{\text{CE}}$ to Power-down ^[9]		10		12	ns
Write Cycle ^[10, 11]						
t _{WC}	Write Cycle Time	10		12		ns
t _{SCE}	$\overline{\text{CE}}$ to Write End	7		8		ns
t _{AW}	Address Set-up to Write End	7		8		ns
t _{HA}	Address Hold from Write End	0		0		ns
t _{SA}	Address Set-up to Write Start	0		0		ns
t _{PWE}	$\overline{\text{WE}}$ Pulse Width	7		8		ns
t _{SD}	Data Set-up to Write End	5.5		6		ns
t _{HD}	Data Hold from Write End	0		0		ns
t _{LZWE}	$\overline{\text{WE}}$ HIGH to Low-Z ^[8]	3		3		ns
t _{HZWE}	$\overline{\text{WE}}$ LOW to High-Z ^[8]		5		6	ns

Notes:

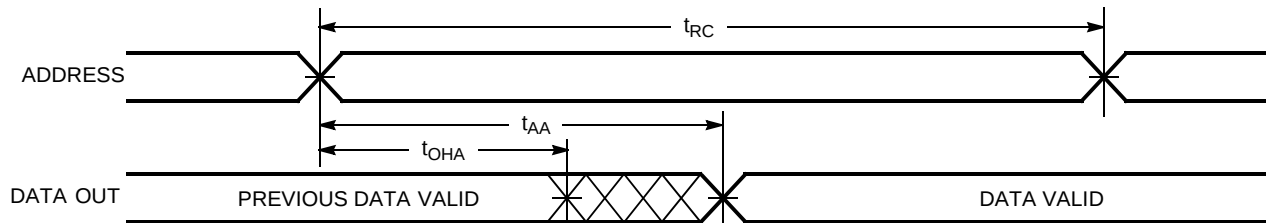
- Valid SRAM operation does not occur until the power supplies have reached the minimum operating V_{DD} (3.0V). As soon as 1ms (T_{power}) after reaching the minimum operating V_{DD}, normal SRAM operation can begin including reduction in V_{DD} to the data retention (V_{CCDR}, 2.0V) voltage.
- Test conditions assume signal transition time of 3 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified I_{OL}/I_{OH} and transmission line loads. Test conditions for the Read cycle use output loading shown in part a) of the AC Test Loads, unless specified otherwise.
- t_{POWER} gives the minimum amount of time that the power supply should be at typical VCC values until the first memory access can be performed.
- t_{HZOE}, t_{HZSCE}, t_{HZWE} and t_{LZOE}, t_{LZCE}, and t_{LZWE} are specified with a load capacitance of 5 pF as in (b) of AC Test Loads. Transition is measured ±200 mV from steady-state voltage.
- These parameters are guaranteed by design and are not tested.
- The internal Write time of the memory is defined by the overlap of $\overline{\text{CE}}$ LOW and $\overline{\text{WE}}$ LOW. $\overline{\text{CE}}$ and $\overline{\text{WE}}$ must be LOW to initiate a Write, and the transition of any of these signals can terminate the Write. The input data set-up and hold timing should be referenced to the leading edge of the signal that terminates the Write.
- The minimum Write cycle time for Write Cycle No. 3 ($\overline{\text{WE}}$ controlled, $\overline{\text{OE}}$ LOW) is the sum of t_{HZWE} and t_{SD}.

Data Retention Waveform

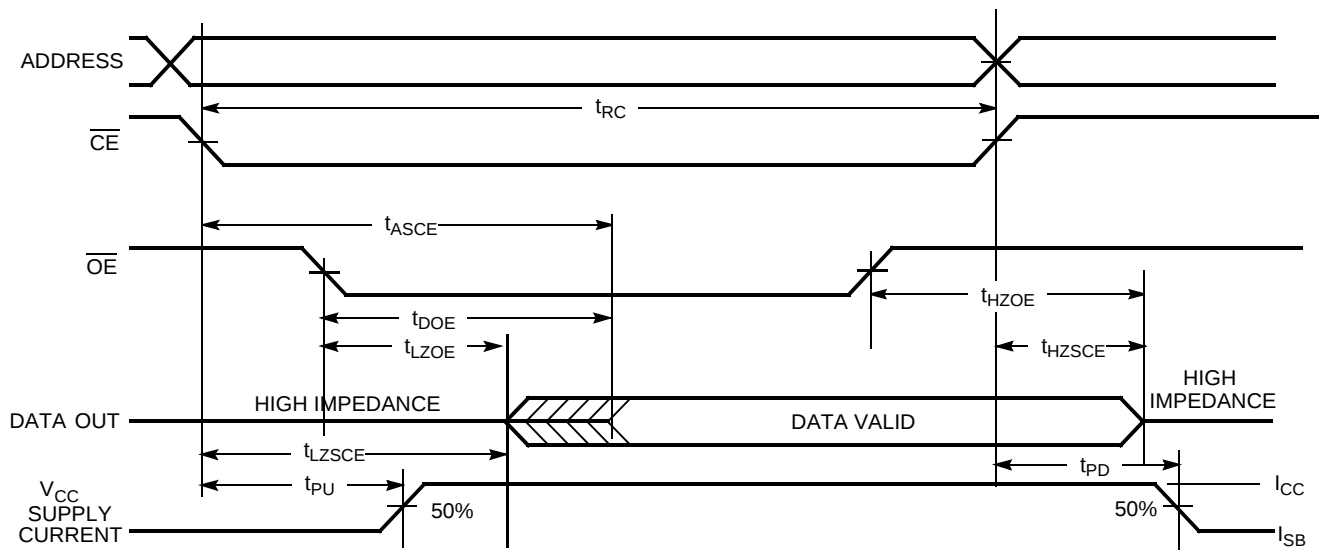


Switching Waveforms

Read Cycle No. 1^[12, 13]

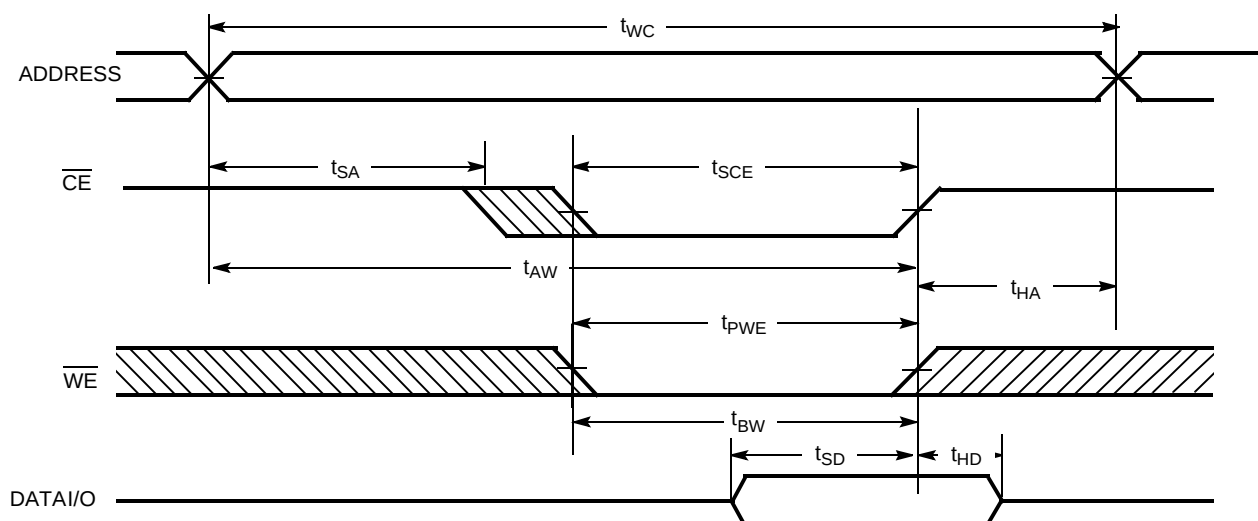
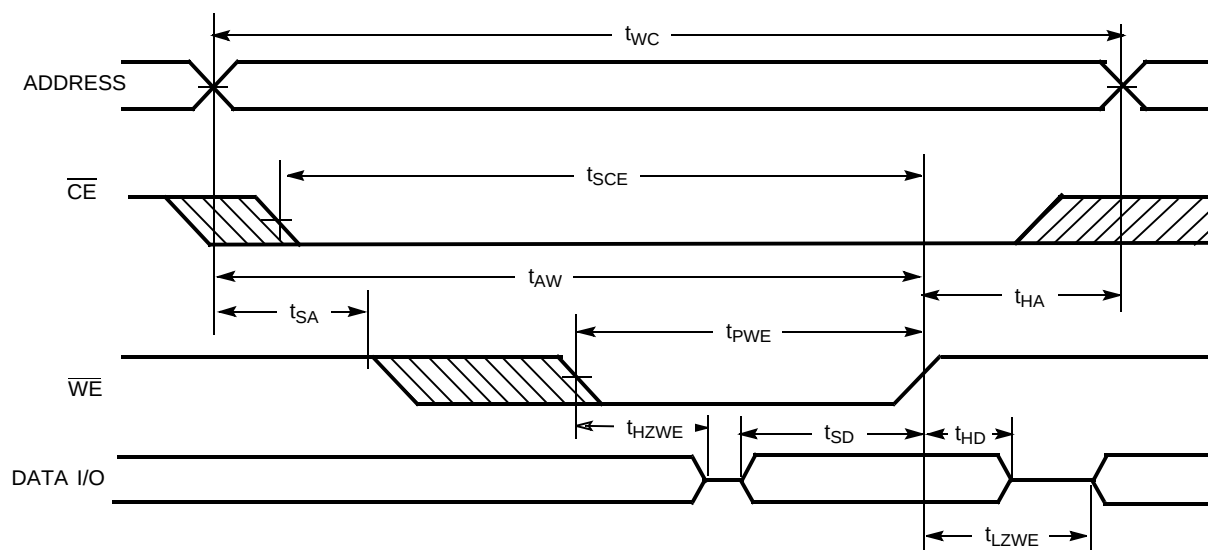


Read Cycle No. 2 ($\overline{OE}$ Controlled)^[13, 14]



Notes:

12. Device is continuously selected. $\overline{CE} = V_{IL}$.
13. $\overline{WE}$ is HIGH for Read cycle.
14. Address valid prior to or coincident with $\overline{CE}$ transition LOW.

Switching Waveforms (continued)
Write Cycle No. 1 ($\overline{\text{CE}}$ Controlled)^[15, 16]

Write Cycle No. 2 ($\overline{\text{WE}}$ Controlled, $\overline{\text{OE}}$ LOW)^[15, 16]

Truth Table

$\overline{\text{CE}}$	$\overline{\text{OE}}$	$\overline{\text{WE}}$	I/O ₀ -I/O ₇	Mode	Power
H	X	X	High-Z	Power-down	Standby (I_{SB})
L	L	H	Data Out	Read	Active (I_{CC})
L	X	L	Data In	Write	Active (I_{CC})
L	H	H	High-Z	Selected, Outputs Disabled	Active (I_{CC})

Notes:

15. Data I/O is high-impedance if $\overline{\text{OE}} = V_{\text{IH}}$.

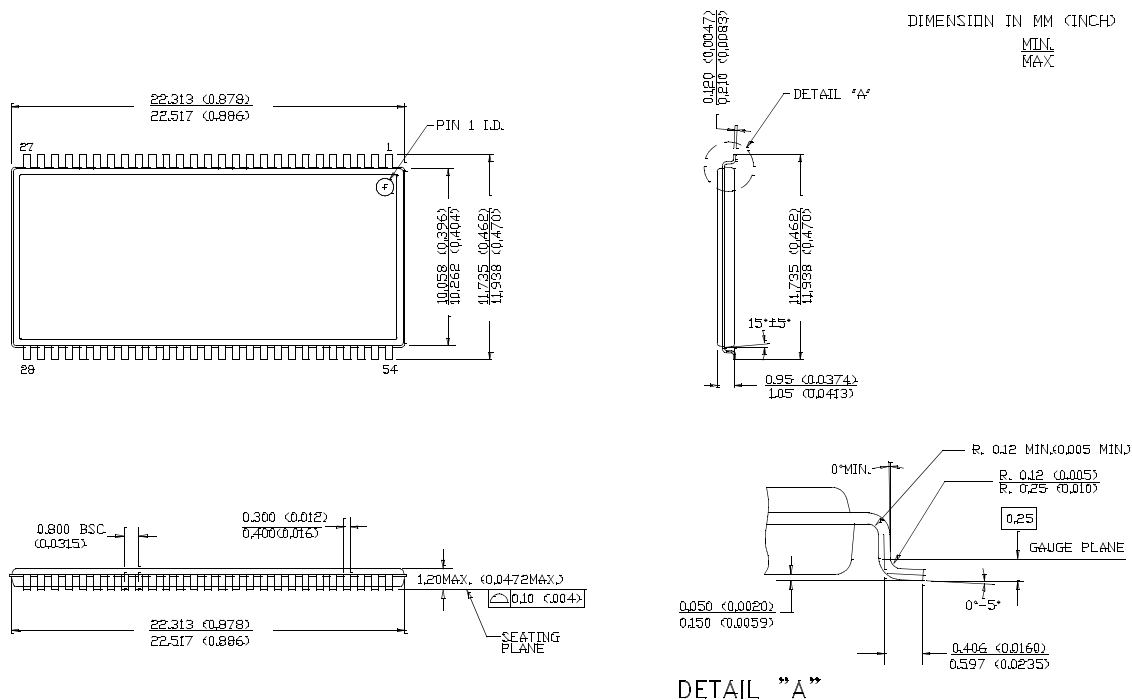
16. If CE goes HIGH simultaneously with WE going HIGH, the output remains in a high-impedance state.

Ordering Information

Speed (ns)	Ordering Code	Package Diagram	Package Type	Operating Range
10	CY7C1069BV33-10ZC	51-85160	54-pin TSOP II	Commercial
	CY7C1069BV33-10ZXC		54-pin TSOP II (Pb-free)	
	CY7C1069BV33-10ZI		54-pin TSOP II	Industrial
12	CY7C1069BV33-10ZXI		54-pin TSOP II (Pb-free)	
	CY7C1069BV33-12ZC		54-pin TSOP II	Commercial
	CY7C1069BV33-12ZXC		54-pin TSOP II (Pb-free)	
	CY7C1069BV33-12ZI		54-pin TSOP II	Industrial
	CY7C1069BV33-12ZXI		54-pin TSOP II (Pb-free)	

Package Diagram

54-pin TSOP II (51-85160)



51-85160-**

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Document History Page

Document Title: CY7C1069BV33 16-Mbit (2M x 8) Static RAM Document Number: 38-05694				
REV.	ECN NO.	Issue Date	Orig. of Change	Description of Change
**	283950	See ECN	RKF	New data sheet
*A	314014	See ECN	RKF	Final data sheet
*B	492137	See ECN	NXR	Removed 8 ns speed bin Changed the description of I_{IX} from Input Load Current to Input Leakage Current in DC Electrical Characteristics table Updated the Ordering Information Table