

MC74HC589A

8-Bit Serial or Parallel-Input/Serial-Output Shift Register with 3-State Output

High-Performance Silicon-Gate CMOS

The MC74HC589A device consists of an 8-bit storage latch which feeds parallel data to an 8-bit shift register. Data can also be loaded serially (see the Function Table). The shift register output, Q_H , is a 3-state output, allowing this device to be used in bus-oriented systems.

The HC589A directly interfaces with the SPI serial data port on CMOS MPUs and MCUs.

Features

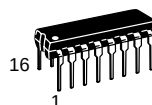
- Output Drive Capability: 15 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2 to 6 V
- Low Input Current: 1 μ A
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 526 FETs or 131.5 Equivalent Gates
- Pb-Free Packages are Available*



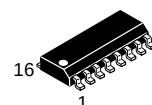
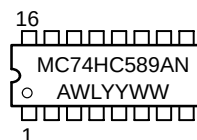
ON Semiconductor®

<http://onsemi.com>

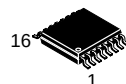
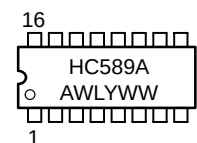
MARKING DIAGRAMS



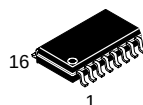
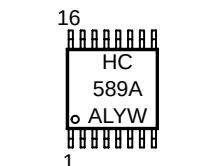
PDIP-16
N SUFFIX
CASE 648



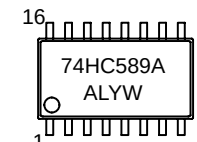
SOIC-16
D SUFFIX
CASE 751B



TSSOP-16
DT SUFFIX
CASE 948F



SOEIAJ-16
CASE 966



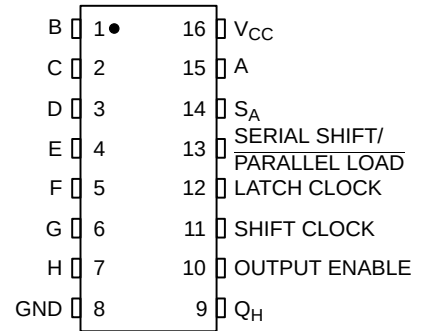
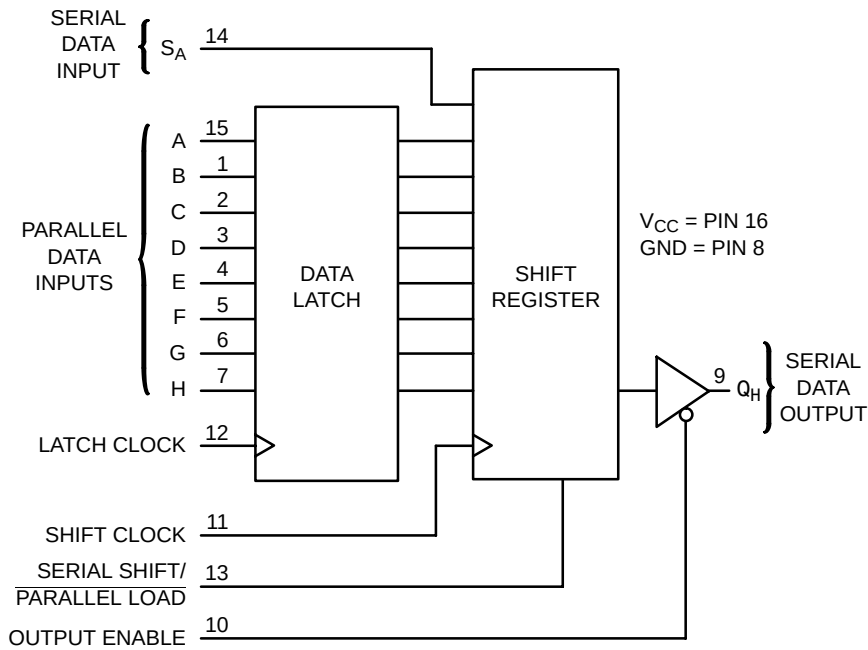
A = Assembly Location
L, WL = Wafer Lot
Y, YY = Year
W, WW = Work Week

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 2 of this data sheet.

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

MC74HC589A



ORDERING INFORMATION

Device	Package	Shipping [†]
MC74HC589AN	PDIP-16	2000 / Box
MC74HC589ANG	PDIP-16 (Pb-Free)	2000 / Box
MC74HC589AD	SOIC-16	48 Units / Rail
MC74HC589ADG	SOIC-16 (Pb-Free)	48 Units / Rail
MC74HC589ADR2	SOIC-16	2500 Tape & Reel
MC74HC589ADR2G	SOIC-16 (Pb-Free)	2500 Tape & Reel
MC74HC589ADTR2	TSSOP-16*	2500 Tape & Reel
MC74HC589AFEL	SOEIAJ-16	2000 Tape & Reel
MC74HC589AFELG	SOEIAJ-16 (Pb-Free)	2000 Tape & Reel

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

*This package is inherently Pb-Free.

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MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V _{CC}	DC Supply Voltage (Referenced to GND)	− 0.5 to + 7.0	V
V _{in}	DC Input Voltage (Referenced to GND)	− 0.5 ≤ V _{CC} + 0.5	V
V _{out}	DC Output Voltage (Referenced to GND)	− 0.5 ≤ V _{CC} + 0.5	V
I _{in}	DC Input Current, per Pin	± 20	mA
I _{out}	DC Output Current, per Pin	± 35	mA
I _{CC}	DC Supply Current, V _{CC} and GND Pins	± 75	mA
I _{GND}	DC Ground Current per Ground Pin	± 75	mA
T _{STG}	Storage Temperature Range	− 65 to + 150	°C
T _L	Lead Temperature, 1 mm from Case for 10 Seconds	260	°C
T _J	Junction Temperature Under Bias	+ 150	°C
θ _{JA}	Thermal Resistance PDIP SOIC TSSOP	78 112 148	°C/W
P _D	Power Dissipation in Still Air at 85°C PDIP SOIC TSSOP	750 500 450	mW
MSL	Moisture Sensitivity	Level 1	
F _R	Flammability Rating Oxygen Index: 30% – 35%	UL 94 V-0 @ 0.125 in	
V _{ESD}	ESD Withstand Voltage Human Body Model (Note 1) Machine Model (Note 2) Charged Device Model (Note 3)	> 4000 > 200 > 1000	V
I _{Latchup}	Latchup Performance Above V _{CC} and Below GND at 85°C (Note 4)	± 300	mA

Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

1. Tested to EIA/JESD22-A114-A.
2. Tested to EIA/JESD22-A115-A.
3. Tested to JESD22-C101-A.
4. Tested to EIA/JESD78.
5. For high frequency or heavy load considerations, see the ON Semiconductor High-Speed CMOS Data Book (DL129/D).

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V _{CC}	DC Supply Voltage (Referenced to GND)	2.0	6.0	V
V _{in} , V _{out}	DC Input Voltage, Output Voltage (Referenced to GND)	0	V _{CC}	V
T _A	Operating Temperature, All Package Types	− 55	+ 125	°C
t _r , t _f	Input Rise and Fall Time (Figure 3) V _{CC} = 2.0 V V _{CC} = 3.0 V V _{CC} = 4.5 V V _{CC} = 6.0 V	0 0 0	1000 800 500 400	ns

6. Unused inputs may not be left open. All inputs must be tied to a high-logic voltage level or a low-logic input voltage level.

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DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND, Note 7)

Symbol	Parameter	Test Conditions	V _{CC} V	Guaranteed Limit			Unit
				− 55°C to 25°C	≤ 85°C	≤ 125°C	
V _{IH}	Minimum High-Level Input Voltage	V _{out} = 0.1 V or V _{CC} − 0.1 V I _{out} ≤ 20 μA	2.0 3.0 4.5 6.0	1.5 2.1 3.15 4.2	1.5 2.1 3.15 4.2	1.5 2.1 3.15 4.2	V
V _{IL}	Maximum Low-Level Input Voltage	V _{out} = 0.1 V or V _{CC} − 0.1 V I _{out} ≤ 20 μA	2.0 3.0 4.5 6.0	0.5 0.9 1.35 1.8	0.5 0.9 1.35 1.8	0.5 0.9 1.35 1.8	V
V _{OH}	Minimum High-Level Output Voltage	V _{in} = V _{IH} or V _{IL} I _{out} ≤ 20 μA	2.0 4.5 6.0	1.9 4.4 5.9	1.9 4.4 5.9	1.9 4.4 5.9	V
		V _{in} = V _{IH} or V _{IL} I _{out} ≤ 2.4 mA	3.0	2.48	2.34	2.20	
		I _{out} ≤ 6.0 mA	4.5	3.98	3.84	3.70	
		I _{out} ≤ 7.8 mA	6.0	5.48	5.34	5.20	
V _{OL}	Maximum Low-Level Output Voltage	V _{in} = V _{IH} I _{out} ≤ 20 μA	2.0 4.5 6.0	0.1 0.1 0.1	0.1 0.1 0.1	0.1 0.1 0.1	V
		V _{in} = V _{IH} or V _{IL} I _{out} ≤ 2.4 mA	3.0	0.26	0.33	0.40	
		I _{out} ≤ 6.0 mA	4.5	0.26	0.33	0.40	
		I _{out} ≤ 7.8 mA	6.0	0.26	0.33	0.40	
I _{in}	Maximum Input Leakage Current	V _{in} = V _{CC} or GND	6.0	± 0.1	± 1.0	± 1.0	μA
I _{OZ}	Maximum Three-State Leakage Current	Output in High-Impedance State V _{in} = V _{IL} or V _{IH} V _{out} = V _{CC} or GND	6.0	± 0.5	± 5.0	± 10	μA
I _{CC}	Maximum Quiescent Supply Current (per Package)	V _{in} = V _{CC} or GND I _{out} = 0 μA	6.0	4	40	160	μA

7. Information on typical parametric values can be found in the ON Semiconductor High-Speed CMOS Data Book (DL129/D).

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AC ELECTRICAL CHARACTERISTICS ($C_L = 50$ pF, Input $t_r = t_f = 6$ ns, Notes 8 and 9)

Symbol	Parameter	V _{CC} V	Guaranteed Limit			Unit
			– 55° C to 25° C	≤ 85° C	≤ 125° C	
f_{max}	Maximum Clock Frequency (50% Duty Cycle) (Figures 4 and 10)	2.0 3.0 4.5 6.0	6.0 15 30 35	4.8 10 24 28	4.0 8.0 20 24	MHz
t_{PLH} , t_{PHL}	Maximum Propagation Delay, Latch Clock to Q _H (Figures 3 and 10)	2.0 3.0 4.5 6.0	175 100 40 30	225 110 50 40	275 125 60 50	ns
t_{PLH} , t_{PHL}	Maximum Propagation Delay, Shift Clock to Q _H (Figures 4 and 10)	2.0 3.0 4.5 6.0	160 90 30 25	200 130 40 30	240 160 48 40	ns
t_{PLH} , t_{PHL}	Maximum Propagation Delay, Serial Shift/Parallel Load to Q _H (Figures 6 and 10)	2.0 3.0 4.5 6.0	160 90 30 25	200 130 40 30	240 160 48 40	ns
t_{PLZ} , t_{PHZ}	Maximum Propagation Delay, Output Enable to Q _H (Figures 5 and 11)	2.0 3.0 4.5 6.0	150 80 27 23	170 100 30 25	200 130 40 30	ns
t_{PZL} , t_{PZH}	Maximum Propagation Delay, Output Enable to Q _H (Figures 5 and 11)	2.0 3.0 4.5 6.0	150 80 27 23	170 100 30 25	200 130 40 30	ns
t_{TLH} , t_{THL}	Maximum Output Transition Time, Any Output (Figures 3 and 10)	2.0 3.0 4.5 6.0	60 23 12 10	75 27 15 13	90 31 18 15	ns
C_{in}	Maximum Input Capacitance	–	10	10	10	pF
C_{out}	Maximum Three-State Output Capacitance (Output in High-Impedance State)	–	15	15	15	pF

8. For propagation delays with loads other than 50 pF, see the ON Semiconductor High-Speed CMOS Data Book (DL129/D).

9. Information on typical parametric values can be found in the ON Semiconductor High-Speed CMOS Data Book (DL129/D).

C _{PD}	Power Dissipation Capacitance (per Package)*	Typical @ 25° C, V _{CC} = 5.0 V	
		50	
			pF

*Used to determine the no-load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$. For load considerations, see the ON Semiconductor High-Speed CMOS Data Book (DL129/D).

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TIMING REQUIREMENTS (Input $t_r = t_f = 6$ ns, Note 10)

Symbol	Parameter	V _{CC} V	Guaranteed Limit			Unit
			– 55° C to 25° C	≤ 85° C	≤ 125° C	
t _{su}	Minimum Setup Time, A–H to Latch Clock (Figure 7)	2.0	100	125	150	ns
		3.0	40	50	60	
		4.5	20	25	30	
		6.0	17	21	26	
t _{su}	Minimum Setup Time, Serial Data Input S _A to Shift Clock (Figure 8)	2.0	100	125	150	ns
		3.0	40	50	60	
		4.5	20	25	30	
		6.0	17	21	26	
t _{su}	Minimum Setup Time, Serial Shift/Parallel Load to Shift Clock (Figure 9)	2.0	100	125	150	ns
		3.0	40	50	60	
		4.5	20	25	30	
		6.0	17	21	26	
t _h	Minimum Hold Time, Latch Clock to A–H (Figure 7)	2.0	25	30	40	ns
		3.0	10	12	15	
		4.5	5	6	8	
		6.0	5	6	7	
t _h	Minimum Hold Time, Shift Clock to Serial Data Input S _A (Figure 8)	2.0	5	5	5	ns
		3.0	5	5	5	
		4.5	5	5	5	
		6.0	5	5	5	
t _w	Minimum Pulse Width, Shift Clock (Figure 4)	2.0	75	95	110	ns
		3.0	40	50	60	
		4.5	15	19	23	
		6.0	13	16	19	
t _w	Minimum Pulse Width, Latch Clock (Figure 3)	2.0	80	100	120	ns
		3.0	40	50	60	
		4.5	16	20	24	
		6.0	14	17	20	
t _w	Minimum Pulse Width, Serial Shift/Parallel Load (Figure 6)	2.0	80	100	120	ns
		3.0	40	50	60	
		4.5	16	20	24	
		6.0	14	17	20	
t _r , t _f	Maximum Input Rise and Fall Times (Figure 3)	2.0	1000	1000	1000	ns
		3.0	800	800	800	
		4.5	500	500	500	
		6.0	400	400	400	

10. Information on typical parametric values can be found in the ON Semiconductor High-Speed CMOS Data Book (DL129/D).

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FUNCTION TABLE

Operation	Inputs						Resulting Function		
	Output Enable	Serial Shift/ Parallel Load	Latch Clock	Shift Clock	Serial Input S_A	Parallel Inputs A-H	Data Latch Contents	Shift Register Contents	Output Q_H
Force Output into High Impedance State	H	X	X	X	X	X	X	X	Z
Load Parallel Data into Data Latch	L	H	$\nearrow$	L, H, $\nearrow$	X	a-h	a-h	U	U
Transfer Latch Contents to Shift Register	L	L	L, H, $\nearrow$	X	X	X	U	$LR_N \rightarrow SR_N$	LR_H
Contents of Input Latch and Shift Register are Unchanged	L	H	L, H, $\nearrow$	L, H, $\nearrow$	X	X	U	U	U
Load Parallel Data into Data Latch and Shift Register	L	L	$\nearrow$	X	X	a-h	a-h	a-h	h
Shift Serial Data into Shift Register	L	H	X	$\nearrow$	D	X	*	$SR_A = D, SR_N \rightarrow SR_{N+1}$	$SR_G \rightarrow SR_H$
Load Parallel Data in Data Latch and Shift Serial Data into Shift Register	L	H	$\nearrow$	$\nearrow$	D	a-h	a-h	$SR_A = D, SR_N \rightarrow SR_{N+1}$	$SR_G \rightarrow SR_H$

LR = latch register contents

SR = shift register contents

a-h = data at parallel data inputs A-H

D = data (L, H) at serial data input S_A

U = remains unchanged

X = don't care

Z = high impedance

* = depends on Latch Clock input

Switching Waveforms

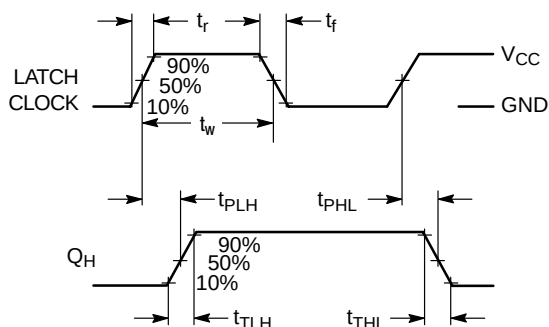


Figure 3. (Serial Shift/Parallel Load = L)

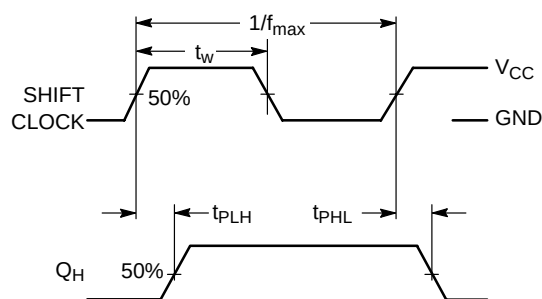


Figure 4. (Serial Shift/Parallel Load = H)

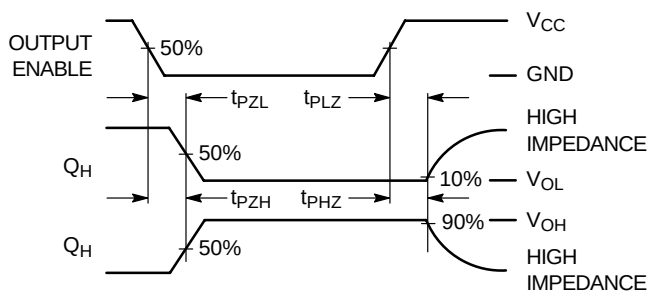


Figure 5.

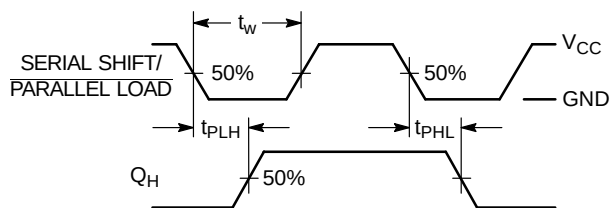


Figure 6.

Switching Waveforms

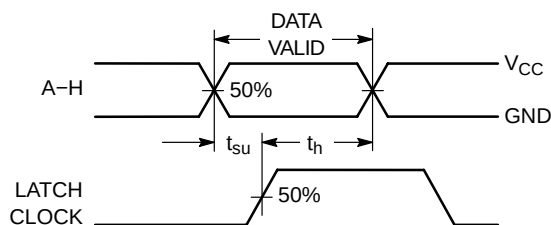


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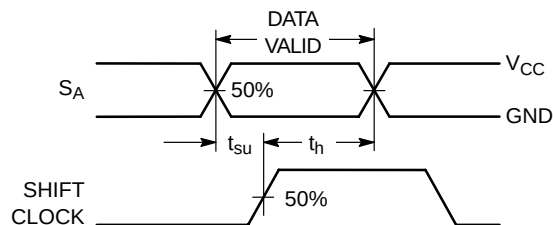


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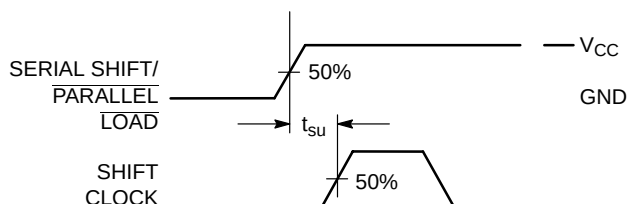
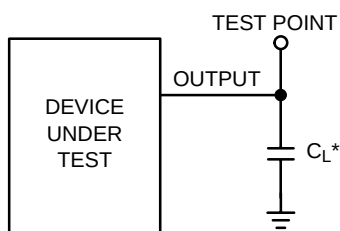
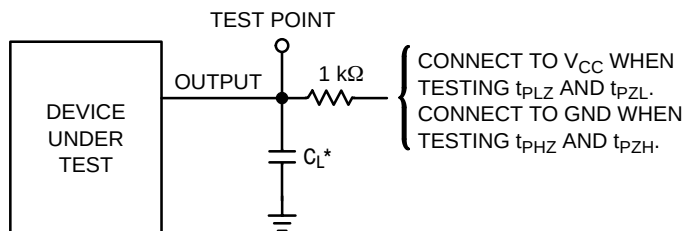


Figure 9.



*Includes all probe and jig capacitance.

Figure 10. Test Circuit



*Includes all probe and jig capacitance.

Figure 11. Test Circuit

Pin Descriptions

Data Inputs

A, B, C, D, E, F, G, H (Pins 15, 1, 2, 3, 4, 5, 6, 7)

Parallel data inputs. Data on these inputs are stored in the data latch on the rising edge of the Latch Clock input.

S_A (Pin 14)

Serial data input. Data on this input is shifted into the shift register on the rising edge of the Shift Clock input if Serial Shift/Parallel Load is high. Data on this input is ignored when Serial Shift/Parallel Load is low.

Control Inputs

Serial Shift/Parallel Load (Pin 13)

Shift register mode control. When a high level is applied to this pin, the shift register is allowed to serially shift data. When a low level is applied to this pin, the shift register accepts parallel data from the data latch.

Shift Clock (Pin 11)

Serial shift clock. A low-to-high transition on this input shifts data on the serial data input into the shift register and

data in stage H is shifted out Q_H, being replaced by the data previously stored in stage G.

Latch Clock (Pin 12)

Data latch clock. A low-to-high transition on this input loads the parallel data on inputs A-H into the data latch.

Output Enable (Pin 10)

Active-low output enable A high level applied to this pin forces the Q_H output into the high impedance state. A low level enables the output. This control does not affect the state of the input latch or the shift register.

Output

Q_H (Pin 9)

Serial data output. This pin is the output from the last stage of the shift register. This is a 3-state output.

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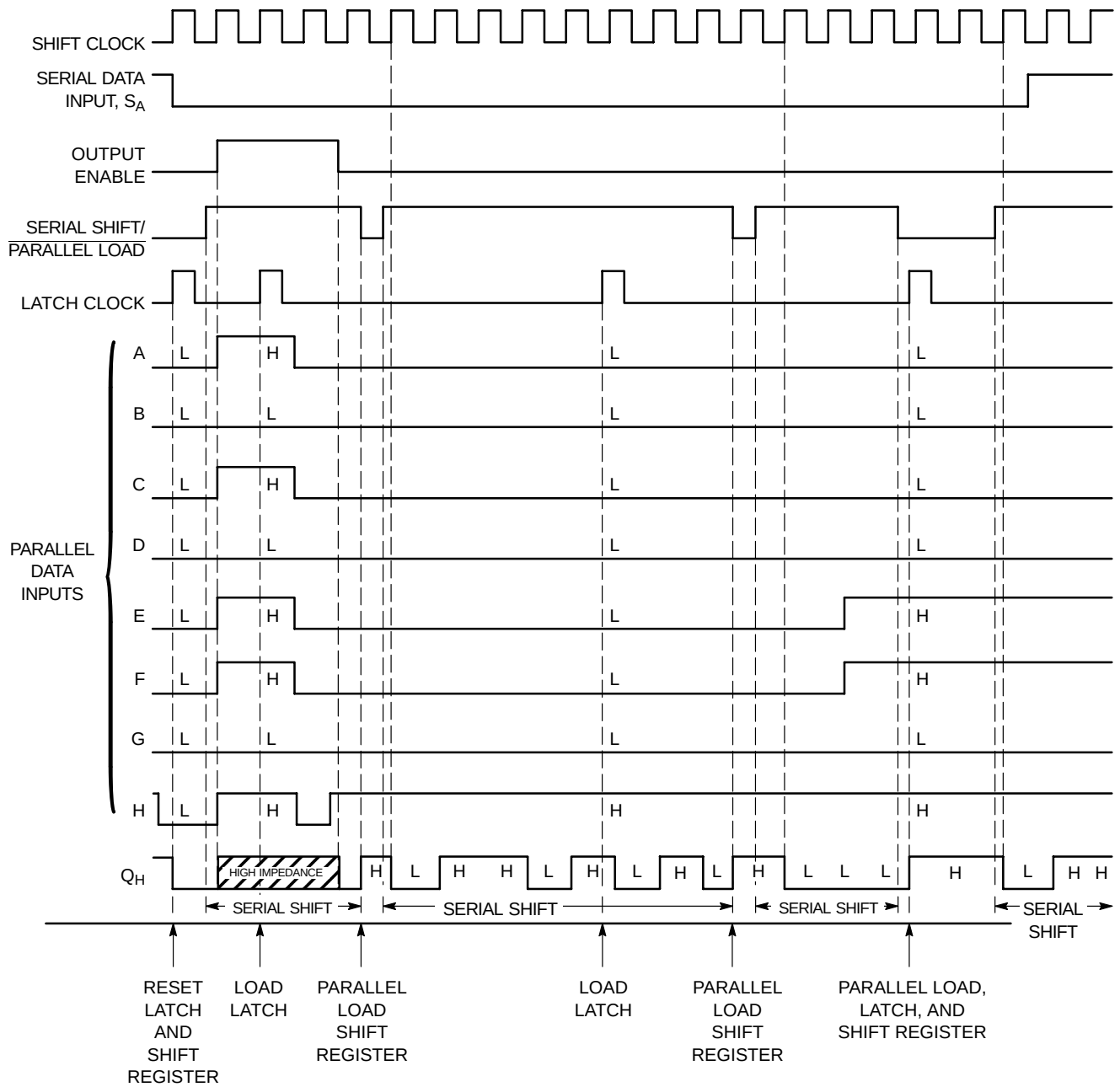
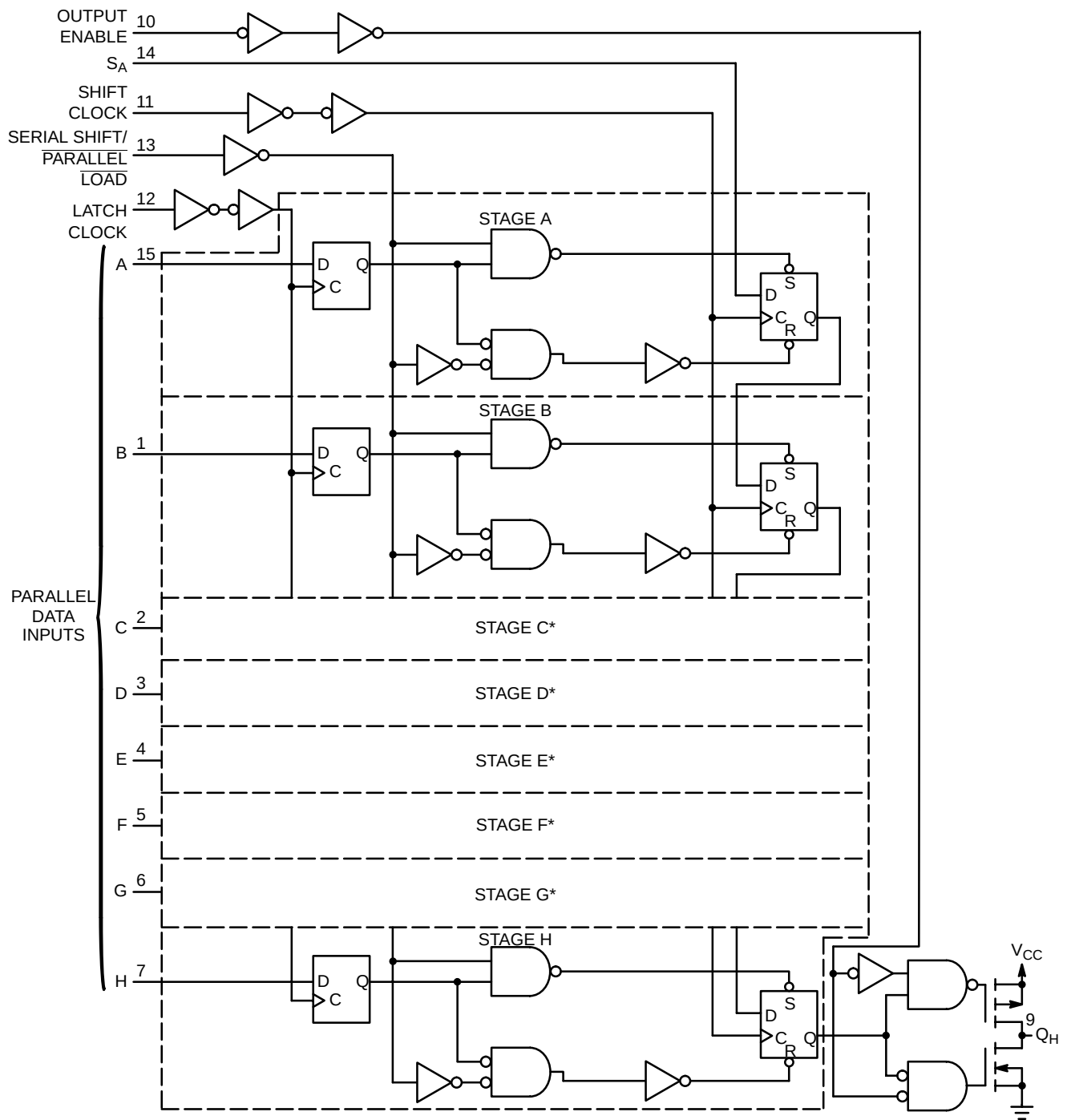


Figure 12. Timing Diagram

MC74HC589A



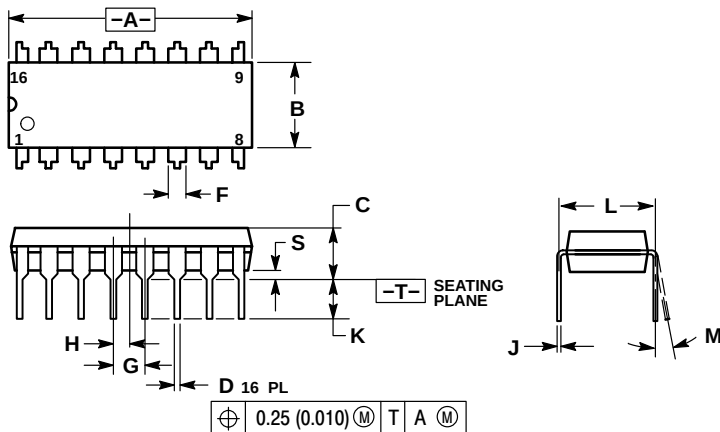
*Stages C thru G (not shown in detail) are identical to stages A and B above.

Figure 13. Logic Detail

MC74HC589A

PACKAGE DIMENSIONS

PDIP-16
N SUFFIX
CASE 648-08
ISSUE T

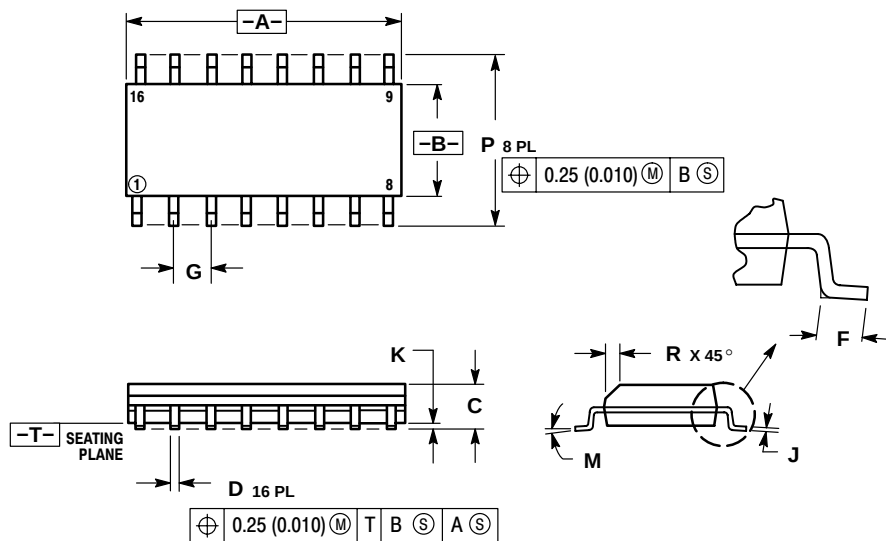


NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.
5. ROUNDED CORNERS OPTIONAL.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.740	0.770	18.80	19.55
B	0.250	0.270	6.35	6.85
C	0.145	0.175	3.69	4.44
D	0.015	0.021	0.39	0.53
F	0.040	0.70	1.02	1.77
G	0.100 BSC		2.54 BSC	
H	0.050 BSC		1.27 BSC	
J	0.008	0.015	0.21	0.38
K	0.110	0.130	2.80	3.30
L	0.295	0.305	7.50	7.74
M	0°	10°	0°	10°
S	0.020	0.040	0.51	1.01

SOIC-16
D SUFFIX
CASE 751B-05
ISSUE J



NOTES:

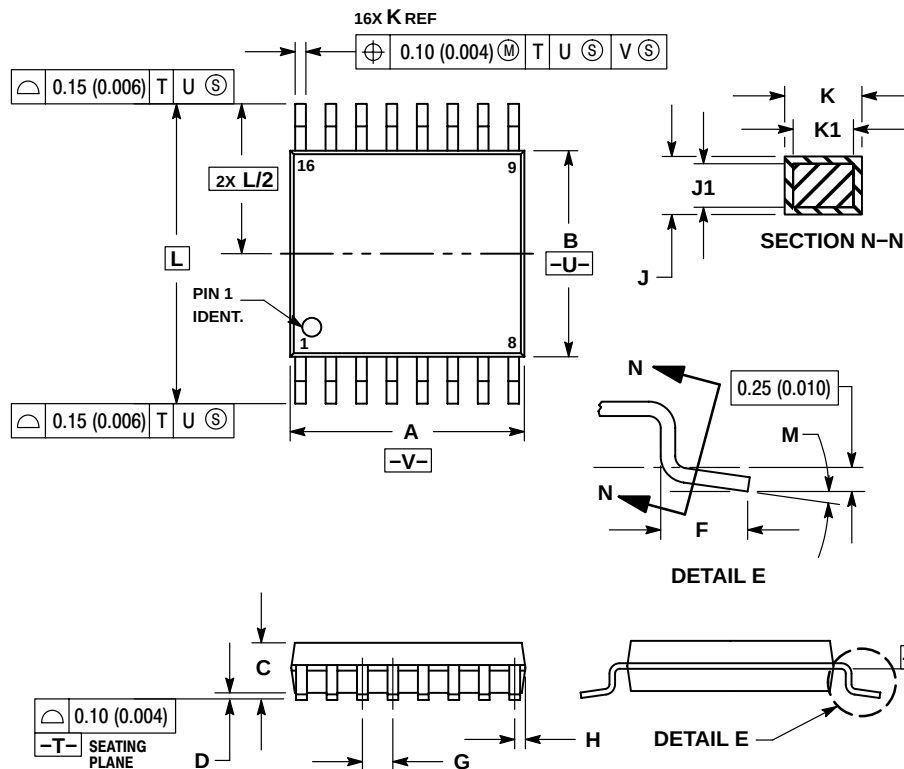
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	9.80	10.00	0.386	0.393
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	5.80	6.20	0.229	0.244
R	0.25	0.50	0.010	0.019

MC74HC589A

PACKAGE DIMENSIONS

TSSOP-16
DT SUFFIX
CASE 948F-01
ISSUE A



NOTES:

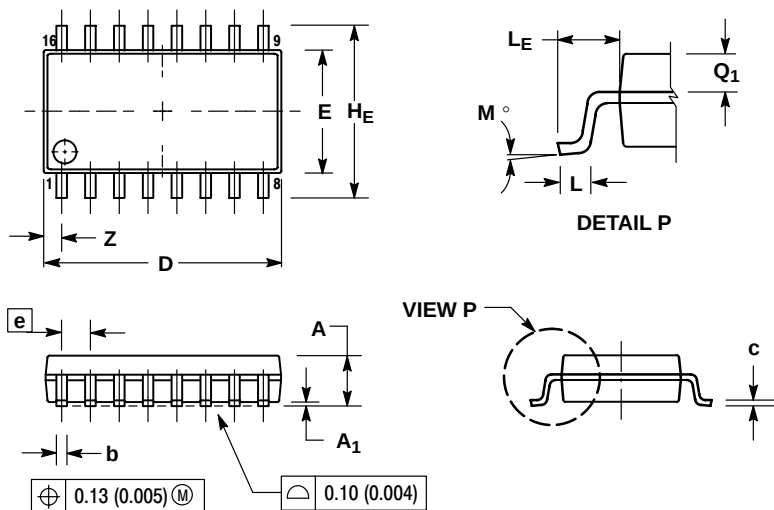
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH. PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.90	5.10	0.193	0.200
B	4.30	4.50	0.169	0.177
C	---	1.20	---	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.18	0.28	0.007	0.011
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0°	8°	0°	8°

MC74HC589A

PACKAGE DIMENSIONS

SOEIAJ-16
CASE 966-01
ISSUE O



NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS AND ARE MEASURED AT THE PARTING LINE. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
5. THE LEAD WIDTH DIMENSION (b) DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE LEAD WIDTH DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSIONS AND ADJACENT LEAD TO BE 0.46 (0.018).

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	---	2.05	---	0.081
A ₁	0.05	0.20	0.002	0.008
b	0.35	0.50	0.014	0.020
c	0.18	0.27	0.007	0.011
D	9.90	10.50	0.390	0.413
E	5.10	5.45	0.201	0.215
e	1.27 BSC		0.050 BSC	
H _E	7.40	8.20	0.291	0.323
L	0.50	0.85	0.020	0.033
L _E	1.10	1.50	0.043	0.059
M	0 °	10 °	0 °	10 °
Q ₁	0.70	0.90	0.028	0.035
Z	---	0.78	---	0.031

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