Document Title

256K x8 bit Low Power and Low Voltage Full CMOS Static RAM

Revision History

Revision No.	History		Draft Date	Remark
0.0	Initial Draft		Oct. 31, 2007	
0.1	0.1 Revision	Fix typo error	Nov. 16, 2007	

Emerging Memory & Logic Solutions Inc.
4F Korea Construction Financial Cooperative B/D, 301-1 Yeon-Dong, Jeju-Si, Jeju-Do, Rep.of Korea Zip Code : 690-719
Tel : +82-64-740-1712 Fax : +82-64-740-1749~1750 / Homepage : www.emlsi.com

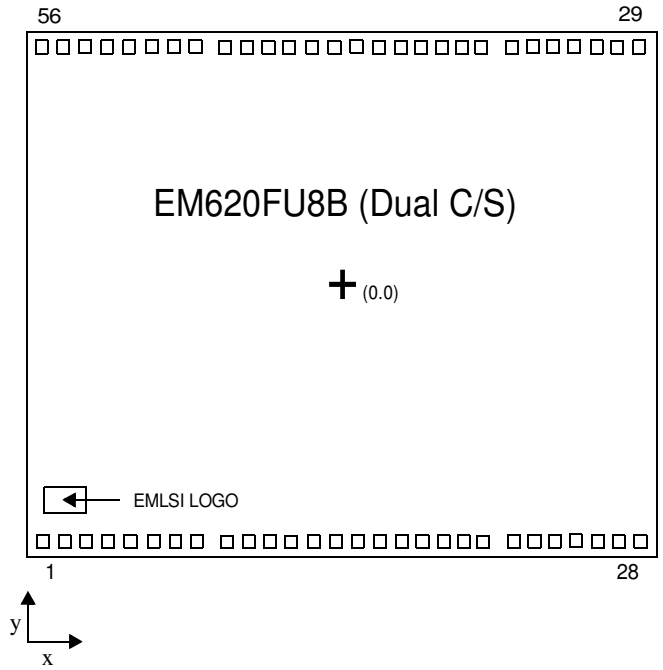
256K x8 Bit Low Power and Low Voltage CMOS Static RAM

FEATURES

- Process Technology : 0.15µm Full CMOS
- Organization :256K x8
- Power Supply Voltage
  => EM620FU8B : 2.7~3.3V
- Low Data Retention Voltage : 1.5V
- Three state output and TTL Compatible
- Packaged product designed for 45/55/70ns

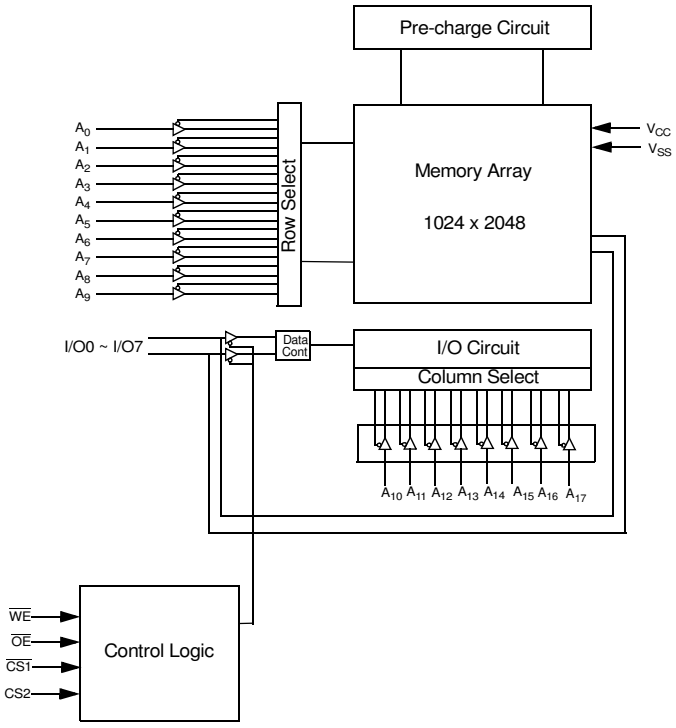
GENERAL PHYSICAL SPECIFICATIONS

- Backside die surface of polished bare silicon
- Typical Die Thickness = 725um +/-15um
- Typical top-level metallization :
  => Metal (Ti/AlCu/TiN/ARC SiON/SiO2) : 5.2K Angstroms
- Topside Passivation :
  => Passivation (HDP/pNIT/PIQ) : 5.4K Angstroms
- Wafer diameter : 8 inch



PAD DESCRIPTIONS

Name	Function	Name	Function
$\overline{CS1}$,CS2	Chip select inputs	Vcc	Power Supply
$\overline{OE}$	Output Enable input	Vss	Ground
$\overline{WE}$	Write Enable input	NC	No Connection
A0~A17	Address Inputs		
I/O0~I/O7	Data Inputs/Outputs		



BONDING INSTRUCTIONS

The 2M full CMOS SRAM die has total 56pads. Refer to the bond pad location and identification table for X, Y coordinates. EMLSI recommends using a bond wire on back side of die onto Vss bond pad for improved noise immunity.

ABSOLUTE MAXIMUM RATINGS *

Parameter	Symbol	Minimum	Unit
Voltage on Any Pin Relative to Vss	V_{IN}, V_{OUT}	-0.2 to 4.0V	V
Voltage on Vcc supply relative to Vss	V_{CC}	-0.2 to 4.0V	V
Power Dissipation	P_D	1.0	W
Operating Temperature	T_A	-40 to 85	^oC

* Stresses greater than those listed above “Absolute Maximum Ratings” may cause permanent damage to the device. Functional operation should be restricted to recommended operating condition. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

FUNCTIONAL DESCRIPTION

$\overline{CS1}$	CS2	$\overline{OE}$	$\overline{WE}$	I/O_{0-7}	Mode	Power
H	X	X	X	High-Z	Deselected	Stand by
X	L	X	X	High-Z	Deselected	Stand by
L	H	H	H	High-Z	Output Disabled	Active
L	H	L	H	Data Out	Read	Active
L	H	X	L	Data In	Write	Active

Note: X means don’t care. (Must be low or high state)

RECOMMENDED DC OPERATING CONDITIONS [1)]

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}	2.7	3.0	3.3	V
Ground	V_{SS}	0	0	0	V
Input high voltage	V_{IH}	2.0	-	V_{CC} + 0.2[2)]	V
Input low voltage	V_{IL}	-0.2[3)]	-	0.6	V

1. TA= -40 to 85°C, otherwise specified
2. Overshoot: Vcc +2.0 V in case of pulse width ≤ 20ns
3. Undershoot: -2.0 V in case of pulse width ≤ 20ns
4. Overshoot and undershoot are sampled, not 100% tested.

CAPACITANCE[1)] (f =1MHz, T_A=25°C)

Item	Symbol	Test Condition	Min	Max	Unit
Input capacitance	C_{IN}	V_{IN}=0V	-	8	pF
Input/Ouput capacitance	C_{IO}	V_{IO}=0V	-	10	pF

1. Capacitance is sampled, not 100% tested.

DC AND OPERATING CHARACTERISTICS

Parameter	Symbol	Test Conditions		Min	Typ	Max	Unit
Input leakage current	I_{LI}	V_{IN}=V_{SS} to V_{CC}		-1	-	1	uA
Output leakage current	I_{LO}	$\overline{CS1}$=V_{IH} or CS2=V_{IL} or $\overline{OE}$=V_{IH} or $\overline{WE}$=V_{IL} V_{IO}=V_{SS} to V_{CC}		-1	-	1	uA
Operating power supply	I_{CC}	I_{IO}=0mA, $\overline{CS1}$=V_{IL}, CS2=$\overline{WE}$=V_{IH}, V_{IN}=V_{IH} or V_{IL}		-	-	3	mA
Average operating current	I_{CC1}	Cycle time=1μs, 100% duty, I_{IO}=0mA, $\overline{CS1}$≤0.2V, CS2≥V_{CC}-0.2V, V_{IN}≤0.2V or V_{IN}≥V_{CC}-0.2V		-	-	3	mA
	I_{CC2}	Cycle time = Min, I_{IO}=0mA, 100% duty, $\overline{CS1}$=V_{IL}, CS2=V_{IH}, V_{IN}=V_{IL} or V_{IH}	45ns	-	-	35	mA
			55ns	-	-	30	
			70ns	-	-	25	
Output low voltage	V_{OL}	I_{OL} = 2.1mA		-	-	0.4	V
Output high voltage	V_{OH}	I_{OH} = -1.0mA		2.4	-	-	V
Standby Current (TTL)	I_{SB}	$\overline{CS1}$=V_{IH}, CS2=V_{IL}, Other inputs=V_{IH} or V_{IL}		-	-	0.3	mA
Standby Current (CMOS)	I_{SB1}	$\overline{CS1}$≥V_{CC}-0.2V, CS2≥V_{CC}-0.2V ($\overline{CS}$ controlled) or 0V≤CS2≤0.2V (CS2 controlled), Other inputs = 0~V_{CC} (Typ. condition : V_{CC}=3.0V @ 25°C) (Max. condition : V_{CC}=3.3V @ 85°C)	LF	-	1[1)]	10	uA

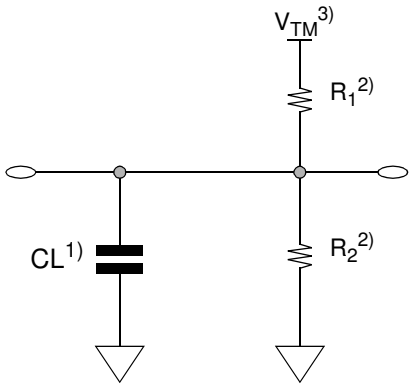
NOTES

1. Typical values are measured at Vcc=3.0V, T_A=25°C and not 100% tested.

AC OPERATING CONDITIONS

Test Conditions (Test Load and Test Input/Output Reference)

Input Pulse Level : 0.4V to 2.2V
Input Rise and Fall Time : 5ns
Input and Output reference Voltage : 1.5V
Output Load (See right) : $CL^{1)}$ = 100pF + 1 TTL
$CL^{1)}$ = 30pF + 1 TTL (only 45ns part)



1. Including scope and Jig capacitance
2. R_1=3070 ohm, R_2=3150 ohm
3. V_{TM}=2.8V
4. CL = 5pF + 1 TTL (measurement with $t_{LZ1,2}$, $t_{HZ1,2}$, t_{OLZ}, t_{OHZ}, t_{WHZ})

READ CYCLE (V_{CC} = 2.7V to 3.3V, Gnd = 0V, T_A = -40°C to +85°C)

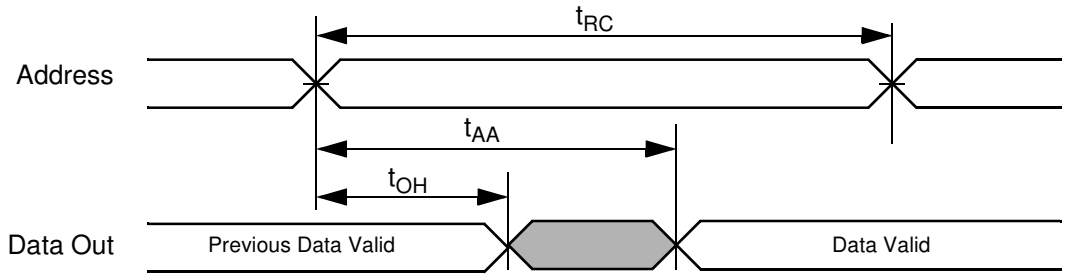
Parameter	Symbol	45ns		55ns		70ns		Unit
		Min	Max	Min	Max	Min	Max	
Read cycle time	t_{RC}	45	-	55	-	70	-	ns
Address access time	t_{AA}	-	45	-	55	-	70	ns
Chip select to output	t_{CO1}, t_{CO2}	-	45	-	55	-	70	ns
Output enable to valid output	t_{OE}	-	25	-	25	-	35	ns
Chip select to low-Z output	t_{LZ1}, t_{LZ2}	10	-	10	-	10	-	ns
Output enable to low-Z output	t_{OLZ}	5	-	5	-	5	-	ns
Chip disable to high-Z output	t_{HZ1}, t_{HZ2}	0	20	0	20	0	25	ns
Output disable to high-Z output	t_{OHZ}	0	15	0	20	0	25	ns
Output hold from address change	t_{OH}	10	-	10	-	10	-	ns

WRITE CYCLE (V_{CC} = 2.7V to 3.3V, Gnd = 0V, T_A = -40°C to +85°C)

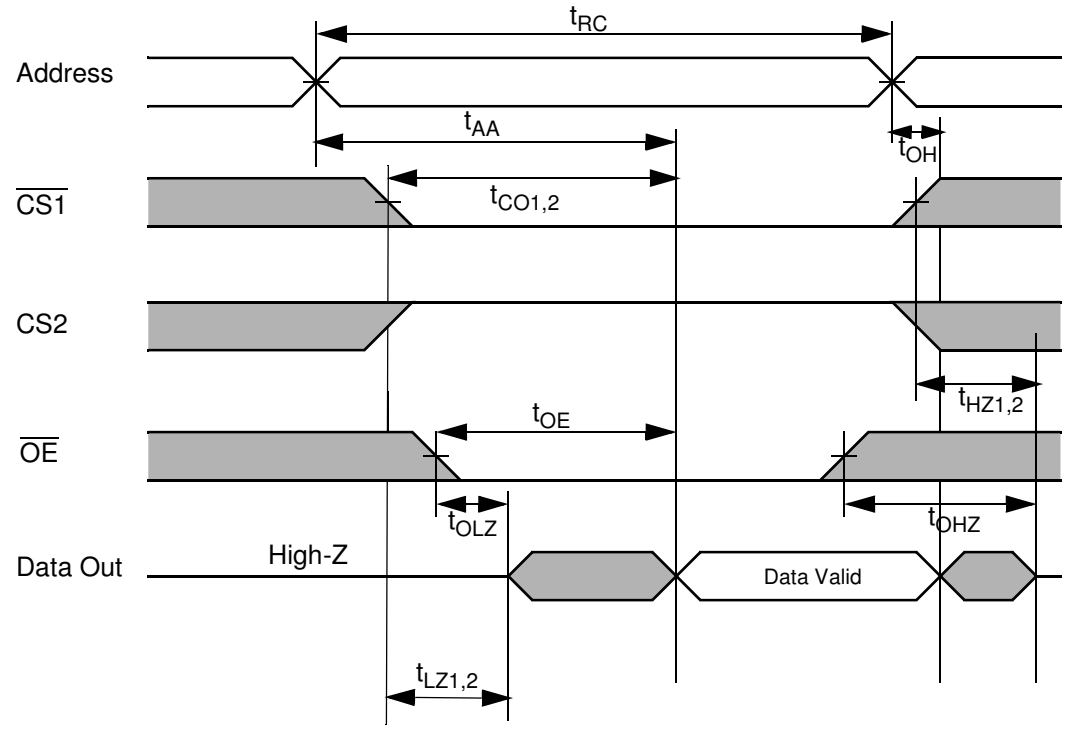
Parameter	Symbol	45ns		55ns		70ns		Unit
		Min	Max	Min	Max	Min	Max	
Write cycle time	t_{WC}	45	-	55	-	70	-	ns
Chip select to end of write	t_{CW1}, t_{CW2}	45	-	45	-	60	-	ns
Address setup time	t_{AS}	0	-	0	-	0	-	ns
Address valid to end of write	t_{AW}	45	-	45	-	60	-	ns
Write pulse width	t_{WP}	35	-	40	-	50	-	ns
Write recovery time	t_{WR}	0	-	0	-	0	-	ns
Write to ouput high-Z	t_{WHZ}	0	15	0	20	0	20	ns
Data to write time overlap	t_{DW}	25		25		30		ns
Data hold from write time	t_{DH}	0	-	0	-	0	-	ns
End write to output low-Z	t_{OW}	5	-	5	-	5	-	ns

TIMING DIAGRAMS

TIMING WAVEFORM OF READ CYCLE(1) (Address Controlled, $\overline{CS1}$=$\overline{OE}$=V_{IL}, CS2=$\overline{WE}$=V_{IH})



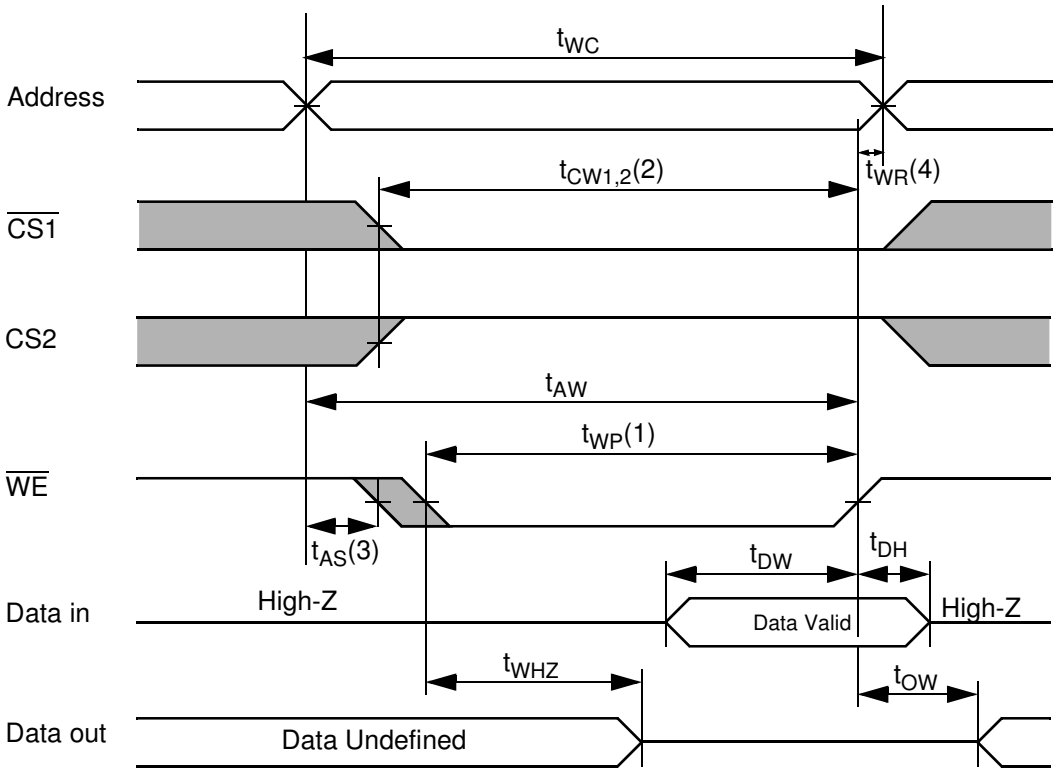
TIMING WAVEFORM OF READ CYCLE(2) ($\overline{WE}$ = V_{IH})



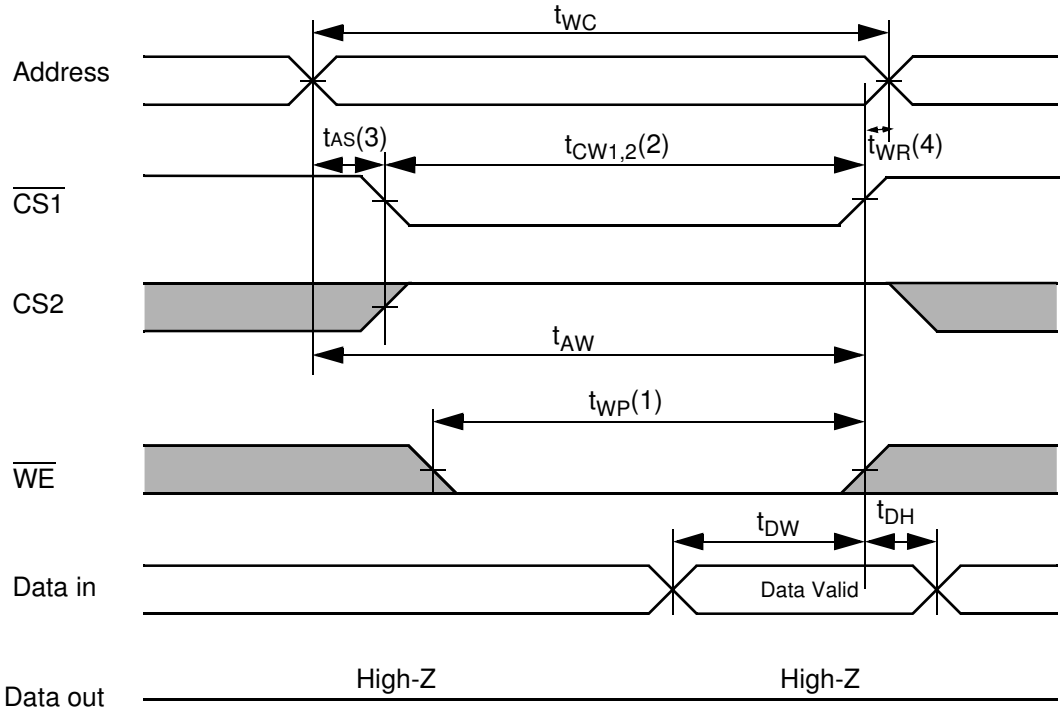
NOTES (READ CYCLE)

1. $t_{HZ1,2}$ and t_{OHZ} are defined as the outputs achieve the open circuit conditions and are not referenced to output voltage levels.
2. At any given temperature and voltage condition, $t_{HZ1,2}$(Max.) is less than $t_{LZ1,2}$(Min.) both for a given device and from device to device interconnection.

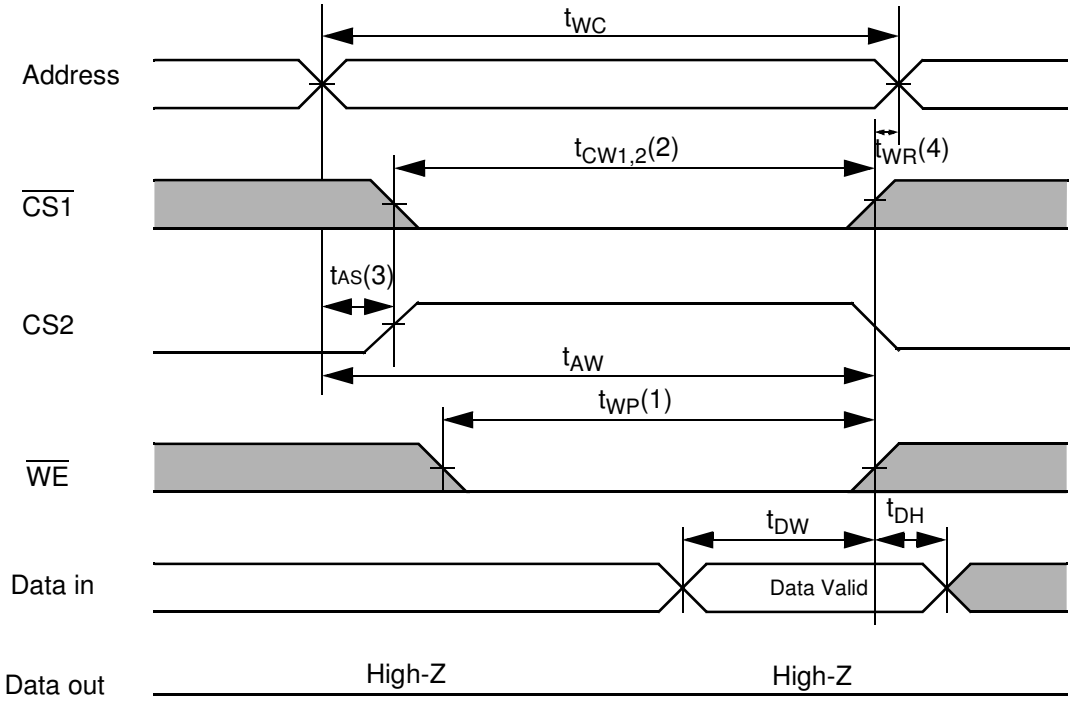
TIMING WAVEFORM OF WRITE CYCLE(1) ($\overline{WE}$ CONTROLLED)



TIMING WAVEFORM OF WRITE CYCLE(2) ($\overline{CS1}$ CONTROLLED)



TIMING WAVEFORM OF WRITE CYCLE(3) (CS2 CONTROLLED)



NOTES (WRITE CYCLE)

1. A write occurs during the overlap(t_{WP}) of low $\overline{CS1}$, a high CS2 and low $\overline{WE}$. A write begins at the latest transition among $\overline{CS1}$ goes low, CS2 goes high and $\overline{WE}$ goes low. A write ends at the earliest transition among $\overline{CS1}$ goes high, CS2 goes low and $\overline{WE}$ goes high. The t_{WP} is measured from the beginning of write to the end of write.
2. t_{CW} is measured from the $\overline{CS1}$ going low or CS2 going high to end of write.
3. t_{AS} is measured from the address valid to the beginning of write.
4. t_{WR} is measured from the end or write to the address change. t_{WR} applied in case a write ends as $\overline{CS1}$ or $\overline{WE}$ going high or CS2 going low.

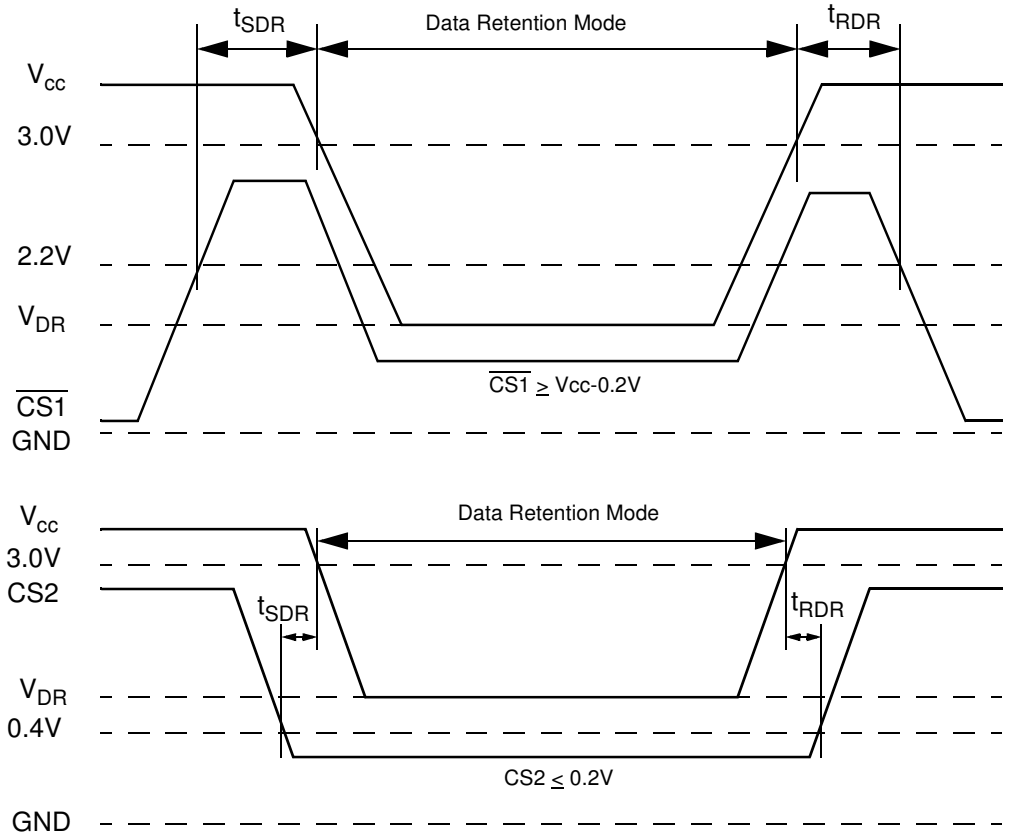
DATA RETENTION CHARACTERISTICS

Parameter	Symbol	Test Condition	Min	Typ[2)]	Max	Unit
V_{CC} for Data Retention	V_{DR}	I_{SB1} Test Condition (Chip Disabled) [1)]	1.5	-	3.3	V
Data Retention Current	I_{DR}	V_{CC}=1.5V, I_{SB1} Test Condition (Chip Disabled) [1)]	-	0.5	5.0	µA
Chip Deselect to Data Retention Time	t_{SDR}	See data retention wave form	0	-	-	ns
Operation Recovery Time	t_{RDR}		t_{RC}	-	-	

NOTES

1. See the I_{SB1} measurement condition of data sheet page 4.
2. Typical value is measured at T_A=25°C and not 100% tested.

DATA RETENTION WAVE FORM



SRAM PART CODING SYSTEM

EM X XX X X X XX X X - XX XX

1. EMLSI Memory
2. Product Type
3. Density
4. Function
5. Technology
6. Operating Voltage
7. Organization
8. Generation
9. Package
10. Speed
11. Power

1. Memory Component
EM ---------- Memory

2. Product Type
6 ---------- SRAM

3. Density
1 ---------- 1M
2 ---------- 2M
4 ---------- 4M
8 ---------- 8M

4. Function
0 ---------- Dual CS
1 ---------- Single CS
2 ---------- Multiplexed
3 ---------- Single CS / LBB, UBB(tBA=tOE)
4 ---------- Single CS / LBB, UBB(tBA=tCO)
5 ---------- Dual CS / LBB, UBB(tBA=tOE)
6 ---------- Dual CS / LBB, UBB(tBA=tCO)

5. Technology
F ---------- Full CMOS

6. Operating Voltage
T ---------- 5.0V
V ---------- 3.3V
U ---------- 3.0V
S ---------- 2.5V
R ---------- 2.0V
P ---------- 1.8V

7. Organization
8 ---------- x8 bit
16 ---------- x16 bit

8. Generation
Blank ---------- 1st generation
A ---------- 2nd generation
B ---------- 3rd generation
C ---------- 4th generation
D ---------- 5th generation
E ---------- 6th generation
F ---------- 7th generation
G ---------- 8th generation

9. Package
Blank ---------- KGD, 48&36FpBGA
S ---------- 32 sTSOP1
T ---------- 32 TSOP1
U ---------- 44 TSOP2
V ---------- 32 TSOP

10. Speed
45 ---------- 45ns
55 ---------- 55ns
70 ---------- 70ns
85 ---------- 85ns
10 ---------- 100ns
12 ---------- 120ns

11. Power
LL ---------- Low Low Power
LF ---------- Low Low Power(Pb-Free & Green)
L ---------- Low Power
S ---------- Standard Power