MC14513B

BCD-To-Seven Segment Latch/Decoder/Driver

CMOS MSI
(Low−Power Complementary MOS)

The MC14513B BCD−to−seven segment latch/decoder/driver is constructed with complementary MOS (CMOS) enhancement mode devices and NPN bipolar output drivers in a single monolithic structure. The circuit provides the functions of a 4−bit storage latch, an 8421 BCD−to−seven segment decoder, and has output drive capability. Lamp test ($\overline{LT}$), blanking ($\overline{BI}$), and latch enable (LE) inputs are used to test the display, to turn−off or pulse modulate the brightness of the display, and to store a BCD code, respectively. The Ripple Blanking Input (RBI) and Ripple Blanking Output (RBO) can be used to suppress either leading or trailing zeroes. It can be used with seven−segment light emitting diodes (LED), incandescent, fluorescent, gas discharge, or liquid crystal readouts either directly or indirectly.

Applications include instrument (e.g., counter, DVM, etc.) display driver, computer/calculator display driver, cockpit display driver, and various clock, watch, and timer uses.

Features

- Low Logic Circuit Power Dissipation
- High−Current Sourcing Outputs (Up to 25 mA)
- Latch Storage of Binary Input
- Blanking Input
- Lamp Test Provision
- Readout Blanking on all Illegal Input Combinations
- Lamp Intensity Modulation Capability
- Time Share (Multiplexing) Capability
- Adds Ripple Blanking In, Ripple Blanking Out to MC14511B
- Supply Voltage Range = 3.0 V to 18 V
- Capable of Driving Two Low−Power TTL Loads, One Low−Power Schottky TTL Load to Two HTL Loads Over the Rated Temperature Range
- Pb−Free Package is Available*

MAXIMUM RATINGS (Voltages Referenced to V_{SS})

Parameter	Symbol	Value	Unit
DC Supply Voltage Range	V_{DD}	−0.5 to +18.0	V
Input Voltage Range, All Inputs	V_{in}	−0.5 to V_{DD} +0.5	V
DC Current Drain per Input Pin	I	10	mA
Power Dissipation per Package (Note 1)	P_D	500	mW
Operating Temperature Range	T_A	−55 to +125	°C
Storage Temperature Range	T_{stg}	−65 to +150	°C
Maximum Continuous Output Drive Current (Source) per Output	I_{OHmax}	25	mA
Maximum Continuous Output Power (Source) per Output (Note 2)	P_{OHmax}	50	mW

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. Temperature Derating: Plastic “P and D/DW” Packages: – 7.0 mW/°C From 65°C To 125°C
2. $P_{OHmax} = I_{OH} (V_{DD} - V_{OH})$

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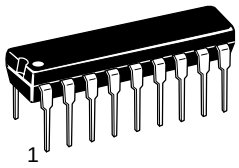
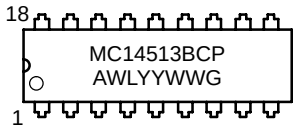


PDIP−18
P SUFFIX
CASE 707

MARKING DIAGRAM



A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week
G = Pb−Free Package

ORDERING INFORMATION

Device	Package	Shipping
MC14513BCP	PDIP−18	20 Units/Rail
MC14513BCPG	PDIP−18 (Pb−Free)	20 Units/Rail

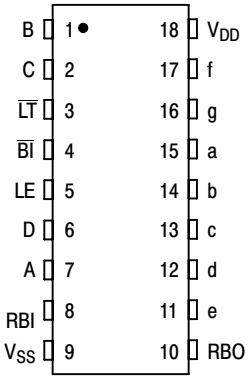
This device contains protection circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high−impedance circuit. A destructive high current mode may occur if V_{in} and V_{out} are not constrained to the range $V_{SS} \le (V_{in}$ or $V_{out}) \le V_{DD}$.

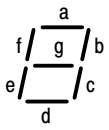
Due to the sourcing capability of this circuit, damage can occur to the device if V_{DD} is applied, and the outputs are shorted to V_{SS} and are at a logical 1 (See Maximum Ratings).

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

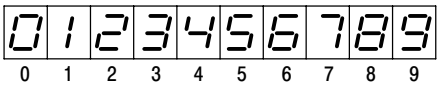
*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

PIN ASSIGNMENT





DISPLAY



TRUTH TABLE

Inputs								Outputs								
RBI	**LE**	**$\overline{BI}$**	**$\overline{LT}$**	**D**	**C**	**B**	**A**	**RBO**	**a**	**b**	**c**	**d**	**e**	**f**	**g**	**Display**
X	X	X	0	X	X	X	X	+	1	1	1	1	1	1	1	8
X	X	0	1	X	X	X	X	+	0	0	0	0	0	0	0	Blank
1	0	1	1	0	0	0	0	1	0	0	0	0	0	0	0	Blank
0	0	1	1	0	0	0	0	0	1	1	1	1	1	1	0	0
X	0	1	1	0	0	0	1	0	0	1	1	0	0	0	0	1
X	0	1	1	0	0	1	0	0	1	1	0	1	1	0	1	2
X	0	1	1	0	0	1	1	0	1	1	1	1	0	0	1	3
X	0	1	1	0	1	0	0	0	0	1	1	0	0	1	1	4
X	0	1	1	0	1	0	1	0	1	0	1	1	0	1	1	5
X	0	1	1	0	1	1	0	0	1	0	1	1	1	1	1	6
X	0	1	1	0	1	1	1	0	1	1	1	0	0	0	0	7
X	0	1	1	1	0	0	0	0	1	1	1	1	1	1	1	8
X	0	1	1	1	0	0	1	0	1	1	1	1	0	1	1	9
X	0	1	1	1	0	1	0	0	0	0	0	0	0	0	0	Blank
X	0	1	1	1	0	1	1	0	0	0	0	0	0	0	0	Blank
X	0	1	1	1	1	0	0	0	0	0	0	0	0	0	0	Blank
X	0	1	1	1	1	0	1	0	0	0	0	0	0	0	0	Blank
X	0	1	1	1	1	1	0	0	0	0	0	0	0	0	0	Blank
X	0	1	1	1	1	1	1	0	0	0	0	0	0	0	0	Blank
X	1	1	1	X	X	X	X	†				*				*

X = Don't Care

†RBO = RBI ($\overline{D}$ $\overline{C}$ $\overline{B}$ $\overline{A}$), indicated by other rows of table

*Depends upon the BCD code previously applied when LE = 0

ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

Characteristic	Symbol	V_{DD} Vdc	− 55°C Min	− 55°C Max	25°C Min	25°C Typ (Note 3)	25°C Max	125°C Min	125°C Max	Unit
Output Voltage — Segment Outputs “0” Level V_{in} = V_{DD} or 0	V_{OL}	5.0	−	0.05	−	0	0.05	−	0.05	Vdc
		10	−	0.05	−	0	0.05	−	0.05	
		15	−	0.05	−	0	0.05	−	0.05	
“1” Level V_{in} = 0 or V_{DD}	V_{OH}	5.0	4.1	−	4.1	5.0	−	4.1	−	Vdc
		10	9.1	−	9.1	10	−	9.1	−	
		15	14.1	−	14.1	15	−	14.1	−	
Output Voltage — RBO Output “0” Level V_{in} = V_{DD} or 0	V_{OL}	5.0	−	0.05	−	0	0.05	−	0.05	Vdc
		10	−	0.05	−	0	0.05	−	0.05	
		15	−	0.05	−	0	0.05	−	0.05	
“1” Level V_{in} = 0 or V_{DD}	V_{OH}	5.0	4.95	−	4.95	5.0	−	4.95	−	Vdc
		10	9.95	−	9.95	10	−	9.95	−	
		15	14.95	−	14.95	15	−	14.95	−	
Input Voltage (Note 3) “0” Level (V_O = 3.8 or 0.5 Vdc) (V_O = 8.8 or 1.0 Vdc) (V_O = 13.8 or 1.5 Vdc)	V_{IL}	5.0	−	1.5	−	2.25	1.5	−	1.5	Vdc
		10	−	3.0	−	4.50	3.0	−	3.0	
		15	−	4.0	−	6.75	4.0	−	4.0	
(V_O = 0.5 or 3.8 Vdc) “1” Level (V_O = 1.0 or 8.8 Vdc) (V_O = 1.5 or 13.8 Vdc)	V_{IH}	5.0	3.5	−	3.5	2.75	−	3.5	−	Vdc
		10	7.0	−	7.0	5.50	−	7.0	−	
		15	11	−	11	8.25	−	11	−	
Output Drive Voltage — Segments (I_{OH} = 0 mA) Source	V_{OH}	5.0	4.1	−	4.1	4.57	−	4.1	−	Vdc
(I_{OH} = 5.0 mA)			−	−	−	4.24	−	−	−	
(I_{OH} = 10 mA)			3.9	−	3.9	4.12	−	3.5	−	
(I_{OH} = 15 mA)			−	−	−	3.94	−	−	−	
(I_{OH} = 20 mA)			3.4	−	3.4	3.70	−	3.0	−	
(I_{OH} = 25 mA)			−	−	−	3.54	−	−	−	
(I_{OH} = 0 mA)		10	9.1	−	9.1	9.58	−	9.1	−	Vdc
(I_{OH} = 5.0 mA)			−	−	−	9.26	−	−	−	
(I_{OH} = 10 mA)			9.0	−	9.0	9.17	−	8.6	−	
(I_{OH} = 15 mA)			−	−	−	9.04	−	−	−	
(I_{OH} = 20 mA)			8.6	−	8.6	8.90	−	8.2	−	
(I_{OH} = 25 mA)			−	−	−	8.75	−	−	−	
(I_{OH} = 0 mA)		15	14.1	−	14.1	14.59	−	14.1	−	Vdc
(I_{OH} = 5.0 mA)			−	−	−	14.27	−	−	−	
(I_{OH} = 10 mA)			14	−	14	14.18	−	13.6	−	
(I_{OH} = 15 mA)			−	−	−	14.07	−	−	−	
(I_{OH} = 20 mA)			13.6	−	13.6	13.95	−	13.2	−	
(I_{OH} = 25 mA)			−	−	−	13.80	−	−	−	

3. Noise immunity specified for worst−case input combination.
Noise Margin for both “1” and “0” level = 1.0 Vdc min @ V_{DD} = 5.0 Vdc
2.0 Vdc min @ V_{DD} = 10 Vdc
2.5 Vdc min @ V_{DD} = 15 Vdc

ELECTRICAL CHARACTERISTICS (continued) (Voltages Referenced to V_{SS})

Characteristic	Symbol	V_{DD} Vdc	– 55°C Min	– 55°C Max	25°C Min	25°C Typ (Note 4)	25°C Max	125°C Min	125°C Max	Unit
Output Drive Current — RBO Output (V_{OH} = 2.5 V) Source (V_{OH} = 9.5 V) (V_{OH} = 13.5 V)	I_{OH}	5.0 10 15	– 0.40 – 0.21 – 0.81	– – –	– 0.32 – 0.17 – 0.66	– 0.64 – 0.34 – 1.30	– – –	– 0.22 – 0.12 – 0.46	– – –	mAdc
(V_{OL} = 0.4 V) Sink (V_{OL} = 0.5 V) (V_{OL} = 1.5 V)	I_{OL}	5.0 10 15	0.18 0.47 1.80	– – –	0.15 0.38 1.50	0.29 0.75 2.90	– – –	0.10 0.26 1.0	– – –	mAdc
Output Drive Current — Segments (V_{OL} = 0.4 V) Sink (V_{OL} = 0.5 V) (V_{OL} = 1.5 V)	I_{OL}	5.0 10 15	0.64 1.6 4.2	– – –	0.51 1.3 3.4	0.88 2.25 8.8	– – –	0.36 0.9 2.4	– – –	mAdc
Input Current	I_{in}	15	–	± 0.1	–	±0.00001	± 0.1	–	± 1.0	μAdc
Input Capacitance	C_{in}	–	–	–	–	5.0	7.5	–	–	pF
Quiescent Current (Per Package) V_{in} = 0 or V_{DD}, I_{out} = 0 μA	I_{DD}	5.0 10 15	– – –	5.0 10 20	– – –	0.005 0.010 0.015	5.0 10 20	– – –	150 300 600	μAdc
Total Supply Current (Note 5, 6) (Dynamic plus Quiescent, Per Package) (C_L = 50 pF on all outputs, all buffers switching)	I_T	5.0 10 15	I_T = (1.9 μA/kHz) f + I_{DD} I_T = (3.8 μA/kHz) f + I_{DD} I_T = (5.7 μA/kHz) f + I_{DD}							μAdc

4. Noise immunity specified for worst−case input combination.
   Noise Margin for both “1” and “0” level = 1.0 Vdc min @ V_{DD} = 5.0 Vdc
   2.0 Vdc min @ V_{DD} = 10 Vdc
   2.5 Vdc min @ V_{DD} = 15 Vdc
5. The formulas given are for the typical characteristics only at 25°C.
6. To calculate total supply current at loads other than 50 pF: $I_T(C_L) = I_T(50\ pF) + 3.5 \times 10^{-3} (C_L - 50) V_{DD} f$ where: I_T is in μA (per package), C_L in pF, V_{DD} in Vdc, and f in kHz is input frequency.

Input LE and RBI low, and Inputs D, $\overline{BI}$ and $\overline{LT}$ high.
f in respect to a system clock.
All outputs connected to respective C_L loads.

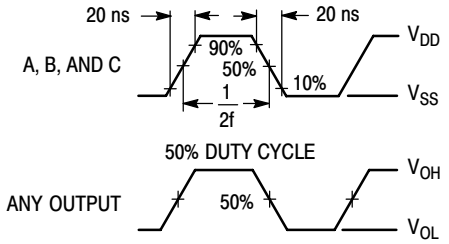
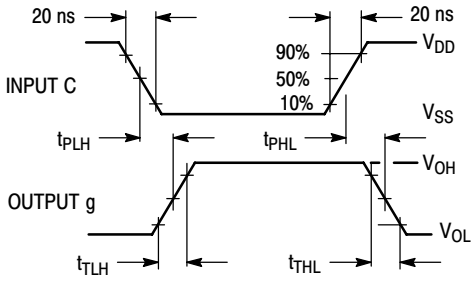


Figure 1. Dynamic Power Dissipation Signal Waveforms

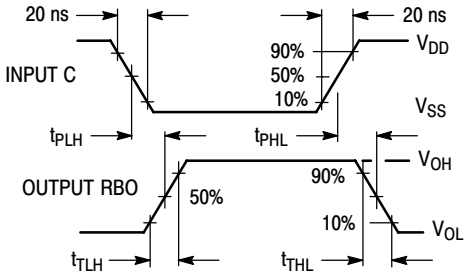
SWITCHING CHARACTERISTICS (Note 7) (C_L = 50 pF, T_A = 25°C)

Characteristic	Symbol	V_{DD} Vdc	All Types			Unit
			Min	Typ	Max	
Output Rise Time — Segment Outputs	t_{TLH}	5.0 10 15	− − −	40 30 25	80 60 50	ns
Output Rise Time — RBO Output	t_{TLH}	5.0 10 15	− − −	480 240 190	960 480 380	ns
Output Fall Time — Segment Outputs (Note 7) t_{THL} = (1.5 ns/pF) C_L + 50 ns t_{THL} = (0.75 ns/pF) C_L + 37.5 ns t_{THL} = (0.55 ns/pF) C_L + 37.5 ns	t_{THL}	5.0 10 15	− − −	125 75 65	250 150 130	ns
Output Fall Time — RBO Outputs t_{THL} = (3.25 ns/pF) C_L + 107.5 ns t_{THL} = (1.35 ns/pF) C_L + 67.5 ns t_{THL} = (0.95 ns/pF) C_L + 62.5 ns	t_{THL}	5.0 10 15	− − −	270 135 110	540 270 220	ns
Propagation Delay Time — A, B, C, D Inputs (Note 7) t_{PLH} = (0.40 ns/pF) C_L + 620 ns t_{PLH} = (0.25 ns/pF) C_L + 237.5 ns t_{PLH} = (0.20 ns/pF) C_L + 165 ns	t_{PLH}	5.0 10 15	− − −	640 250 175	1280 500 350	ns
t_{PHL} = (1.3 ns/pF) C_L + 655 ns t_{PHL} = (0.60 ns/pF) C_L + 260 ns t_{PHL} = (0.35 ns/pF) C_L + 182.5 ns	t_{PHL}	5.0 10 15	− − −	720 290 200	1440 580 400	ns
Propagation Delay Time — RBI and $\overline{BI}$ Inputs (Note 7) t_{PLH} = (1.05 ns/pF) C_L + 547.5 ns t_{PLH} = (0.45 ns/pF) C_L + 177.5 ns t_{PLH} = (0.30 ns/pF) C_L + 135 ns	t_{PLH}	5.0 10 15	− − −	600 200 150	750 300 220	ns
t_{PHL} = (0.85 ns/pF) C_L + 442.5 ns t_{PHL} = (0.45 ns/pF) C_L + 177.5 ns t_{PHL} = (0.35 ns/pF) C_L + 142.5 ns	t_{PHL}	5.0 10 15	− − −	485 200 160	970 400 320	ns
Propagation Delay Time — $\overline{LT}$ Input (Note 7) t_{PLH} = (0.45 ns/pF) C_L + 290.5 ns t_{PLH} = (0.25 ns/pF) C_L + 112.5 ns t_{PLH} = (0.20 ns/pF) C_L + 80 ns	t_{PLH}	5.0 10 15	− − −	313 125 90	625 250 180	ns
t_{PHL} = (1.3 ns/pF) C_L + 248 ns t_{PHL} = (0.45 ns/pF) C_L + 102.5 ns t_{PHL} = (0.35 ns/pF) C_L + 72.5 ns	t_{PHL}	5.0 10 15	− − −	313 125 90	625 250 180	ns
Setup Time	t_{su}	5.0 10 15	100 40 30	− − −	− − −	ns
Hold Time	t_h	5.0 10 15	60 40 30	− − −	− − −	ns
Latch Enable Pulse Width	$t_{WL(LE)}$	5.0 10 15	520 220 130	260 110 65	− − −	ns

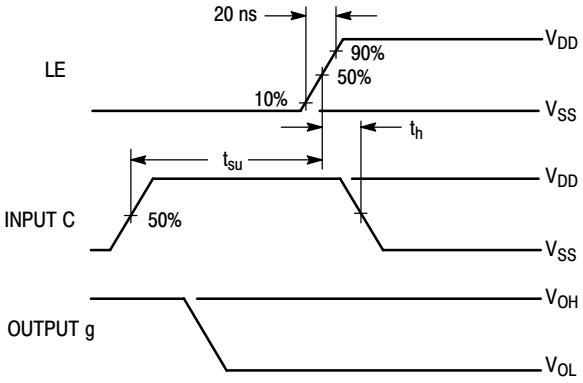
7. The formulas given are for the typical characteristics only.



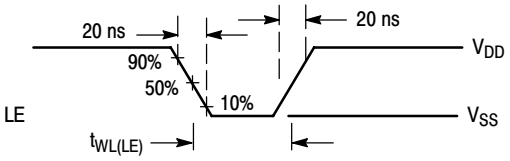
a. Data Propagation Delay: Inputs RBI, D and LE low, and Inputs A, B, $\overline{BI}$ and $\overline{LT}$ high.



b. Inputs A, B, D and LE low, and Inputs RBI, $\overline{BI}$ and $\overline{LT}$ high.



c. Setup and Hold Times: Input RBI and D low, Inputs A, B, $\overline{BI}$ and $\overline{LT}$ high.

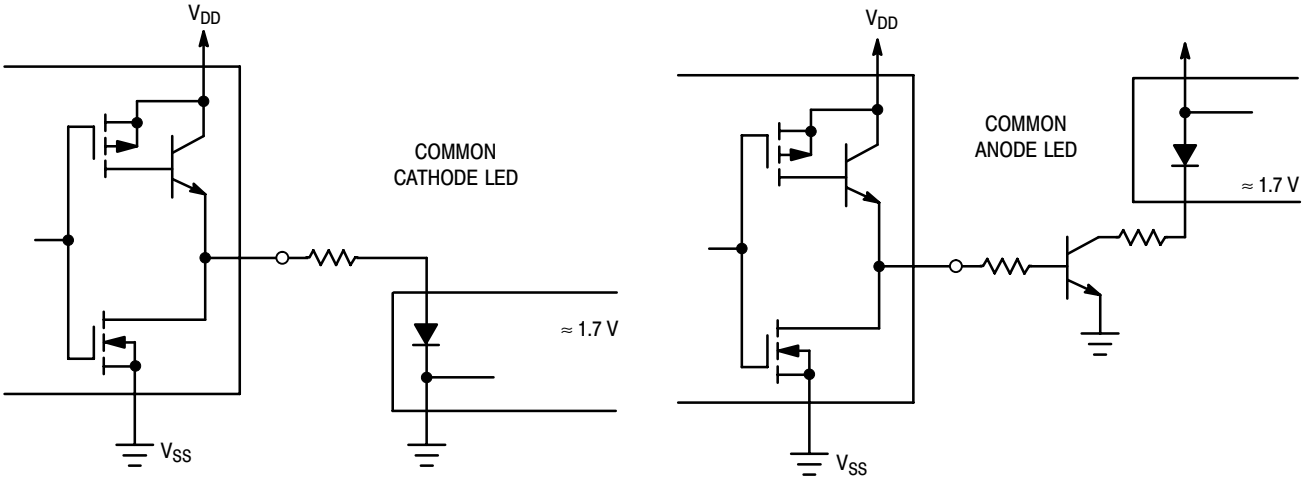


d. Pulse Width: Data DCBA strobed into latches.

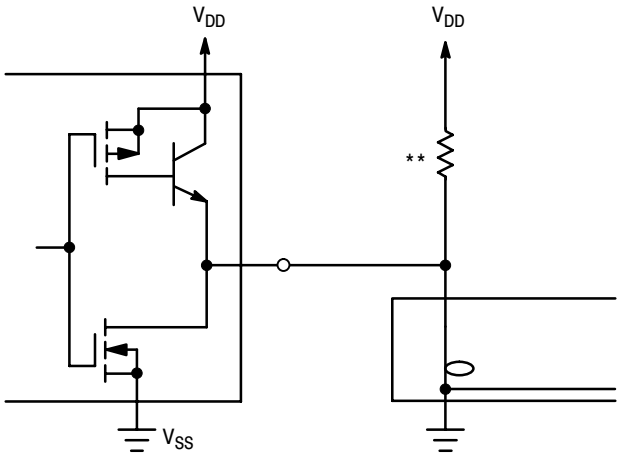
Figure 2. Dynamic Signal Waveforms

CONNECTIONS TO VARIOUS DISPLAY READOUTS

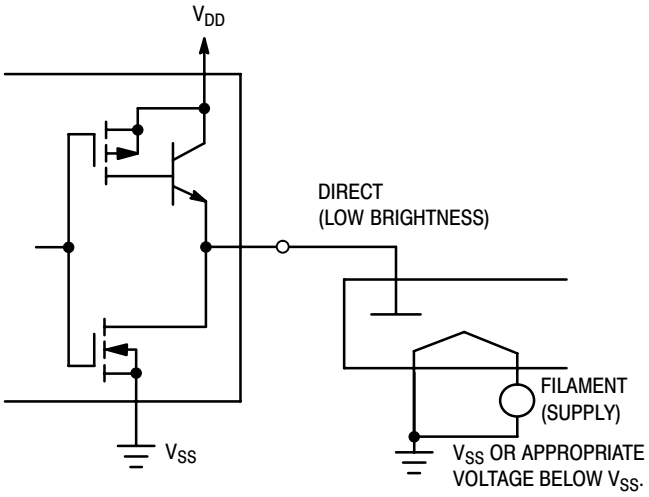
LIGHT EMITTING DIODE (LED) READOUT



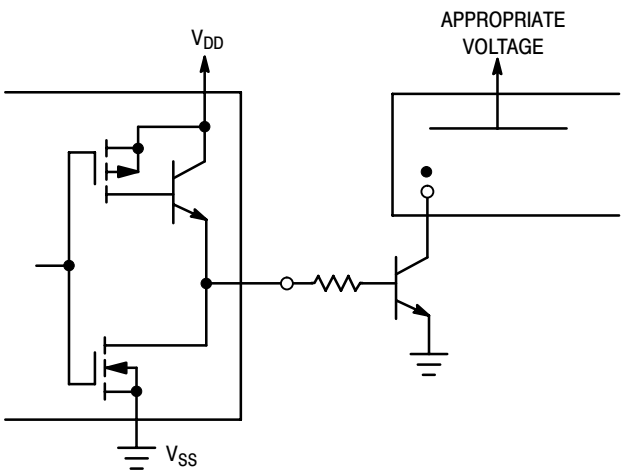
INCANDESCENT READOUT



FLUORESCENT READOUT

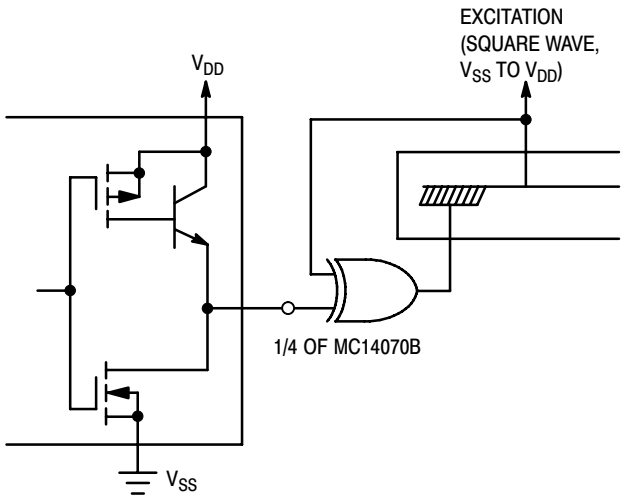


GAS DISCHARGE READOUT



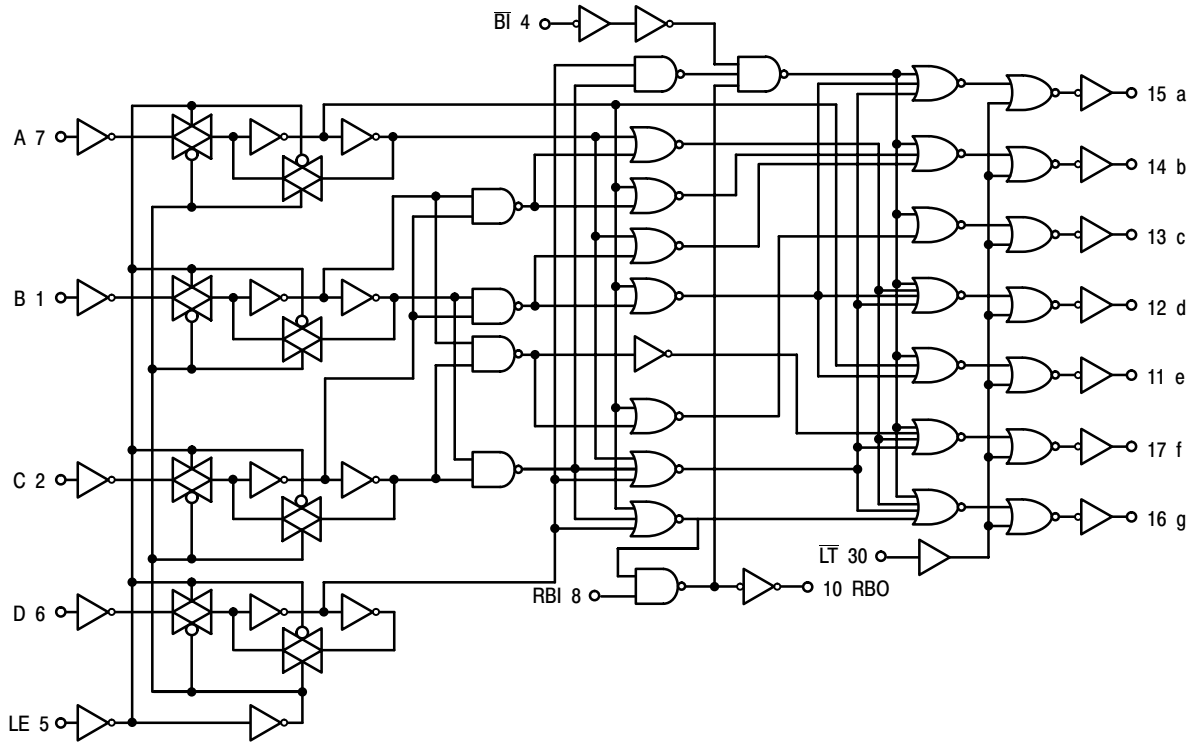
** A filament pre−warm resistor is recommended to reduce filament thermal shock and increase the effective cold resistance of the filament.

LIQUID CRYSTAL (LC) READOUT



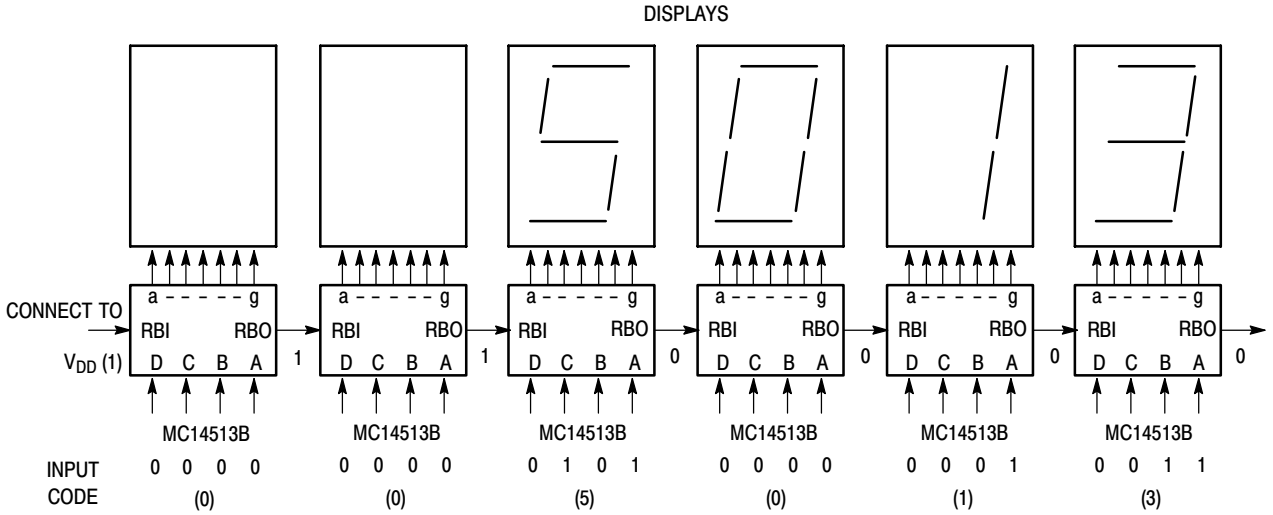
Direct dc drive of LC's not recommended for life of LC readouts.

LOGIC DIAGRAM

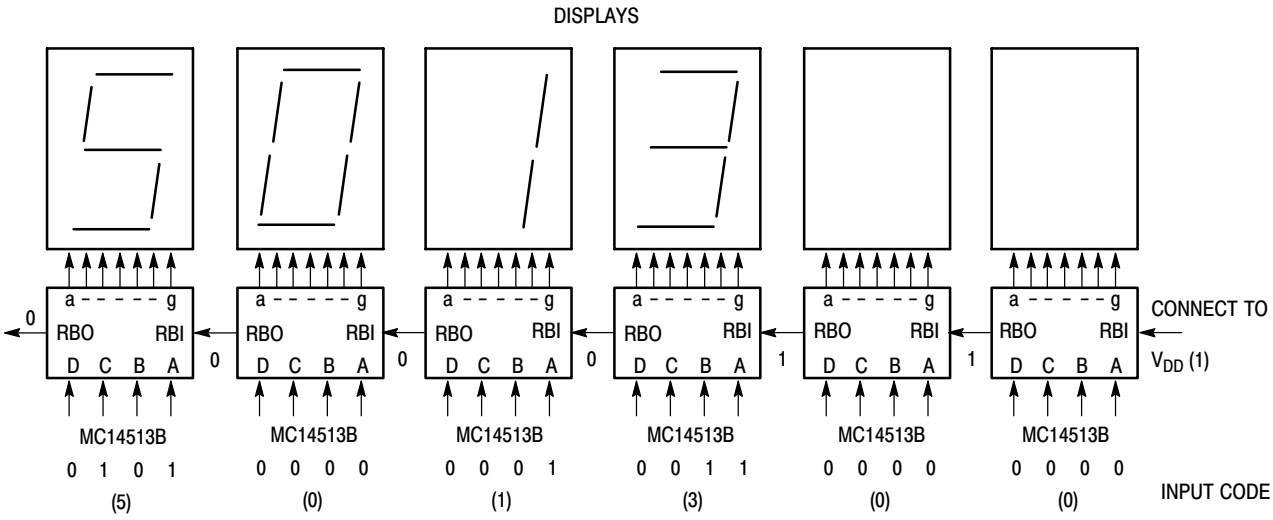


TYPICAL APPLICATIONS FOR RIPPLE BLANKING

LEADING EDGE ZERO SUPPRESSION

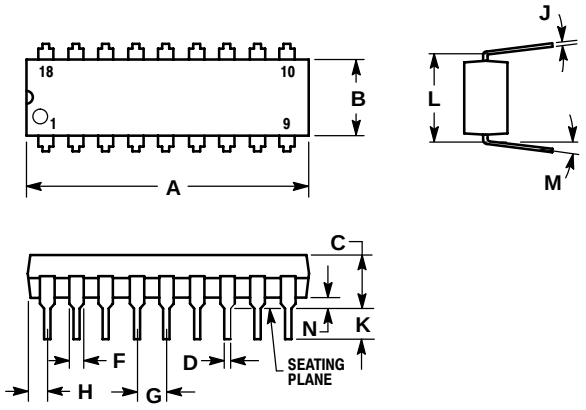


TRAILING EDGE ZERO SUPPRESSION



PACKAGE DIMENSIONS

PDIP−18
CASE 707−02
ISSUE D



NOTES:
1. POSITIONAL TOLERANCE OF LEADS (D), SHALL BE WITHIN 0.25 mm (0.010) AT MAXIMUM MATERIAL CONDITION, IN RELATION TO SEATING PLANE AND EACH OTHER.
2. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSION B DOES NOT INCLUDE MOLD FLASH.
4. CONTROLLING DIMENSION: INCH.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.875	0.915	22.22	23.24
B	0.240	0.260	6.10	6.60
C	0.140	0.180	3.56	4.57
D	0.014	0.022	0.36	0.56
F	0.050	0.070	1.27	1.78
G	0.100 BSC		2.54 BSC	
H	0.040	0.060	1.02	1.52
J	0.008	0.012	0.20	0.30
K	0.115	0.135	2.92	3.43
L	0.300 BSC		7.62 BSC	
M	0 °	15°	0 °	15 °
N	0.020	0.040	0.51	1.02

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