

# MC10EL34, MC100EL34

## 5V ECL $\div 2$ , $\div 4$ , $\div 8$ Clock Generation Chip

### Description

The MC10/100EL34 is a low skew  $\div 2$ ,  $\div 4$ ,  $\div 8$  clock generation chip designed explicitly for low skew clock generation applications. The internal dividers are synchronous to each other, therefore, the common output edges are all precisely aligned. The  $V_{BB}$  pin, an internally generated voltage supply, is available to this device only. For single-ended input conditions, the unused differential input is connected to  $V_{BB}$  as a switching reference voltage.  $V_{BB}$  may also rebias AC coupled inputs. When used, decouple  $V_{BB}$  and  $V_{CC}$  via a 0.01  $\mu\text{F}$  capacitor and limit current sourcing or sinking to 0.5 mA. When not used,  $V_{BB}$  should be left open.

The common enable ( $\overline{\text{EN}}$ ) is synchronous so that the internal dividers will only be enabled/disabled when the internal clock is already in the LOW state. This avoids any chance of generating a runt clock pulse on the internal clock when the device is enabled/disabled as can happen with an asynchronous control. An internal runt pulse could lead to losing synchronization between the internal divider stages. The internal enable flip-flop is clocked on the falling edge of the input clock, therefore, all associated specification limits are referenced to the negative edge of the clock input.

Upon startup, the internal flip-flops will attain a random state; the master reset (MR) input allows for the synchronization of the internal dividers, as well as multiple EL34s in a system.

The 100 Series contains temperature compensation.

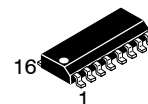
### Features

- 50 ps Output-to-Output Skew
- Synchronous Enable/Disable
- Master Reset for Synchronization
- PECL Mode Operating Range:  
 $V_{CC} = 4.2 \text{ V to } 5.7 \text{ V with } V_{EE} = 0 \text{ V}$
- NECL Mode Operating Range:  
 $V_{CC} = 0 \text{ V with } V_{EE} = -4.2 \text{ V to } -5.7 \text{ V}$
- Internal Input 75 k $\Omega$  Pulldown Resistors on CLK(s),  $\overline{\text{EN}}$ , and MR
- Pb-Free Packages are Available\*



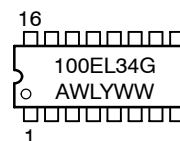
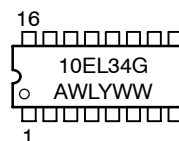
**ON Semiconductor®**

<http://onsemi.com>



**SO-16  
D SUFFIX  
CASE 751B**

### MARKING DIAGRAMS\*



A = Assembly Location  
WL = Wafer Lot  
YY = Year  
WW = Work Week  
G = Pb-Free Package

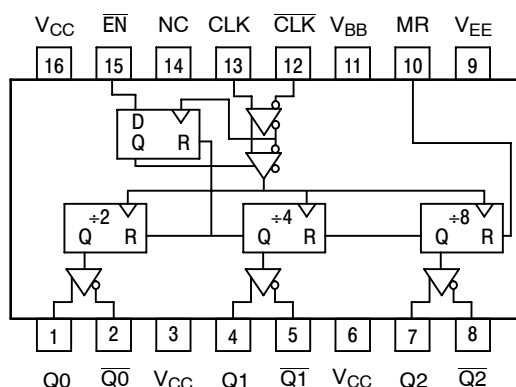
\*For additional marking information, refer to Application Note AND8002/D.

### ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 7 of this data sheet.

\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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\*All  $V_{CC}$  pins are tied together on the die.

Warning: All  $V_{CC}$  and  $V_{EE}$  pins must be externally connected to Power Supply to guarantee proper operation.

### Figure 1. Logic Diagram and Pinout Assignment

### Table 1. FUNCTION TABLE

| CLK* | EN* | MR* | Function               |
|------|-----|-----|------------------------|
| Z    | L   | L   | Divide                 |
| ZZ   | H   | L   | Hold Q <sub>0-3</sub>  |
| X    | X   | H   | Reset Q <sub>0-3</sub> |

\*Pins will default low when left open.

Z = Low-to-High Transition

ZZ = High-to-Low Transition

### Table 2. PIN DESCRIPTION

| Pin                          | Function                 |
|------------------------------|--------------------------|
| CLK, $\overline{\text{CLK}}$ | ECL Diff Clock Inputs    |
| EN                           | ECL Sync Enable          |
| MR                           | ECL Master Reset         |
| Q0, $\overline{\text{Q0}}$   | ECL Diff +2 Outputs      |
| Q1, $\overline{\text{Q1}}$   | ECL Diff +4 Outputs      |
| Q2, $\overline{\text{Q2}}$   | ECL Diff +8 Outputs      |
| V <sub>BB</sub>              | Reference Voltage Output |
| V <sub>CC</sub>              | Positive Supply          |
| V <sub>EE</sub>              | Negative Supply          |
| NC                           | No Connect               |

### Table 3. ATTRIBUTES

| Characteristics                                        | Value                                                    |
|--------------------------------------------------------|----------------------------------------------------------|
| Internal Input Pulldown Resistor                       | 75 KΩ                                                    |
| Internal Input Pullup Resistor                         | N/A                                                      |
| ESD Protection                                         | Human Body Model<br>Machine Model<br>Charge Device Model |
|                                                        | > 1 KV<br>> 100 V<br>> 2 KV                              |
| Moisture Sensitivity (Note 1)                          | Level 1                                                  |
| Flammability Rating                                    | Oxygen Index: 28 to 34                                   |
|                                                        | UL 94 V-0 @ 0.125 in                                     |
| Transistor Count                                       | 191 Devices                                              |
| Meets or Exceeds JEDEC Spec EIA/JESD78 IC Latchup Test |                                                          |

1. For additional Moisture Sensitivity information, refer to Application Note AND8003/D.

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**Table 4. MAXIMUM RATINGS**

| Symbol        | Parameter                                          | Condition 1                                    | Condition 2                            | Rating      | Unit         |
|---------------|----------------------------------------------------|------------------------------------------------|----------------------------------------|-------------|--------------|
| $V_{CC}$      | PECL Mode Power Supply                             | $V_{EE} = 0\text{ V}$                          |                                        | 8           | V            |
| $V_{EE}$      | NECL Mode Power Supply                             | $V_{CC} = 0\text{ V}$                          |                                        | -8          | V            |
| $V_I$         | PECL Mode Input Voltage<br>NECL Mode Input Voltage | $V_{EE} = 0\text{ V}$<br>$V_{CC} = 0\text{ V}$ | $V_I \leq V_{CC}$<br>$V_I \geq V_{EE}$ | 6<br>-6     | V<br>V       |
| $I_{out}$     | Output Current                                     | Continuous<br>Surge                            |                                        | 50<br>100   | mA<br>mA     |
| $I_{BB}$      | $V_{BB}$ Sink/Source                               |                                                |                                        | $\pm 0.5$   | mA           |
| $T_A$         | Operating Temperature Range                        |                                                |                                        | -40 to +85  | °C           |
| $T_{stg}$     | Storage Temperature Range                          |                                                |                                        | -65 to +150 | °C           |
| $\theta_{JA}$ | Thermal Resistance (Junction-to-Ambient)           | 0 lfpm<br>500 lfpm                             | SO-16<br>SO-16                         | 130<br>75   | °C/W<br>°C/W |
| $\theta_{JC}$ | Thermal Resistance (Junction-to-Case)              | Standard Board                                 | SO-16                                  | 33 to 36    | °C/W         |
| $T_{sol}$     | Wave Solder<br>Pb<br>Pb-Free                       | <2 to 3 sec @ 248°C<br><2 to 3 sec @ 260°C     |                                        | 265<br>265  | °C           |

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

**Table 5. 10EL SERIES PECL DC CHARACTERISTICS**  $V_{CC} = 5.0\text{ V}$ ;  $V_{EE} = 0\text{ V}$  (Note 2)

| Symbol      | Characteristic                                               | -40°C |      |      | 25°C |      |      | 85°C |      |      | Unit |
|-------------|--------------------------------------------------------------|-------|------|------|------|------|------|------|------|------|------|
|             |                                                              | Min   | Typ  | Max  | Min  | Typ  | Max  | Min  | Typ  | Max  |      |
| $I_{EE}$    | Power Supply Current                                         |       |      | 39   |      |      | 39   |      |      | 39   | mA   |
| $V_{OH}$    | Output HIGH Voltage (Note 3)                                 | 3920  | 4010 | 4110 | 4020 | 4105 | 4190 | 4090 | 4185 | 4280 | mV   |
| $V_{OL}$    | Output LOW Voltage (Note 3)                                  | 3050  | 3200 | 3350 | 3050 | 3210 | 3370 | 3050 | 3227 | 3405 | mV   |
| $V_{IH}$    | Input HIGH Voltage (Single-Ended)                            | 3770  |      | 4110 | 3870 |      | 4190 | 3940 |      | 4280 | mV   |
| $V_{IL}$    | Input LOW Voltage (Single-Ended)                             | 3050  |      | 3500 | 3050 |      | 3520 | 3050 |      | 3555 | mV   |
| $V_{BB}$    | Output Voltage Reference                                     | 3.57  |      | 3.7  | 3.65 |      | 3.75 | 3.69 |      | 3.81 | V    |
| $V_{IHCMR}$ | Input HIGH Voltage Common Mode Range (Differential) (Note 4) | 3.0   |      | 4.6  | 3.0  |      | 4.6  | 3.0  |      | 4.6  | V    |
| $I_{IH}$    | Input HIGH Current                                           |       |      | 150  |      |      | 150  |      |      | 150  | μA   |
| $I_{IL}$    | Input LOW Current                                            | 0.5   |      |      | 0.5  |      |      | 0.3  |      |      | μA   |

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

- Input and output parameters vary 1:1 with  $V_{CC}$ .  $V_{EE}$  can vary +0.06 V / -0.5 V.
- Outputs are terminated through a 50  $\Omega$  resistor to  $V_{CC} - 2.0\text{ V}$ .
- $V_{IHCMR}$  min varies 1:1 with  $V_{EE}$ .  $V_{IHCMR}$  max varies 1:1 with  $V_{CC}$ . The  $V_{IHCMR}$  range is referenced to the most positive side of the differential input signal. Normal operation is obtained if the HIGH level falls within the specified range and the peak-to-peak voltage lies between  $V_{ppmin}$  and 1 V.

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**Table 6. 10EL SERIES NECL DC CHARACTERISTICS**  $V_{CC} = 0\text{ V}$ ;  $V_{EE} = -5.0\text{ V}$  (Note 5)

| Symbol      | Characteristic                                               | -40°C |       |       | 25°C  |       |       | 85°C  |       |       | Unit          |
|-------------|--------------------------------------------------------------|-------|-------|-------|-------|-------|-------|-------|-------|-------|---------------|
|             |                                                              | Min   | Typ   | Max   | Min   | Typ   | Max   | Min   | Typ   | Max   |               |
| $I_{EE}$    | Power Supply Current                                         |       |       | 39    |       |       | 39    |       |       | 39    | mA            |
| $V_{OH}$    | Output HIGH Voltage (Note 6)                                 | -1080 | -990  | -890  | -980  | -895  | -810  | -910  | -815  | -720  | mV            |
| $V_{OL}$    | Output LOW Voltage (Note 6)                                  | -1950 | -1800 | -1650 | -1950 | -1790 | -1630 | -1950 | -1773 | -1595 | mV            |
| $V_{IH}$    | Input HIGH Voltage (Single-Ended)                            | -1230 |       | -890  | -1130 |       | -810  | -1060 |       | -720  | mV            |
| $V_{IL}$    | Input LOW Voltage (Single-Ended)                             | -1950 |       | -1500 | -1950 |       | -1480 | -1950 |       | -1445 | mV            |
| $V_{BB}$    | Output Voltage Reference                                     | -1.43 |       | -1.30 | -1.35 |       | -1.25 | -1.31 |       | -1.19 | V             |
| $V_{IHCMR}$ | Input HIGH Voltage Common Mode Range (Differential) (Note 7) | -2.0  |       | -0.4  | -2.0  |       | -0.4  | -2.0  |       | -0.4  | V             |
| $I_{IH}$    | Input HIGH Current                                           |       |       | 150   |       |       | 150   |       |       | 150   | $\mu\text{A}$ |
| $I_{IL}$    | Input LOW Current                                            | 0.5   |       |       | 0.5   |       |       | 0.3   |       |       | $\mu\text{A}$ |

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

5. Input and output parameters vary 1:1 with  $V_{CC}$ .  $V_{EE}$  can vary +0.06 V / -0.5 V.

6. Outputs are terminated through a 50  $\Omega$  resistor to  $V_{CC} - 2.0\text{ V}$ .

7.  $V_{IHCMR}$  min varies 1:1 with  $V_{EE}$ ,  $V_{IHCMR}$  max varies 1:1 with  $V_{CC}$ . The  $V_{IHCMR}$  range is referenced to the most positive side of the differential input signal. Normal operation is obtained if the HIGH level falls within the specified range and the peak-to-peak voltage lies between  $V_{ppmin}$  and 1 V.

**Table 7. 100EL SERIES PECL DC CHARACTERISTICS**  $V_{CC} = 5.0\text{ V}$ ;  $V_{EE} = 0\text{ V}$  (Note 8)

| Symbol      | Characteristic                                                              | -40°C |      |      | 25°C |      |      | 85°C |      |      | Unit          |
|-------------|-----------------------------------------------------------------------------|-------|------|------|------|------|------|------|------|------|---------------|
|             |                                                                             | Min   | Typ  | Max  | Min  | Typ  | Max  | Min  | Typ  | Max  |               |
| $I_{EE}$    | Power Supply Current                                                        |       |      | 39   |      |      | 39   |      |      | 42   | mA            |
| $V_{OH}$    | Output HIGH Voltage (Note 9)                                                | 3915  | 3995 | 4120 | 3975 | 4045 | 4120 | 3975 | 4050 | 4120 | mV            |
| $V_{OL}$    | Output LOW Voltage (Note 9)                                                 | 3170  | 3305 | 3445 | 3190 | 3295 | 3380 | 3190 | 3295 | 3380 | mV            |
| $V_{IH}$    | Input HIGH Voltage (Single-Ended)                                           | 3835  |      | 4120 | 3835 |      | 4120 | 3835 |      | 4120 | mV            |
| $V_{IL}$    | Input LOW Voltage (Single-Ended)                                            | 3190  |      | 3525 | 3190 |      | 3525 | 3190 |      | 3525 | mV            |
| $V_{BB}$    | Output Voltage Reference                                                    | 3.62  |      | 3.74 | 3.62 |      | 3.74 | 3.62 |      | 3.74 | V             |
| $V_{IHCMR}$ | Input HIGH Voltage Common Mode Range (Differential Configuration) (Note 10) | 2.2   |      | 4.6  | 2.2  |      | 4.6  | 2.2  |      | 4.6  | V             |
| $I_{IH}$    | Input HIGH Current                                                          |       |      | 150  |      |      | 150  |      |      | 150  | $\mu\text{A}$ |
| $I_{IL}$    | Input LOW Current                                                           | 0.5   |      |      | 0.5  |      |      | 0.5  |      |      | $\mu\text{A}$ |

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

8. Input and output parameters vary 1:1 with  $V_{CC}$ .  $V_{EE}$  can vary +0.8 V / -0.5 V.

9. Outputs are terminated through a 50  $\Omega$  resistor to  $V_{CC} - 2.0\text{ V}$ .

10.  $V_{IHCMR}$  min varies 1:1 with  $V_{EE}$ ,  $V_{IHCMR}$  max varies 1:1 with  $V_{CC}$ . The  $V_{IHCMR}$  range is referenced to the most positive side of the differential input signal. Normal operation is obtained if the HIGH level falls within the specified range and the peak-to-peak voltage lies between  $V_{ppmin}$  and 1 V.

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**Table 8. 100EL SERIES NECL DC CHARACTERISTICS**  $V_{CC} = 0\text{ V}$ ;  $V_{EE} = -5.0\text{ V}$  (Note 11)

| Symbol      | Characteristic                                                              | -40°C |       |       | 25°C  |       |       | 85°C  |       |       | Unit |
|-------------|-----------------------------------------------------------------------------|-------|-------|-------|-------|-------|-------|-------|-------|-------|------|
|             |                                                                             | Min   | Typ   | Max   | Min   | Typ   | Max   | Min   | Typ   | Max   |      |
| $I_{EE}$    | Power Supply Current                                                        |       |       | 39    |       |       | 39    |       |       | 42    | mA   |
| $V_{OH}$    | Output HIGH Voltage (Note 12)                                               | -1085 | -1005 | -880  | -1025 | -955  | -880  | -1025 | -955  | -880  | mV   |
| $V_{OL}$    | Output LOW Voltage (Note 12)                                                | -1830 | -1695 | -1555 | -1810 | -1705 | -1620 | -1810 | -1705 | -1620 | mV   |
| $V_{IH}$    | Input HIGH Voltage (Single-Ended)                                           | -1165 |       | -880  | -1165 |       | -880  | -1165 |       | -880  | mV   |
| $V_{IL}$    | Input LOW Voltage (Single-Ended)                                            | -1810 |       | -1475 | -1810 |       | -1475 | -1810 |       | -1475 | mV   |
| $V_{BB}$    | Output Voltage Reference                                                    | -1.38 |       | -1.26 | -1.38 |       | -1.26 | -1.38 |       | -1.26 | V    |
| $V_{IHCMR}$ | Input HIGH Voltage Common Mode Range (Differential Configuration) (Note 13) | -2.8  |       | -0.4  | -2.8  |       | -0.4  | -2.8  |       | -0.4  | V    |
| $I_{IH}$    | Input HIGH Current                                                          |       |       | 150   |       |       | 150   |       |       | 150   | μA   |
| $I_{IL}$    | Input LOW Current                                                           | 0.5   |       |       | 0.5   |       |       | 0.5   |       |       | μA   |

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

11. Input and output parameters vary 1:1 with  $V_{CC}$ .  $V_{EE}$  can vary +0.8 V / -0.5 V.

12. Outputs are terminated through a 50 Ω resistor to  $V_{CC} - 2.0\text{ V}$ .

13.  $V_{IHCMR}$  min varies 1:1 with  $V_{EE}$ .  $V_{IHCMR}$  max varies 1:1 with  $V_{CC}$ . The  $V_{IHCMR}$  range is referenced to the most positive side of the differential input signal. Normal operation is obtained if the HIGH level falls within the specified range and the peak-to-peak voltage lies between  $V_{ppmin}$  and 1 V.

**Table 9. AC CHARACTERISTICS**  $V_{CC} = 5.0\text{ V}$ ;  $V_{EE} = 0.0\text{ V}$  or  $V_{CC} = 0.0\text{ V}$ ;  $V_{EE} = -5.0\text{ V}$  (Note 14)

| Symbol                 | Characteristic                                              | -40°C             |     |                      | 25°C              |     |                      | 85°C              |     |                      | Unit |
|------------------------|-------------------------------------------------------------|-------------------|-----|----------------------|-------------------|-----|----------------------|-------------------|-----|----------------------|------|
|                        |                                                             | Min               | Typ | Max                  | Min               | Typ | Max                  | Min               | Typ | Max                  |      |
| $f_{max}$              | Maximum Toggle Frequency                                    | 1.1               |     |                      | 1.1               |     |                      | 1.1               |     |                      | GHz  |
| $t_{PLH}$<br>$t_{PHL}$ | Propagation Delay to<br>CLK to Q0<br>CLK to Q1,2<br>MR to Q | 960<br>900<br>750 |     | 1200<br>1140<br>1060 | 960<br>900<br>750 |     | 1200<br>1140<br>1060 | 970<br>910<br>790 |     | 1210<br>1150<br>1090 | ps   |
| $t_{SKEW}$             | Within-Device Skew (Note 15)                                |                   | 100 |                      |                   | 100 |                      |                   | 100 |                      | ps   |
| $t_{JITTER}$           | Cycle-to-Cycle Jitter                                       |                   | 1.0 |                      |                   | 1.0 |                      |                   | 1.0 |                      | ps   |
| $t_S$                  | Setup Time $\overline{EN}$                                  | 400               |     |                      | 400               |     |                      | 400               |     |                      | ps   |
| $t_H$                  | Hold Time $\overline{EN}$                                   | 250               |     |                      | 250               |     |                      | 250               |     |                      | ps   |
| $t_{RR}$               | Set/Reset Recovery                                          | 400               | 200 |                      | 400               | 200 |                      | 400               | 200 |                      | ps   |
| $V_{PP}$               | Input Swing (Note 16)                                       | 150               |     | 1000                 | 150               |     | 1000                 | 150               |     | 1000                 | mV   |
| $t_r$<br>$t_f$         | Output Rise/Fall Times Q<br>(20% - 80%)                     | 225               |     | 475                  | 225               |     | 475                  | 225               |     | 475                  | ps   |

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

14. 10 Series:  $V_{EE}$  can vary +0.06 V / -0.5 V.

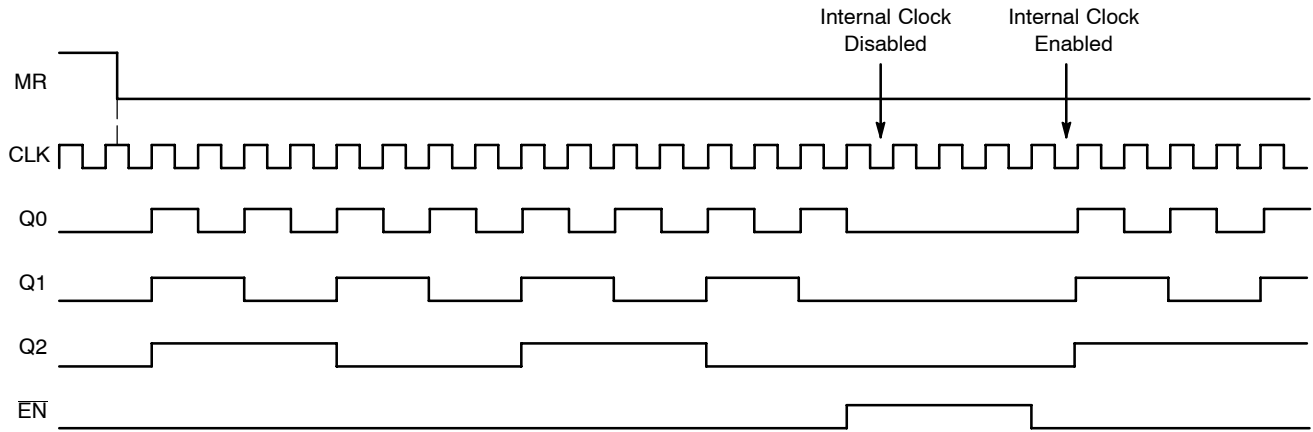
100 Series:  $V_{EE}$  can vary +0.8 V / -0.5 V.

15. Within-device skew is defined as identical transitions on similar paths through a device.

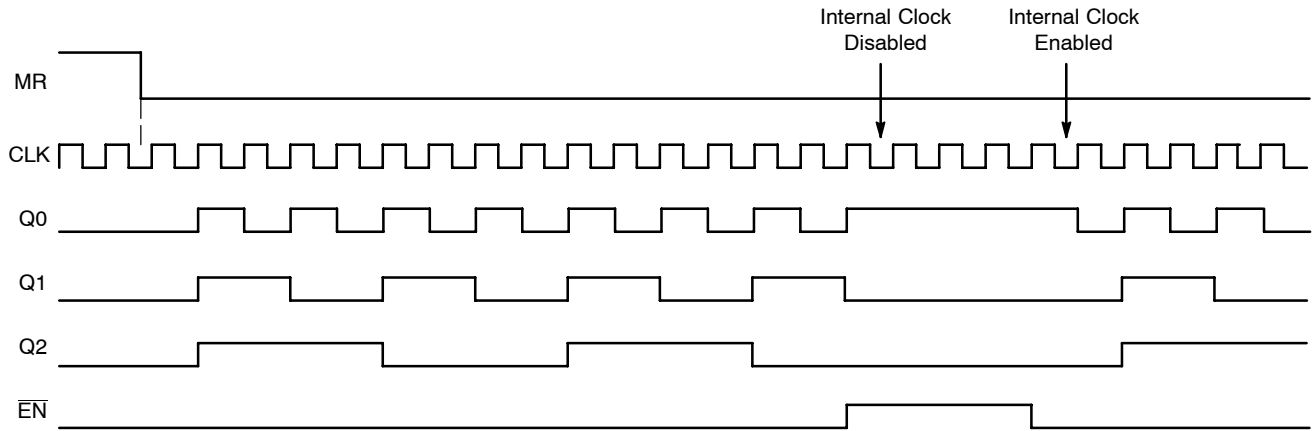
16.  $V_{ppmin}$  is minimum input swing for which AC parameters guaranteed. The device has a DC gain of  $\approx 40$ .

## MC10EL34, MC100EL34

There are two distinct functional relationships between the Master Reset and Clock:



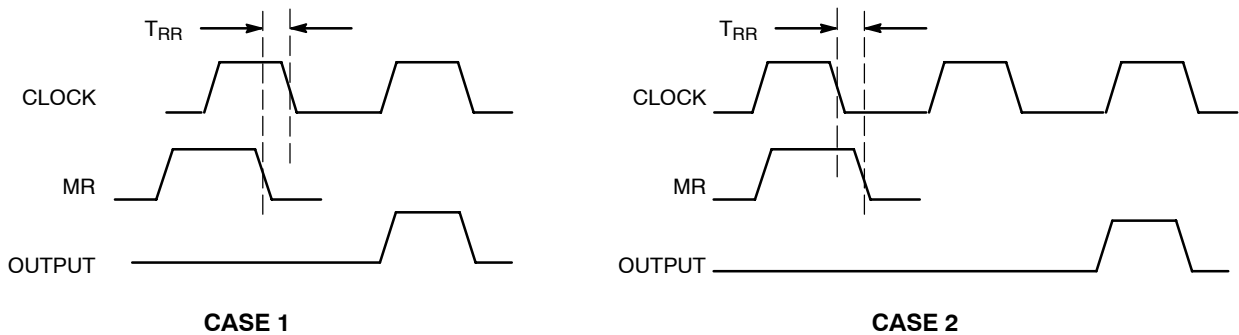
**CASE 1: If the MR is de-asserted (H-L), while the Clock is still high, the outputs will follow the first ensuing clock rising edge.**



**CASE 2: If the MR is de-asserted (H-L), after the Clock has transitioned low, the outputs will follow the second ensuing clock rising edge.**

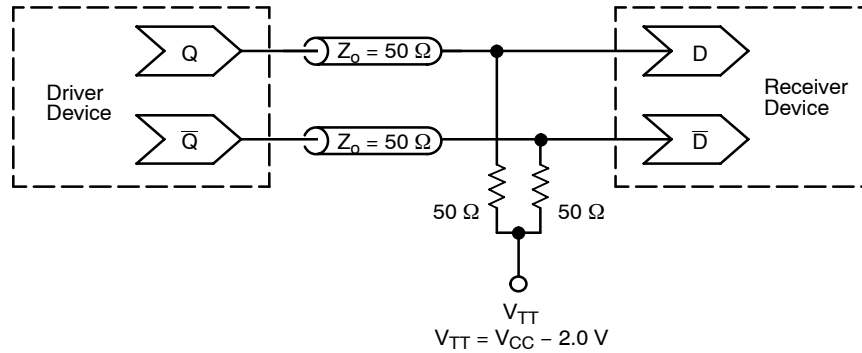
**Figure 2. Timing Diagrams**

The  $\overline{\text{EN}}$  signal will “freeze” the internal divider flip-flops on the first falling edge of CLK after its assertion. The internal divider flip-flops will maintain their state during the freeze. The  $\overline{\text{EN}}$  is deasserted (LOW), and after the next falling edge of CLK, then the internal divider flip-flops will “unfreeze” and continue to their next state count with proper phase relationships.



**Figure 3. Reset Recovery Time**

## MC10EL34, MC100EL34



**Figure 4. Typical Termination for Output Driver and Device Evaluation**  
 (See Application Note AND8020/D – Termination of ECL Logic Devices.)

### ORDERING INFORMATION

| Device        | Package            | Shipping <sup>†</sup> |
|---------------|--------------------|-----------------------|
| MC10EL34D     | SO-16              | 48 Units / Rail       |
| MC10EL34DG    | SO-16<br>(Pb-Free) | 48 Units / Rail       |
| MC10EL34DR2   | SO-16              | 2500 / Tape & Reel    |
| MC10EL34DR2G  | SO-16<br>(Pb-Free) | 2500 / Tape & Reel    |
| MC100EL34D    | SO-16              | 48 Units / Rail       |
| MC100EL34DG   | SO-16<br>(Pb-Free) | 48 Units / Rail       |
| MC100EL34DR2  | SO-16              | 2500 / Tape & Reel    |
| MC100EL34DR2G | SO-16<br>(Pb-Free) | 2500 / Tape & Reel    |

<sup>†</sup>For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

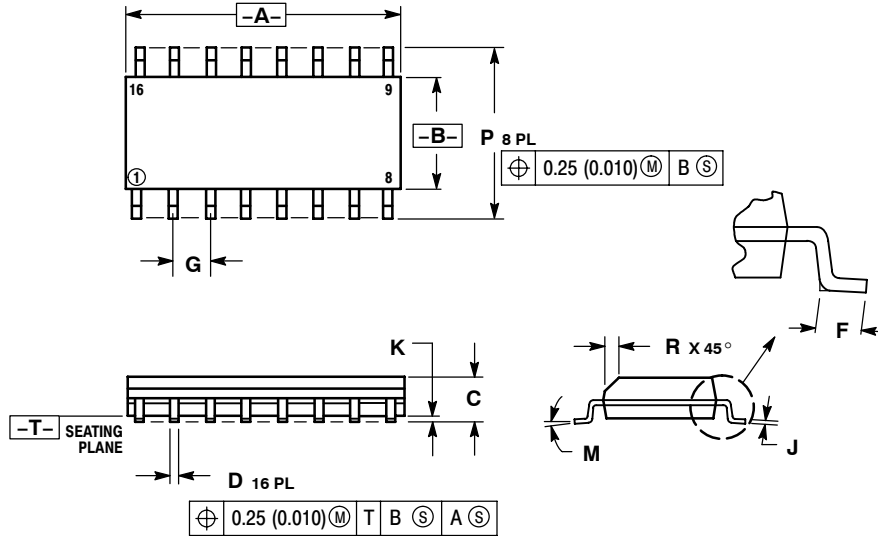
### Resource Reference of Application Notes

- AN1405/D** – ECL Clock Distribution Techniques
- AN1406/D** – Designing with PECL (ECL at +5.0 V)
- AN1503/D** – ECLinPS™ I/O SPICE Modeling Kit
- AN1504/D** – Metastability and the ECLinPS Family
- AN1568/D** – Interfacing Between LVDS and ECL
- AN1672/D** – The ECL Translator Guide
- AND8001/D** – Odd Number Counters Design
- AND8002/D** – Marking and Date Codes
- AND8020/D** – Termination of ECL Logic Devices
- AND8066/D** – Interfacing with ECLinPS
- AND8090/D** – AC Characteristics of ECL Devices

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## PACKAGE DIMENSIONS

SO-16  
D SUFFIX  
CASE 751B-05  
ISSUE J



### NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

| DIM | MILLIMETERS |       | INCHES    |       |
|-----|-------------|-------|-----------|-------|
|     | MIN         | MAX   | MIN       | MAX   |
| A   | 9.80        | 10.00 | 0.386     | 0.393 |
| B   | 3.80        | 4.00  | 0.150     | 0.157 |
| C   | 1.35        | 1.75  | 0.054     | 0.068 |
| D   | 0.35        | 0.49  | 0.014     | 0.019 |
| F   | 0.40        | 1.25  | 0.016     | 0.049 |
| G   | 1.27 BSC    |       | 0.050 BSC |       |
| J   | 0.19        | 0.25  | 0.008     | 0.009 |
| K   | 0.10        | 0.25  | 0.004     | 0.009 |
| M   | 0°          | 7°    | 0°        | 7°    |
| P   | 5.80        | 6.20  | 0.229     | 0.244 |
| R   | 0.25        | 0.50  | 0.010     | 0.019 |

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