

HD74LVC125A

Quad. Bus Buffer Gates with 3-state Outputs

REJ03D0348-0400Z
(Previous ADE-205-108C (Z))
Rev.4.00
Jul. 23, 2004

Description

The HD74LVC125A has four bus buffer gates in a 14 pin package. The device require the three state control input C to be taken high to put the output into the high impedance condition, whereas the device requires the control input to be low to put the output into high impedance. Low voltage and high-speed operation is suitable at the battery drive product (note type personal computer) and low power consumption extends the life of a battery for long time operation.

Features

- $V_{CC} = 2.0 \text{ V to } 5.5 \text{ V}$
- All inputs $V_{IH} (\text{Max.}) = 5.5 \text{ V} (@V_{CC} = 0 \text{ V to } 5.5 \text{ V})$
- All outputs $V_{OUT} (\text{Max.}) = 5.5 \text{ V} (@V_{CC} = 0 \text{ V or output off state})$
- Typical V_{OL} ground bounce $< 0.8 \text{ V} (@V_{CC} = 3.3 \text{ V, } T_a = 25^\circ\text{C})$
- Typical V_{OH} undershoot $> 2.0 \text{ V} (@V_{CC} = 3.3 \text{ V, } T_a = 25^\circ\text{C})$
- High output current $\pm 24 \text{ mA} (@V_{CC} = 3.0 \text{ V to } 5.5 \text{ V})$
- Ordering Information

Part Name	Package Type	Package Code	Package Abbreviation	Taping Abbreviation (Quantity)
HD74LVC125AFPEL	SOP-14 pin (JEITA)	FP-14DAV	FP	EL (2,000 pcs/reel)
HD74LVC125ATELL	TSSOP-14 pin	TTP-14DV	T	ELL (2,000 pcs/reel)

Note: Please consult the sales office for the above package availability.

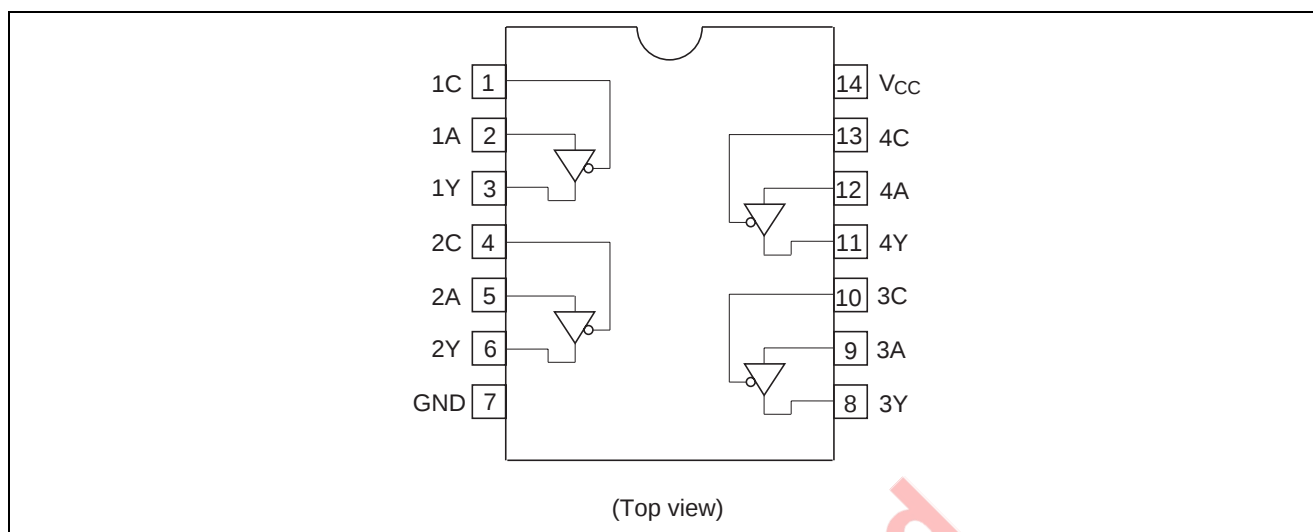
Function Table

Inputs

C	A	Outputs Y
H	X	Z
L	L	L
L	H	H

H: High level
L: Low level
X: Immaterial
Z: High impedance

Pin Arrangement



Absolute Maximum Ratings

Item	Symbol	Ratings	Unit	Conditions
Supply voltage	V_{CC}	-0.5 to 6.0	V	
Input diode current	I_{IK}	-50	mA	$V_I = -0.5$ V
Input voltage	V_I	-0.5 to 6.0	V	
Output diode current	I_{OK}	-50	mA	$V_O = -0.5$ V
		50		$V_O = V_{CC} + 0.5$ V
Output voltage	V_O	-0.5 to $V_{CC} + 0.5$	V	Output "H" or "L"
		-0.5 to 6.0		Output "Z" or V_{CC} :OFF
Output current	I_O	± 50	mA	
V_{CC} , GND current / pin	I_{CC} or I_{GND}	± 100	mA	
Storage temperature	Tstg	-65 to +150	°C	

Note: The absolute maximum ratings are values, which must not individually be exceeded, and furthermore, no two of which may be realized at the same time.

Recommended Operating Conditions

Item	Symbol	Ratings	Unit	Conditions
Supply voltage	V_{CC}	1.5 to 5.5	V	Data hold
		2.0 to 5.5		At operation
Input / output voltage	V_I	0 to 5.5	V	C, A
	V_O	0 to V_{CC}	V	Output "H" or "L"
		0 to 5.5		Output "Z" or V_{CC} :OFF
Operating temperature	T_a	-40 to 85	°C	
Output current	I_{OH}	-12	mA	$V_{CC} = 2.7$ V
		-24 ^{*2}		$V_{CC} = 3.0$ V to 5.5 V
	I_{OL}	12	mA	$V_{CC} = 2.7$ V
		24 ^{*2}		$V_{CC} = 3.0$ V to 5.5 V
Input rise / fall time ^{*1}	t_r, t_f	10	ns/V	

Notes: 1. This item guarantees maximum limit when one input switches.

Waveform: Refer to test circuit of switching characteristics.

2. Duty cycle $\leq 50\%$

Electrical Characteristics

Item	Symbol	V_{CC} (V)	$T_a = -40$ to 85°C		Unit	Test Conditions
			Min	Max		
Input voltage	V_{IH}	2.7 to 3.6	2.0	—	V	
		4.5 to 5.5	$V_{CC} \times 0.7$	—		
	V_{IL}	2.7 to 3.6	—	0.8	V	
		4.5 to 5.5	—	$V_{CC} \times 0.3$		
Output voltage	V_{OH}	2.7 to 5.5	$V_{CC} - 0.2$	—	V	$I_{OH} = -100 \mu\text{A}$
		2.7	2.2	—		$I_{OH} = -12 \text{ mA}$
		3.0	2.4	—		
		3.0	2.2	—		$I_{OH} = -24 \text{ mA}$
		4.5	3.8	—		
	V_{OL}	2.7 to 5.5	—	0.2	V	$I_{OL} = 100 \mu\text{A}$
		2.7	—	0.4		$I_{OL} = 12 \text{ mA}$
		3.0	—	0.55		$I_{OL} = 24 \text{ mA}$
		4.5	—	0.55		
Input current	I_{IN}	0 to 5.5	—	± 5.0	μA	$V_{IN} = 5.5 V_{CC} \text{ GND}$
Off state output current	I_{IOZ}	2.7 to 5.5	—	± 5.0	μA	$V_{IN} = V_{CC}, \text{ GND},$ $V_{OUT} = 5.5 \text{ V or GND}$
Output leak current	I_{OFF}	0	—	20	μA	$V_{IN} / V_{OUT} = 5.5 \text{ V}$
Quiescent supply current	I_{CC}	2.7 to 3.6	—	± 10	μA	$V_{IN} / V_{OUT} = 3.6$ to 5.5 V
		2.7 to 5.5	—	10		$V_{IN} = V_{CC} \text{ or GND}$
	ΔI_{CC}	3.0 to 3.6	—	500	μA	$V_{IN} = \text{one input at } (V_{CC} - 0.6) \text{ V},$ other inputs at $V_{CC} \text{ or GND}$

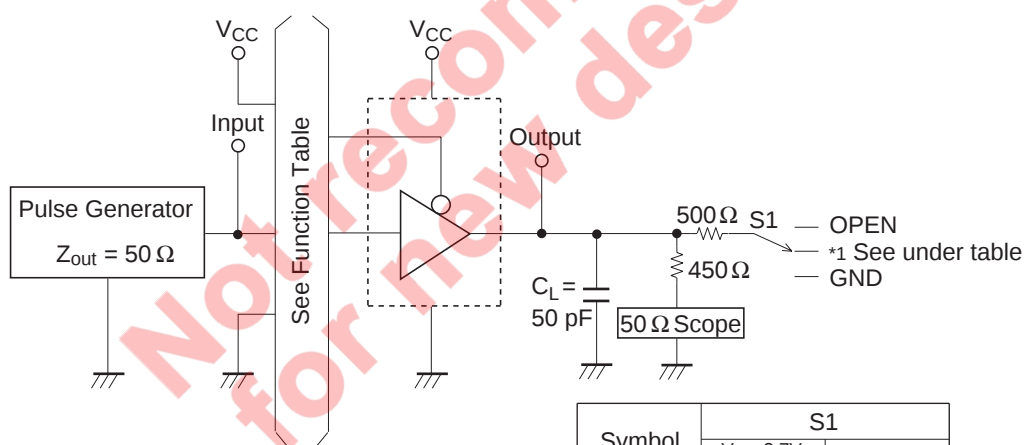
Switching Characteristics

Item	Symbol	V _{CC} (V)	Ta = -40 to 85°C			Unit	From (Input)	To (Output)
			Min	Typ	Max			
Propagation delay time	t _{PLH}	2.7	—	—	6.5	ns	A	Y
	t _{PHL}	3.3±0.3	1.5	—	6.0			
		5.0±0.5	—	—	5.0			
Output enable time	t _{ZH}	2.7	—	—	8.0	ns	C	Y
	t _{ZL}	3.3±0.3	1.5	—	7.0			
		5.0±0.5	—	—	6.0			
Output disable time	t _{HZ}	2.7	—	—	6.5	ns	C	Y
	t _{LZ}	3.3±0.3	1.5	—	5.5			
		5.0±0.5	—	—	4.5			
Between output pins skew ^{*1}	t _{OSLH}	2.7	—	—	—	ns		
	t _{OSHL}	3.3±0.3	—	—	1.0			
		5.0±0.5	—	—	1.0			
Input capacitance	C _{IN}	2.7	—	3.0	—	pF		
Output capacitance	C _O	2.7	—	15.0	—	pF		

Note: 1. This parameter is characterized but not tested.

$$t_{OSLH} = |t_{PLHm} - t_{PLHn}|, t_{OSHL} = |t_{PHLm} - t_{PHLn}|$$

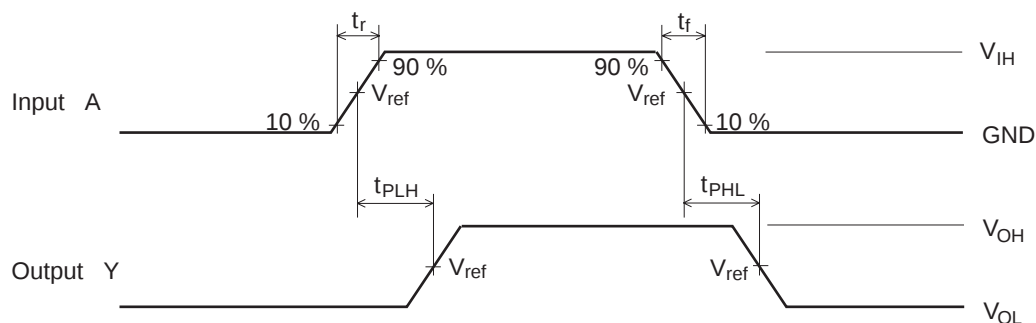
Test Circuit



Symbol	S1	
	V _{CC} =2.7V, 3.3±0.3V	V _{CC} =5.0±0.5V
t _{PLH} / t _{PHL}	OPEN	OPEN
t _{ZH} / t _{HZ}	GND	GND
t _{ZL} / t _{LZ}	6 V	2×V _{CC}

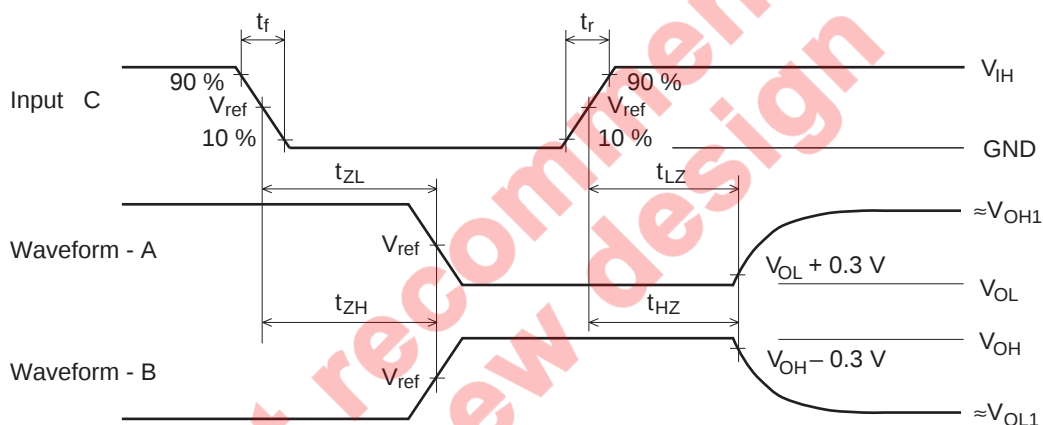
Note: 1. C_L includes probe and jig capacitance.

Waveforms – 1



- Notes:
1. $t_r = 2.5$ ns, $t_f = 2.5$ ns
 2. Input waveform : PRR = 10 MHz, duty cycle 50%

Waveforms – 2



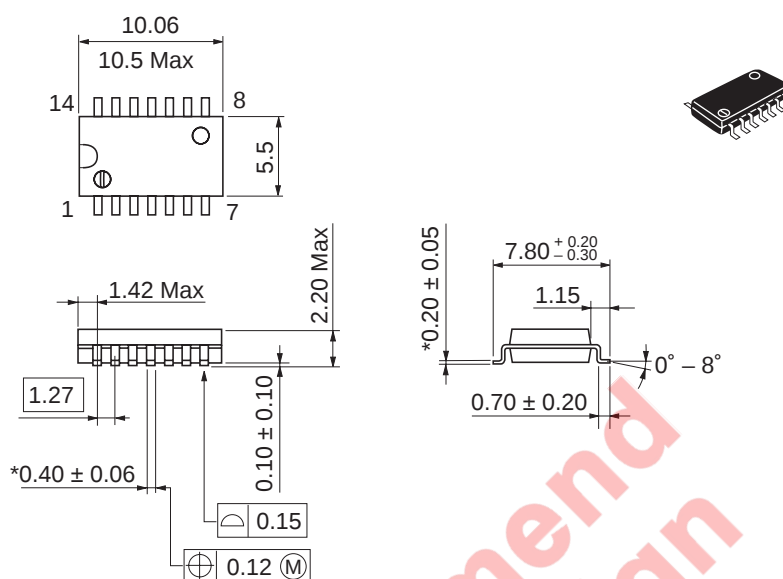
TEST	$V_{CC}=2.7V, 3.3\pm0.3V$	$V_{CC}=5.0\pm0.5V$
V_{IH}	2.7 V	V_{CC}
V_{ref}	1.5 V	50% V_{CC}
V_{OH1}	3 V	V_{CC}
V_{OL1}	GND	GND

- Notes:
1. $t_r = 2.5$ ns, $t_f = 2.5$ ns
 2. Input waveform : PRR = 10 MHz, duty cycle 50%
 3. Waveform – A shows input conditions such that the output is "L" level when enable by the output control.
 4. Waveform – B shows input conditions such that the output is "H" level when enable by the output control.

Package Dimensions

As of January, 2003

Unit: mm

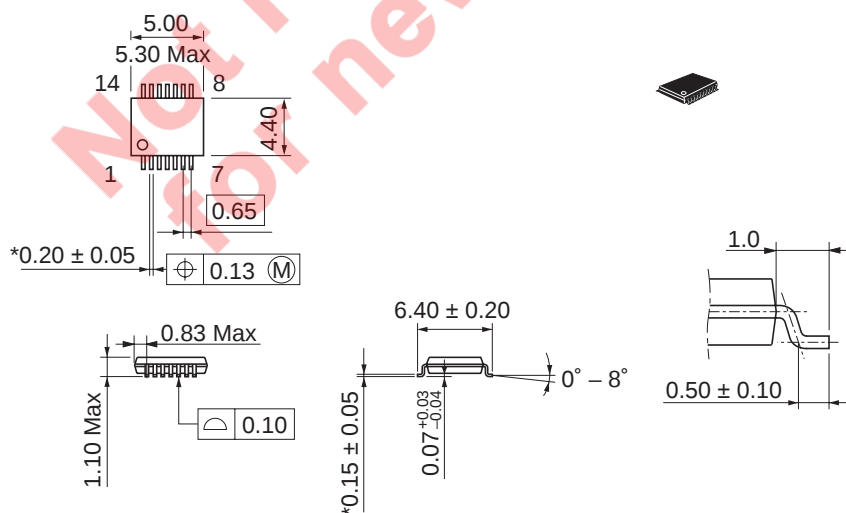


*Ni/Pd/Au plating

Package Code	FP-14DAV
JEDEC	—
JEITA	Conforms
Mass (reference value)	0.23 g

As of January, 2003

Unit: mm



*Ni/Pd/Au plating

Package Code	TTP-14DV
JEDEC	—
JEITA	—
Mass (reference value)	0.05 g

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