PRELIMINARY

Integrated Circuit Systems, Inc.

ICS843004-02

CRYSTAL-TO-3.3V LVPECL FREQUENCY SYNTHESIZER

GENERAL DESCRIPTION

The ICS843004-02 is a 4 output LVPECL Synthesizer optimized to generate clock frequencies for a variety of high performance applications and is a member of the HiPerClocks™ family of high performance clock solutions from ICS. This device can select its input reference clock from either a crystal input or a single-ended clock signal and can be configured to generate a number of different output frequencies via the 3 frequency select pins (F_SEL2:0). The ICS843004-02 uses ICS' 3rd generation low phase noise VCO technology and can achieve 1ps or lower typical rms phase jitter. This ensures that it will easily meet clocking requirements for high-speed communication protocols such as 10 and 12 Gigabit Ethernet, 10 Gigbit Fibre Channel, and SONET. This device is also suitable for next generation serial I/O technologies like serial ATA and SCSI and is conveniently packaged in a small 24-pin TSSOP package.

FUNCTION TABLE

Inputs			M Divider Value	N Divider Value
F_SEL2	F_SEL1	F_SEL0		
0	0	0	18	3
0	0	1	24	4
0	1	0	24	8
0	1	1	32	1
1	0	0	32	2
1	0	1	32	4
1	1	0	32	8
1	1	1	40	8

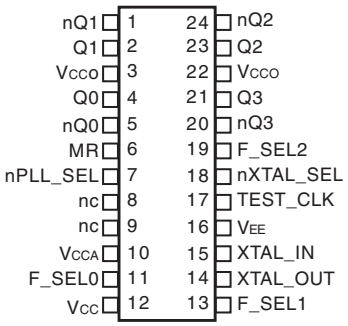
FEATURES

- Four 3.3V LVPECL outputs
- Selectable crystal oscillator interface or LVCMOS/LVTTL single-ended input
- Crystal input range: 14MHz - 37.78MHz
- VCO Range: 560MHz - 680MHz
- Supports the following applications: SONET, Ethernet, Serial ATA, SCSI and HDTV
- RMS phase jitter @ 155.52MHz (12kHz - 20MHz): 0.91ps (typical)

Offset	Noise Power
100Hz	-97.1 dBc/Hz
1kHz	-121.6 dBc/Hz
10kHz	-124.9 dBc/Hz
100kHz	-125.1 dBc/Hz

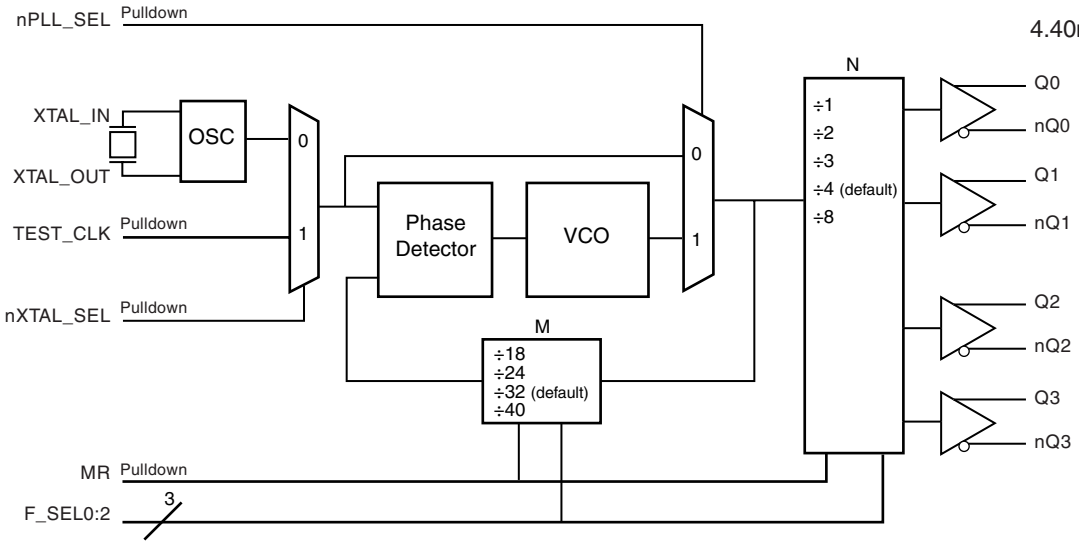
- Full 3.3V supply mode
- 0°C to 70°C ambient operating temperature

PIN ASSIGNMENT



ICS843004-02
24-Lead TSSOP
4.40mm x 7.8mm x 0.92mm
package body
G Package
Top View

BLOCK DIAGRAM



The Preliminary Information presented herein represents a product in prototyping or pre-production. The noted characteristics are based on initial product characterization. Integrated Circuit Systems, Incorporated (ICS) reserves the right to change any circuitry or specifications without notice.

TABLE 1. PIN DESCRIPTIONS

Number	Name	Type		Description
1, 2	nQ1, Q1	Output		Differential output pair. LVPECL interface levels.
3, 22	V_{CCO}	Power		Output supply pins.
4, 5	Q0, nQ0	Ouput		Differential output pair. LVPECL interface levels.
6	MR	Input	Pulldown	Active HIGH Master Reset. When logic HIGH, the internal dividers are reset causing the true outputs Qx to go low and the inverted outputs nQx to go high. When logic LOW, the internal dividers and the outputs are enabled. LVCMOS/LVTTL interface levels.
7	nPLL_SEL	Input	Pulldown	Selects between the PLL and TEST_CLK as input to the dividers. When LOW, selects PLL (PLL Enable). When HIGH, deselects the reference clock (PLL Bypass). LVCMOS/LVTTL interface levels.
8, 9	nc	Unused		No connect.
10	V_{CCA}	Power		Analog supply pin.
11, 19	F_SEL0, F_SEL2	Input	Pullup	Frequency select pins. LVCMOS/LVTTL interface levels.
12	V_{CC}	Power		Core supply pin.
13	F_SEL1	Input	Pulldown	Frequency select pins. LVCMOS/LVTTL interface levels.
14, 15	XTAL_OUT, XTAL_IN	Input		Parallel resonant crystal interface. XTAL_OUT is the output, XTAL_IN is the input.
16	V_{EE}	Power		Negative supply pin.
17	TEST_CLK	Input	Pulldown	LVCMOS/LVTTL clock input.
18	nXTAL_SEL	Input	Pulldown	Selects between crystal or TEST_CLK inputs as the the PLL Reference source. Selects XTAL inputs when LOW. Selects TEST_CLK when HIGH. LVCMOS/LVTTL interface levels.
20, 21	nQ3, Q3	Output		Differential output pair. LVPECL interface levels.
23, 24	Q2, nQ2	Output		Differential output pair. LVPECL interface levels.

NOTE: *Pulldown and Pullup* refers to internal input resistors. See Table 2, Pin Characteristics, for typical values.

TABLE 2. PIN CHARACTERISTICS

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C_{IN}	Input Capacitance			4		pF
$R_{PULLDOWN}$	Input Pulldown Resistor			51		kΩ
R_{PULLUP}	Input Pullup Resistor			51		kΩ

TABLE 3. OUTPUT CONFIGURATION AND FREQUENCY RANGE FUNCTION TABLE

Inputs				M Divider Value	N Divider Value	VCO (MHz)	Output Frequency (MHz)	Application
F_SEL2	F_SEL1	F_SEL0	Reference Clock					
0	1	0	24.75	24	8	594	74.25	HDTV
1	1	1	14.8351649	40	8	593.4066	74.1758245	HDTV
1	1	1	16	40	8	640	80	SCSI
1	0	1	19.44	32	4	622.08	155.52	SONET
1	1	0	19.44	32	8	622.08	77.76	SONET
0	1	1	19.44	32	1	622.08	622.08	SONET
1	0	0	19.44	32	2	622.08	311.04	SONET
0	0	1	25	24	4	600	150	SATA
0	1	0	25	24	8	600	75	SATA
0	0	1	26.5625	24	4	637.5	159.375	10 Gig Fibre Channel
1	0	1	19.53125	32	4	625	156.25	10 Gig Ethernet
0	0	0	31.25	18	3	562.5	187.5	12 Gig Ethernet

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{CC}	4.6V
Inputs, V_I	-0.5V to V_{CC} + 0.5V
Outputs, I_O	
Continuous Current	50mA
Surge Current	100mA
Package Thermal Impedance, θ_{JA}	70°C/W (0 lfpm)
Storage Temperature, T_{STG}	-65°C to 150°C

NOTE: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

TABLE 4A. POWER SUPPLY DC CHARACTERISTICS, $V_{CC} = V_{CCA} = V_{CCO}$ = 3.3V±5%, TA = 0°C TO 70°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{CC}	Core Supply Voltage		3.135	3.3	3.465	V
V_{CCA}	Analog Supply Voltage		3.135	3.3	3.465	V
V_{CCO}	Output Supply Voltage		3.135	3.3	3.465	V
I_{EE}	Power Supply Current			125		mA
I_{CCA}	Analog Supply Current			12		mA

TABLE 4B. LVCMOS / LVTTL DC CHARACTERISTICS, $V_{CC} = V_{CCA} = V_{CCO}$ = 3.3V±5%, TA = 0°C TO 70°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage			2		V_{CC} + 0.3	V
V_{IL}	Input Low Voltage	nPLL_SEL, nXTAL_SEL, F_SEL0:F_SEL2, MR		-0.3		0.8	V
		TEST_CLK		-0.3		1.3	V
I_{IH}	Input High Current	TEST_CLK, MR, F_SEL1 nPLL_SEL, nXTAL_SEL	$V_{CC} = V_{IN}$ = 3.465V			150	µA
		F_SEL0, F_SEL2	$V_{CC} = V_{IN}$ = 3.465V			5	µA
I_{IL}	Input Low Current	TEST_CLK, MR, F_SEL1 nPLL_SEL, nXTAL_SEL,	V_{CC} = 3.465V, V_{IN} = 0V	-150			µA
		F_SEL0, F_SEL2	V_{CC} = 3.465V, V_{IN} = 0V	-5			µA

TABLE 4C. LVPECL DC CHARACTERISTICS, $V_{CC} = V_{CCA} = V_{CCO}$ = 3.3V±5%, TA = 0°C TO 70°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{OH}	Output High Voltage; NOTE 1		V_{CCO} - 1.4		V_{CCO} - 0.9	V
V_{OL}	Output Low Voltage; NOTE 1		V_{CCO} - 2.0		V_{CCO} - 1.7	V
V_{SWING}	Peak-to-Peak Output Voltage Swing		0.6		1.0	V

NOTE 1: Outputs terminated with 50Ω to V_{CCO} - 2V.

TABLE 5. CRYSTAL CHARACTERISTICS

Parameter	Test Conditions	Minimum	Typical	Maximum	Units
Mode of Oscillation		Fundamental			MHz
Frequency		14		37.78	MHz
Equivalent Series Resistance (ESR)				50	Ω
Shunt Capacitance				7	pF

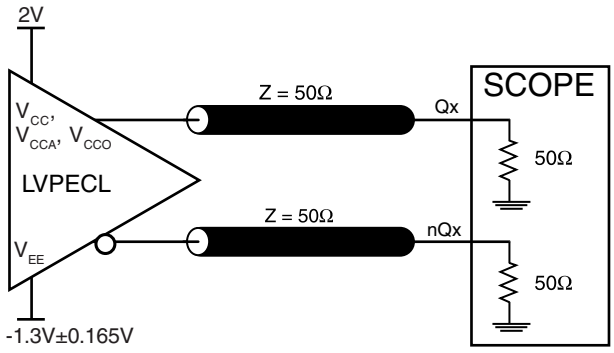
NOTE: Characterized using an 18pf parallel resonant crystal.

TABLE 6. AC CHARACTERISTICS, $V_{CC} = V_{CCA} = V_{CCO}$ = 3.3V±5%, TA = 0°C TO 70°C

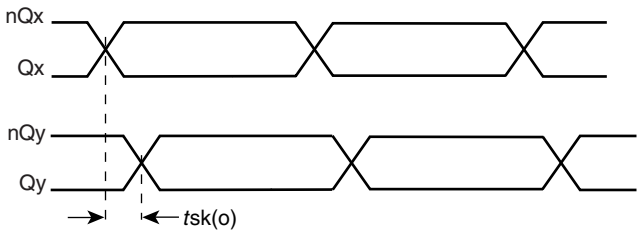
Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{OUT}	Output Frequency		74.17		637.5	MHz
f_{VCO}	PLL VCO Lock Range		562.5		640	MHz
		F_SEL0:F_SEL2 = 0	562.5		580	MHz
*t*sk(o)	Output Skew; NOTE 1			15		ps
*t*jit(Ø)	RMS Phase Jitter; NOTE 2, 3	155.52MHz, 12kHz -20MHz		0.91		ps
t_L	PLL Lock Time			TBD		ms
t_R / t_F	Output Rise/Fall Time	20% to 80%		450		ps
odc	Output Duty Cycle			50		%

NOTE 1: Defined as skew between outputs at the same supply voltages and with equal load conditions. Measured at the output differential cross points.
NOTE 2: Phase jitter is dependent on the input source used.
NOTE 3: This parameter is defined in accordance with JEDEC Standard 65.

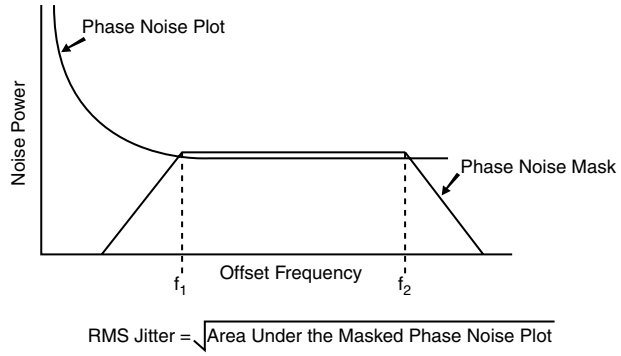
PARAMETER MEASUREMENT INFORMATION



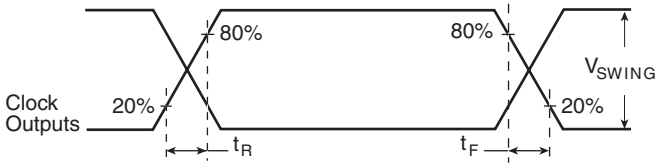
3.3V CORE/3.3V OUTPUT LOAD AC TEST CIRCUIT



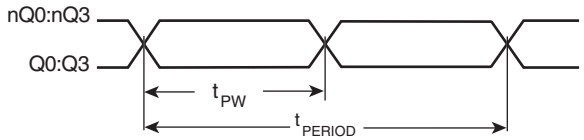
OUTPUT SKEW



RMS PHASE JITTER



OUTPUT RISE/FALL TIME



$$odc = \frac{t_{PW}}{t_{PERIOD}} \times 100\%$$

OUTPUT DUTY CYCLE/PULSE WIDTH/PERIOD

APPLICATION INFORMATION

POWER SUPPLY FILTERING TECHNIQUES

As in any high speed analog circuitry, the power supply pins are vulnerable to random noise. The ICS843004-02 provides separate power supplies to isolate any high switching noise from the outputs to the internal PLL. V_{CC}, V_{CCA}, and V_{CCO} should be individually connected to the power supply plane through vias, and bypass capacitors should be used for each pin. To achieve optimum jitter performance, power supply isolation is required. *Figure 1* illustrates how a 10Ω resistor along with a 10µF and a .01µF bypass capacitor should be connected to each V_{CCA}.

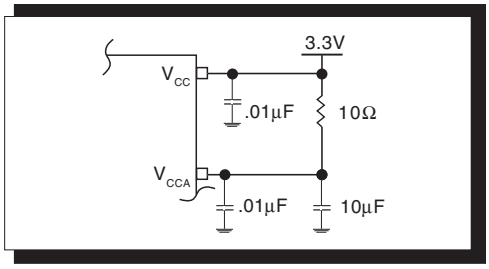


FIGURE 1. POWER SUPPLY FILTERING

RECOMMENDATIONS FOR UNUSED INPUT AND OUTPUT PINS

INPUTS:

CRYSTAL INPUT:
For applications not requiring the use of the crystal oscillator input, both XTAL_IN and XTAL_OUT can be left floating. Though not required, but for additional protection, a 1kΩ resistor can be tied from XTAL_IN to ground.

TEST CLK INPUT:
For applications not requiring the use of the test clock, it can be left floating. Though not required, but for additional protection, a 1kΩ resistor can be tied from the TEST_CLK to ground.

SELECT PINS:
All select pins have internal pull-ups and pull-downs; additional resistance is not required but can be added for additional protection. A 1kΩ resistor can be used.

OUTPUTS:

LVPECL OUTPUT
All unused LVPECL outputs can be left floating. We recommend that there is no trace attached. Both sides of the differential output pair should either be left floating or terminated.

CRYSTAL INPUT INTERFACE

The ICS843004-02 has been characterized with 18pF parallel resonant crystals. The capacitor values shown in *Figure 2* below were determined using a 26.5625MHz 18pF parallel resonant crystal and were chosen to minimize the ppm error.

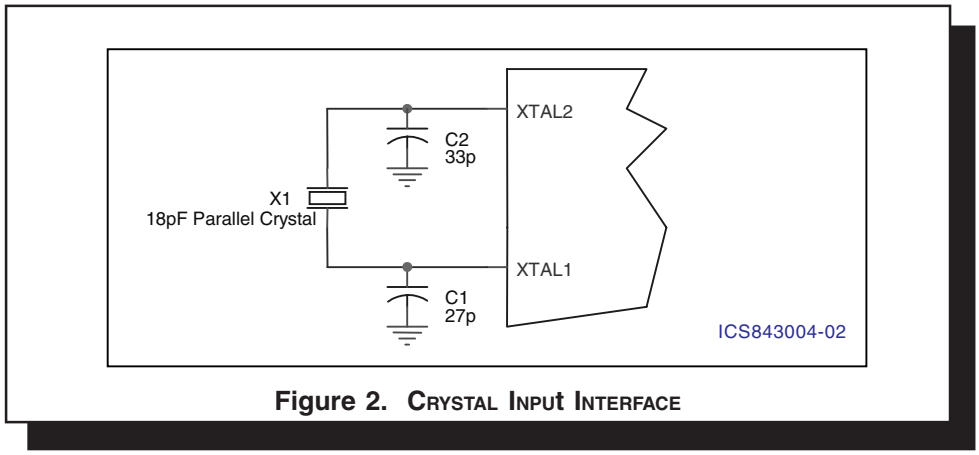


Figure 2. CRYSTAL INPUT INTERFACE

TERMINATION FOR 3.3V LVPECL OUTPUT

The clock layout topology shown below is a typical termination for LVPECL outputs. The two different layouts mentioned are recommended only as guidelines.

FOUT and nFOUT are low impedance follower outputs that generate ECL/LVPECL compatible outputs. Therefore, terminating resistors (DC current path to ground) or current sources must be used for functionality. These outputs are designed to drive 50Ω transmission lines. Matched impedance techniques should be used to maximize operating frequency and minimize signal distortion. *Figures 3A and 3B* show two different layouts which are recommended only as guidelines. Other suitable clock layouts may exist and it would be recommended that the board designers simulate to guarantee compatibility across all printed circuit and clock component process variations.

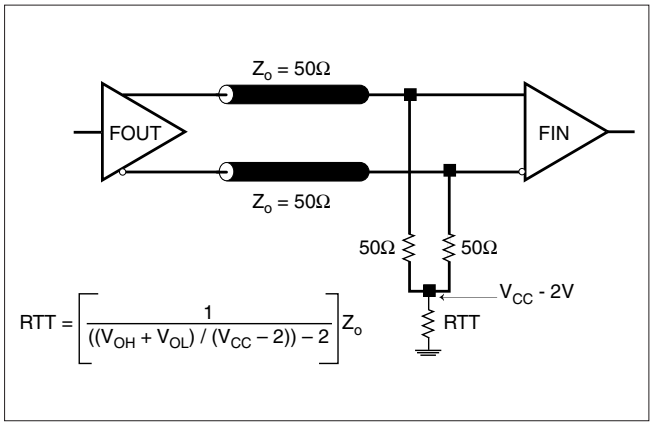


FIGURE 3A. LVPECL OUTPUT TERMINATION

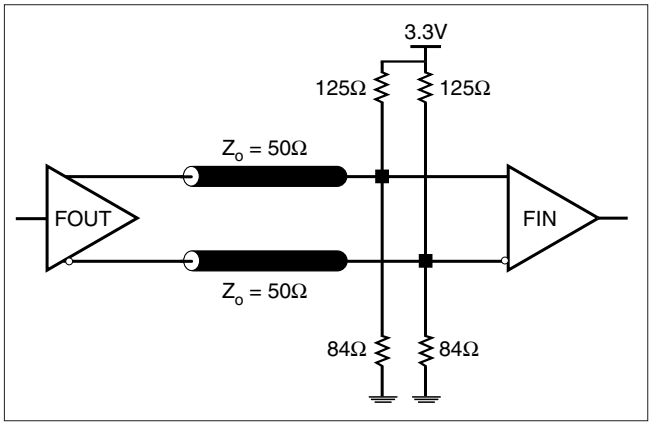


FIGURE 3B. LVPECL OUTPUT TERMINATION

LAYOUT GUIDELINE

Figure 4 shows an example of ICS843004-02 application schematic. In this example, the device is operated at V_{CC}=3.3V. The decoupling capacitor should be located as close as possible to the power pin. Both input options are shown. The device can either be driven using a quartz crystal or a 3.3V LVCMOS signal. For the LVPECL output drivers, only two termination examples are shown in this schematic. Additional termination approaches are shown in the LVPECL Termination Application Note.

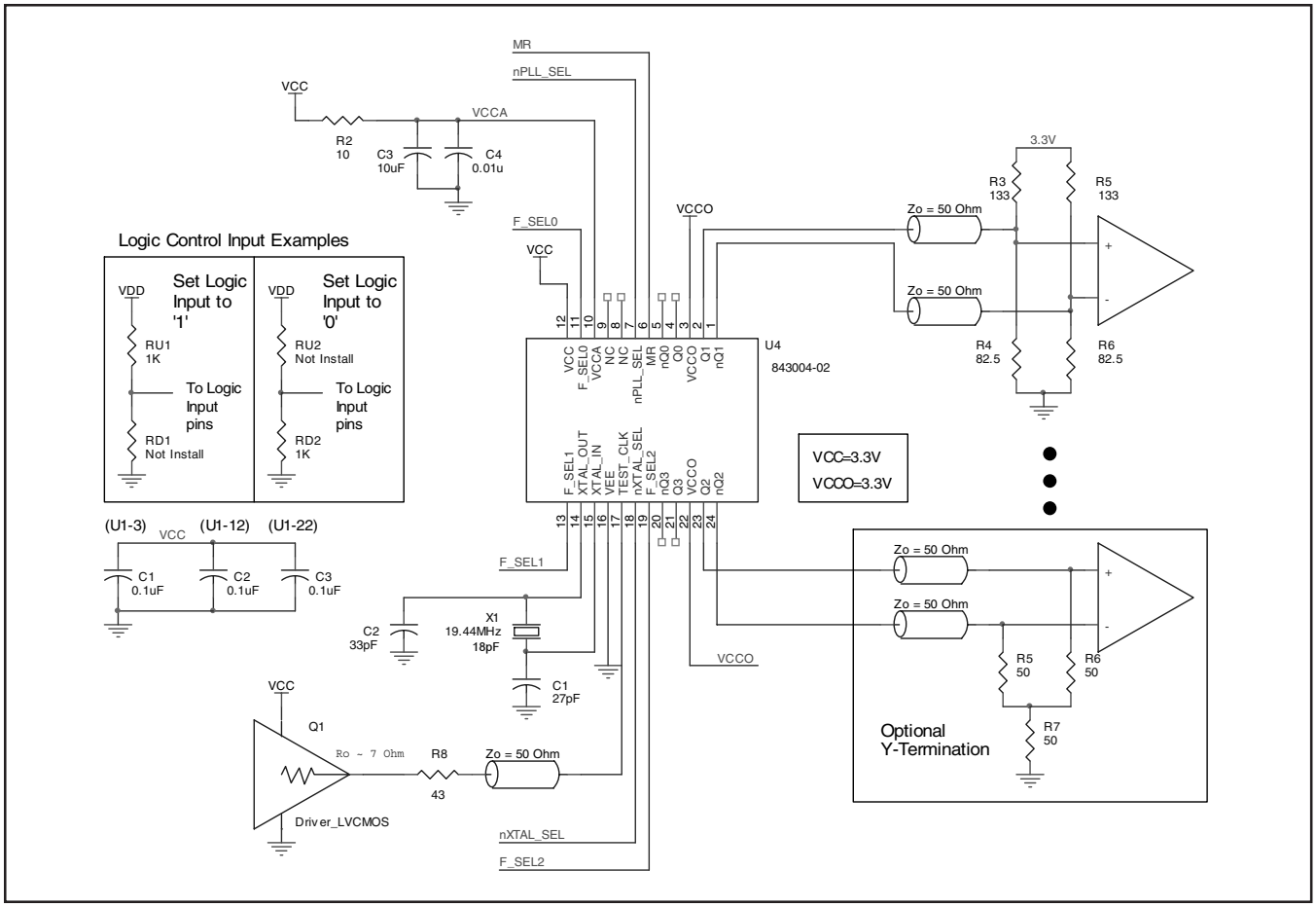


FIGURE 4. ICS843004-02 SCHEMATIC EXAMPLE

RELIABILITY INFORMATION

TABLE 7. θ_{JA} VS. AIR FLOW TABLE FOR 24 LEAD TSSOP

θ_{JA} by Velocity (Meters per Second)			
	0	**1**	**2.5**
Multi-Layer PCB, JEDEC Standard Test Boards	70°C/W	65°C/W	62°C/W

TRANSISTOR COUNT

The transistor count for ICS843004-02 is: 3467

PACKAGE OUTLINE - G SUFFIX FOR 24 LEAD TSSOP

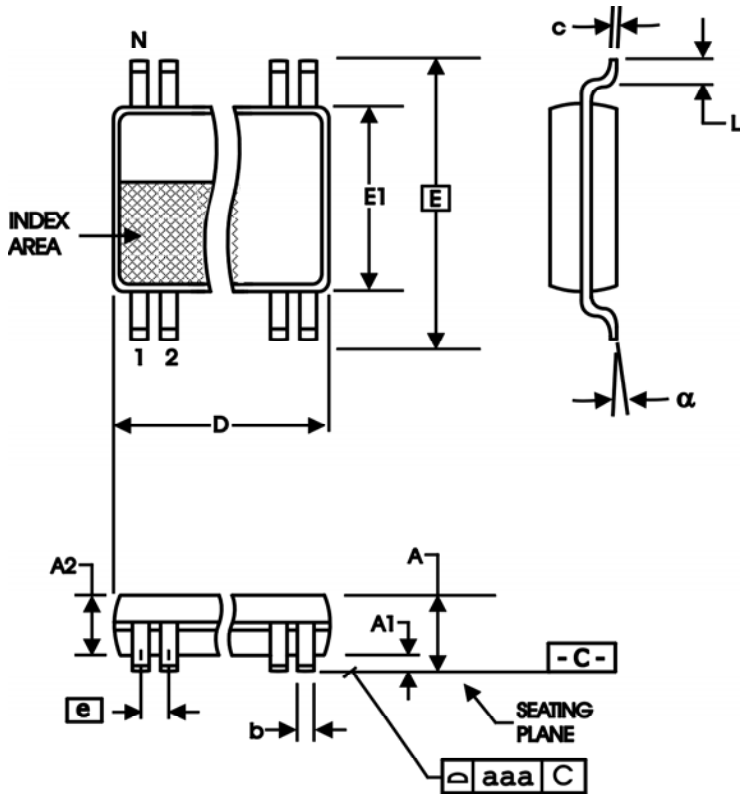


TABLE 8. PACKAGE DIMENSIONS

SYMBOL	Millimeters	
	Minimum	Maximum
N	24	
A	--	1.20
A1	0.05	0.15
A2	0.80	1.05
b	0.19	0.30
c	0.09	0.20
D	7.70	7.90
E	6.40 BASIC	
E1	4.30	4.50
e	0.65 BASIC	
L	0.45	0.75
α	0°	8°
aaa	--	0.10

Reference Document: JEDEC Publication 95, MO-153

TABLE 9. ORDERING INFORMATION

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
ICS843004AG-02	ICS843004A02	24 Lead TSSOP	tube	0°C to 70°C
ICS843004AG-02T	ICS843004A02	24 Lead TSSOP	2500 tape & reel	0°C to 70°C

The aforementioned trademark, HiPerClockS is a trademark of Integrated Circuit Systems, Inc. or its subsidiaries in the United States and/or other countries.

While the information presented herein has been checked for both accuracy and reliability, Integrated Circuit Systems, Incorporated (ICS) assumes no responsibility for either its use or for infringement of any patents or other rights of third parties, which would result from its use. No other circuits, patents, or licenses are implied. This product is intended for use in normal commercial applications. Any other applications such as those requiring extended temperature range, high reliability, or other extraordinary environmental requirements are not recommended without additional processing by ICS. ICS reserves the right to change any circuitry or specifications without notice. ICS does not authorize or warrant any ICS product for use in life support devices or critical medical instruments.