



STD16NE10L

N - CHANNEL 100V - 0.07 Ω - 16A DPAK STripFET™ POWER MOSFET

PRELIMINARY DATA

TYPE	V _{DSS}	R _{DS(on)}	I _D
STD16NE10L	100 V	< 0.10 Ω	16 A

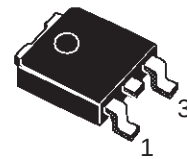
- TYPICAL R_{DS(on)} = 0.07 Ω
- AVALANCHE RUGGED TECHNOLOGY
- LOW GATE CHARGE
- HIGH CURRENT CAPABILITY
- 175 °C OPERATING TEMPERATURE
- LOW THRESHOLD DRIVE
- ADD SUFFIX "T4" FOR ORDERING IN TAPE & REEL

DESCRIPTION

This Power MOSFET is the latest development of STMicroelectronics unique "Single Feature Size™" strip-based process. The resulting transistor shows extremely high packing density for low on-resistance, rugged avalanche characteristics and less critical alignment steps therefore a remarkable manufacturing reproducibility.

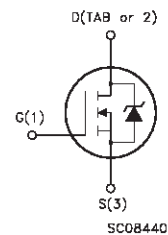
APPLICATIONS

- HIGH CURRENT, HIGH SPEED SWITCHING
- SOLENOID AND RELAY DRIVERS
- DC-DC & DC-AC CONVERTERS
- AUTOMOTIVE ENVIRONMENT



**DPAK
TO-252**
(Suffix "T4")

INTERNAL SCHEMATIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V _{DS}	Drain-source Voltage (V _{GS} = 0)	100	V
V _{DGR}	Drain- gate Voltage (R _{GS} = 20 k Ω)	100	V
V _{GS}	Gate-source Voltage	± 20	V
I _D	Drain Current (continuous) at T _c = 25 °C	16	A
I _D	Drain Current (continuous) at T _c = 100 °C	11	A
I _{DM} (•)	Drain Current (pulsed)	64	A
P _{tot}	Total Dissipation at T _c = 25 °C	55	W
	Derating Factor	0.36	W/°C
dv/dt (1)	Peak Diode Recovery voltage slope	7	V/ns
T _{stg}	Storage Temperature	-65 to 175	°C
T _j	Max. Operating Junction Temperature	175	°C

(•) Pulse width limited by safe operating area

(1) I_{SD} ≤ 16A, di/dt ≤ 300 A/ μ S, V_{DD} ≤ V_{(BR)DSS}, T_j ≤ T_{JMAX}

STD16NE10L

THERMAL DATA

$R_{thj-pcb}$	Thermal Resistance Junction-PC Board	Max	2.73	$^{\circ}\text{C}/\text{W}$
$R_{thj-amb}$	Thermal Resistance Junction-ambient	Max	100	$^{\circ}\text{C}/\text{W}$
$R_{thj-sink}$	Thermal Resistance Case-sink	Typ	1.5	$^{\circ}\text{C}/\text{W}$
T_I	Maximum Lead Temperature For Soldering Purpose		275	$^{\circ}\text{C}$

AVALANCHE CHARACTERISTICS

Symbol	Parameter	Max Value	Unit
I_{AR}	Avalanche Current, Repetitive or Not-Repetitive (pulse width limited by T_j max)	16	A
E_{AS}	Single Pulse Avalanche Energy (starting $T_j = 25^{\circ}\text{C}$, $I_D = I_{AR}$, $V_{DD} = 30\text{ V}$)	75	mJ

ELECTRICAL CHARACTERISTICS ($T_{case} = 25^{\circ}\text{C}$ unless otherwise specified)

OFF

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source Breakdown Voltage	$I_D = 250\text{ }\mu\text{A}$ $V_{GS} = 0$	100			V
I_{DSS}	Zero Gate Voltage Drain Current ($V_{GS} = 0$)	$V_{DS} = \text{Max Rating}$ $V_{DS} = \text{Max Rating}$ $T_c = 125^{\circ}\text{C}$			1 10	μA μA
I_{GSS}	Gate-body Leakage Current ($V_{DS} = 0$)	$V_{GS} = \pm 20\text{ V}$			± 100	nA

ON (*)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}$ $I_D = 250\text{ }\mu\text{A}$	1	1.7	2.5	V
$R_{DS(on)}$	Static Drain-source On Resistance	$V_{GS} = 10\text{ V}$ $I_D = 8\text{ A}$ $V_{GS} = 5\text{ V}$ $I_D = 8\text{ A}$		0.07 0.085	0.085 0.1	Ω Ω
$I_{D(on)}$	On State Drain Current	$V_{DS} > I_{D(on)} \times R_{DS(on)max}$ $V_{GS} = 10\text{ V}$	16			A

DYNAMIC

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$g_{fs} (*)$	Forward Transconductance	$V_{DS} > I_{D(on)} \times R_{DS(on)max}$ $I_D = 8\text{ A}$	5	9		S
C_{iss} C_{oss} C_{rss}	Input Capacitance Output Capacitance Reverse Transfer Capacitance	$V_{DS} = 25\text{ V}$ $f = 1\text{ MHz}$ $V_{GS} = 0\text{ V}$		1750 165 45		pF pF pF

ELECTRICAL CHARACTERISTICS (continued)**SWITCHING ON**

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on Delay Time	$V_{DD} = 50\text{ V}$ $I_D = 8\text{ A}$		40		ns
t_r	Rise Time	$R_G = 4.7\ \Omega$ $V_{GS} = 4.5\text{ V}$ (Resistive Load, see fig. 3)		80		ns
Q_g	Total Gate Charge	$V_{DD} = 80\text{ V}$ $I_D = 16\text{ A}$ $V_{GS} = 5\text{ V}$		24	32	nC
Q_{gs}	Gate-Source Charge			5.5		nC
Q_{gd}	Gate-Drain Charge			11		nC

SWITCHING OFF

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{d(off)}$	Turn-off Delay Time	$V_{DD} = 50\text{ V}$ $I_D = 8\text{ A}$		45		ns
t_f	Fall Time	$R_G = 4.7\ \Omega$ $V_{GS} = 4.5\text{ V}$ (Resistive Load, see fig. 3)		12		ns
$t_{r(voff)}$	Off-voltage Rise Time	$V_{DD} = 80\text{ V}$ $I_D = 16\text{ A}$		12		ns
t_f	Fall Time	$R_G = 4.7\ \Omega$ $V_{GS} = 4.5\text{ V}$		17		ns
t_c	Cross-over Time	(Inductive Load, see fig. 5)		35		ns

SOURCE DRAIN DIODE

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain Current				16	A
$I_{SDM}(\bullet)$	Source-drain Current (pulsed)				64	A
$V_{SD} (*)$	Forward On Voltage	$I_{SD} = 16\text{ A}$ $V_{GS} = 0$			1.5	V
t_{rr}	Reverse Recovery Time	$I_{SD} = 16\text{ A}$ $di/dt = 100\text{ A}/\mu\text{s}$ $V_{DD} = 40\text{ V}$ $T_J = 150\text{ }^\circ\text{C}$ (see test circuit, fig. 5)		100		ns
Q_{rr}	Reverse Recovery Charge			300		nC
I_{RRM}	Reverse Recovery Current			6		A

(*) Pulsed: Pulse duration = 300 μs , duty cycle 1.5 %

(\bullet) Pulse width limited by safe operating area

Fig. 1: Unclamped Inductive Load Test Circuit

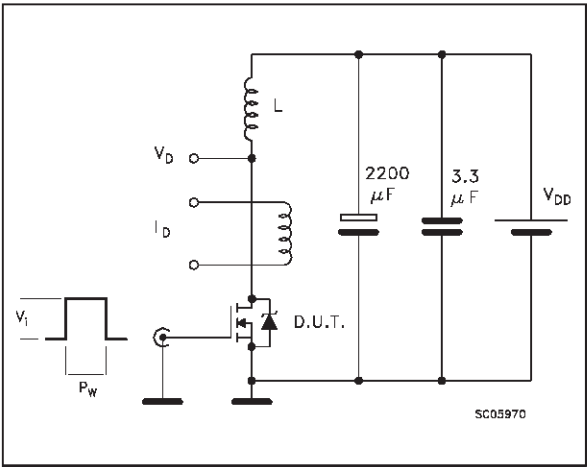


Fig. 2: Unclamped Inductive Waveform

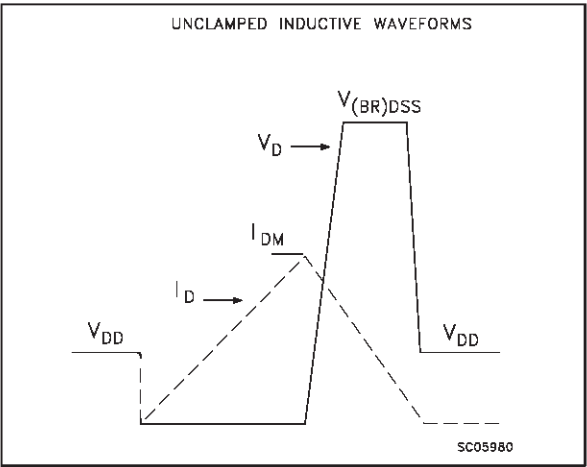


Fig. 3: Switching Times Test Circuits For Resistive Load

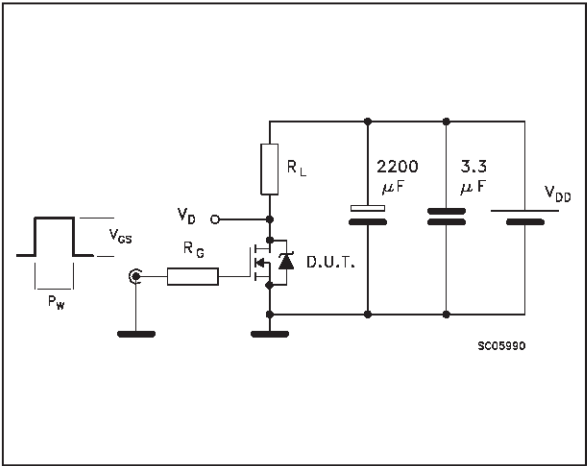


Fig. 4: Gate Charge test Circuit

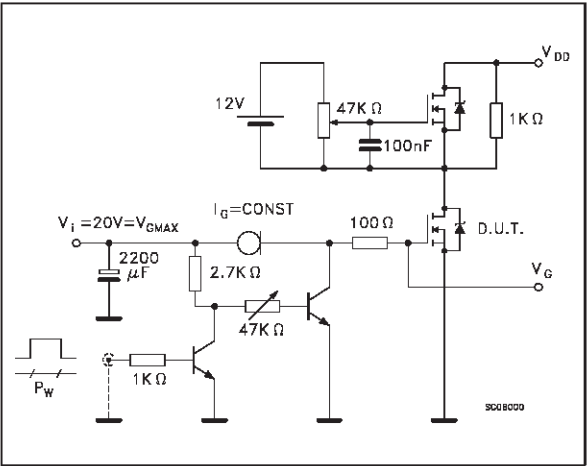
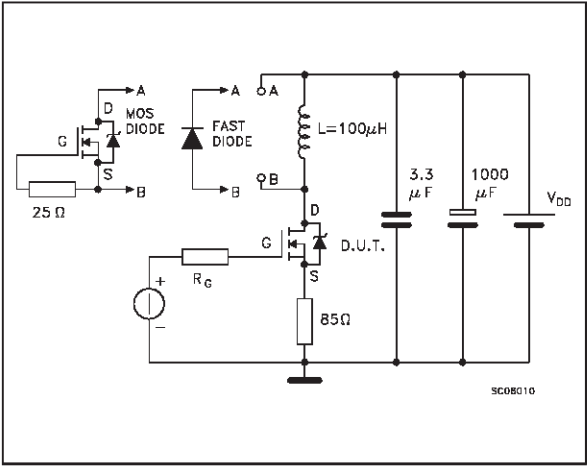
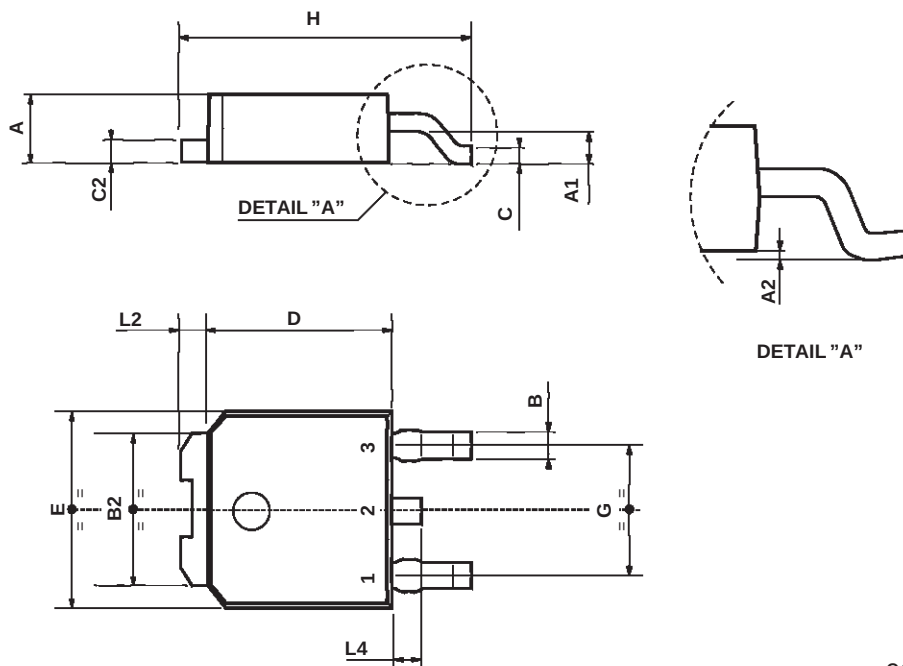


Fig. 5: Test Circuit For Inductive Load Switching And Diode Recovery Times



TO-252 (DPAK) MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	2.2		2.4	0.086		0.094
A1	0.9		1.1	0.035		0.043
A2	0.03		0.23	0.001		0.009
B	0.64		0.9	0.025		0.035
B2	5.2		5.4	0.204		0.212
C	0.45		0.6	0.017		0.023
C2	0.48		0.6	0.019		0.023
D	6		6.2	0.236		0.244
E	6.4		6.6	0.252		0.260
G	4.4		4.6	0.173		0.181
H	9.35		10.1	0.368		0.397
L2		0.8			0.031	
L4	0.6		1	0.023		0.039



Information furnished is believed to be accurate and reliable. However, STMicroelectronics assumes no responsibility for the consequences of use of such information nor for any infringement of patents or other rights of third parties which may result from its use. No license is granted by implication or otherwise under any patent or patent rights of STMicroelectronics. Specification mentioned in this publication are subject to change without notice. This publication supersedes and replaces all information previously supplied. STMicroelectronics products are not authorized for use as critical components in life support devices or systems without express written approval of STMicroelectronics.

The ST logo is a trademark of STMicroelectronics

© 2000 STMicroelectronics – Printed in Italy – All Rights Reserved

STMicroelectronics GROUP OF COMPANIES

Australia - Brazil - China - Finland - France - Germany - Hong Kong - India - Italy - Japan - Malaysia - Malta - Morocco -
Singapore - Spain - Sweden - Switzerland - United Kingdom - U.S.A.

<http://www.st.com>