ADSP-21060 Industrial SHARC® DSP Microcomputer Family

ADSP-21060C/ADSP-21060LC

SUMMARY

High Performance Signal Processor for Communications, Graphics, and Imaging Applications

Super Harvard Architecture
Four Independent Buses for Dual Data Fetch, Instruction Fetch, and Nonintrusive I/O

32-Bit IEEE Floating-Point Computation Units—Multiplier, ALU, and Shifter

Dual-Ported On-Chip SRAM and Integrated I/O Peripherals—A Complete System-On-A-Chip

Integrated Multiprocessing Features

Industrial Temperature Grade Hermetic Ceramic QFP Package

KEY FEATURES

40 MIPS, 25 ns Instruction Rate, Single-Cycle Instruction Execution

120 MFLOPS Peak, 80 MFLOPS Sustained Performance

Dual Data Address Generators with Modulo and Bit-Reverse Addressing

Efficient Program Sequencing with Zero-Overhead Looping: Single-Cycle Loop Setup

IEEE JTAG Standard 1149.1 Test Access Port and On-Chip Emulation

240-Lead Thermally Enhanced CQFP Package

32-Bit Single-Precision and 40-Bit Extended-Precision IEEE Floating-Point Data Formats or 32-Bit Fixed-Point Data Format

Parallel Computations

Single-Cycle Multiply and ALU Operations in Parallel with Dual Memory Read/Writes and Instruction Fetch

Multiply with Add and Subtract for Accelerated FFT Butterfly Computation

4 Mbit On-Chip SRAM

Dual-Ported for Independent Access by Core Processor and DMA

Off-Chip Memory Interfacing

4 Gigawords Addressable

Programmable Wait State Generation, Page-Mode DRAM Support

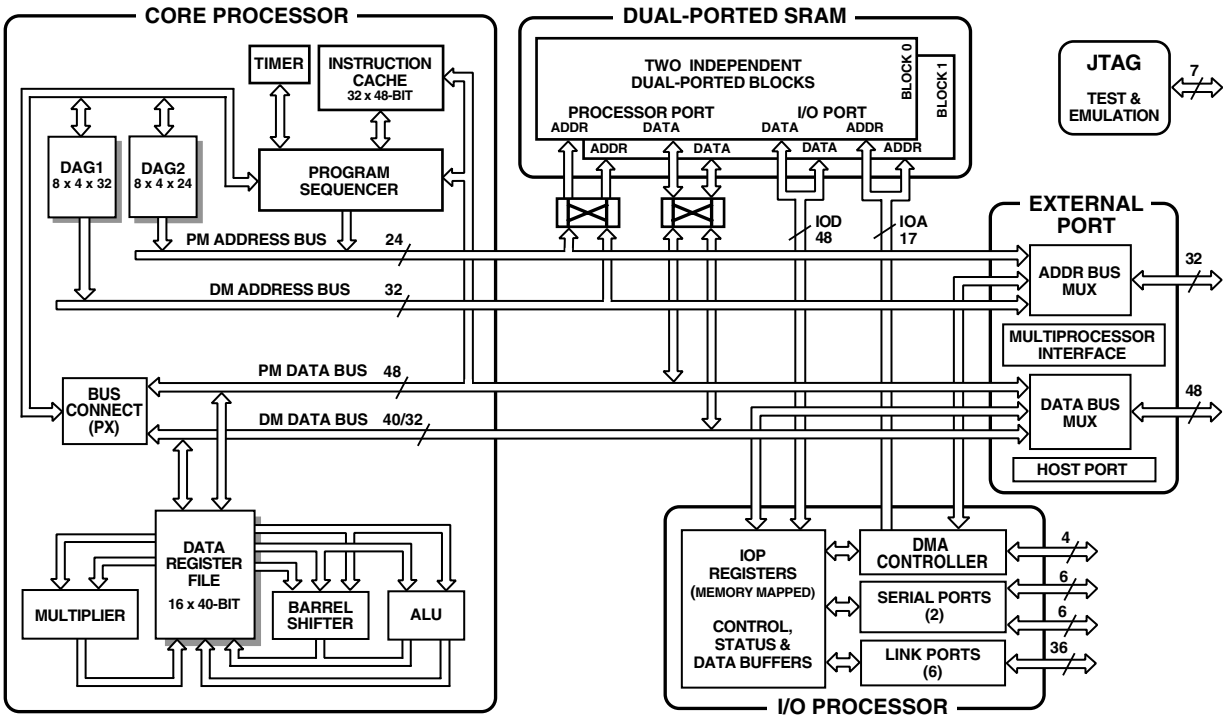

Figure 1. Block Diagram

REV. B

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DMA Controller

10 DMA Channels for Transfers Between ADSP-2106x Internal Memory and External Memory, External Peripherals, Host Processor, Serial Ports, or Link Ports

Background DMA Transfers at 40 MHz, in Parallel with Full-Speed Processor Execution

Host Processor Interface to 16- and 32-Bit Microprocessors

Host Can Directly Read/Write ADSP-2106x Internal Memory

Multiprocessing

Glueless Connection for Scalable DSP Multiprocessing Architecture

Distributed On-Chip Bus Arbitration for Parallel Bus Connect of Up to Six ADSP-2106xs Plus Host

Six Link Ports for Point-to-Point Connectivity and Array Multiprocessing

240 Mbytes/s Transfer Rate Over Parallel Bus

240 Mbytes/s Transfer Rate Over Link Ports

Serial Ports

Two 40 Mbit/s Synchronous Serial Ports with Companding Hardware

Independent Transmit and Receive Functions

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GENERAL DESCRIPTION

The ADSP-2106x SHARC—Super Harvard Architecture Computer—is a signal processing microcomputer that offers new capabilities and levels of performance. The ADSP-2106x SHARCs are 32-bit processors optimized for high performance DSP applications. The ADSP-2106x builds on the ADSP-21000 DSP core to form a complete system-on-a-chip, adding a dual-ported on-chip SRAM and integrated I/O peripherals supported by a dedicated I/O bus.

Fabricated in a high speed, low power CMOS process, the ADSP-2106x has a 25 ns instruction cycle time and operates at 40 MIPS. With its on-chip instruction cache, the processor can execute every instruction in a single cycle. Table I shows performance benchmarks for the ADSP-2106x.

The ADSP-2106x SHARC represents a new standard of integration for signal computers, combining a high performance floating-point DSP core with integrated, on-chip system features including a 4 Mbit SRAM memory host processor interface, DMA controller, serial ports, and link port and parallel bus connectivity for glueless DSP multiprocessing.

Figure 1 shows a block diagram of the ADSP-21060C/ADSP-21060LC, illustrating the following architectural features:

- Computation Units (ALU, Multiplier and Shifter) with a Shared Data Register File
- Data Address Generators (DAG1, DAG2)
- Program Sequencer with Instruction Cache
- Interval Timer
- On-Chip SRAM
- External Port for Interfacing to Off-Chip Memory and Peripherals
- Host Port and Multiprocessor Interface
- DMA Controller
- Serial Ports and Link Ports
- JTAG Test Access Port

Figure 2 shows a typical single-processor system. A multiprocessing system is shown in Figure 3.

Table I. ADSP-21060C/ADSP-21060LC Benchmarks (@ 40 MHz)

1024-Pt. Complex FFT (Radix 4, with Digit Reverse)	0.46 ms	18,221 cycles
FIR Filter (per Tap)	25 ns	1 cycle
IIR Filter (per Biquad)	100 ns	4 cycles
Divide (y/x)	150 ns	6 cycles
Inverse Square Root ($1/\sqrt{x}$)	225 ns	9 cycles
DMA Transfer Rate	240 Mbytes/s	

ADSP-21000 FAMILY CORE ARCHITECTURE

The ADSP-2106x includes the following architectural features of the ADSP-21000 family core. The ADSP-21060C is code- and function-compatible with the ADSP-21061 and ADSP-21062.

Independent, Parallel Computation Units

The arithmetic/logic unit (ALU), multiplier and shifter all perform single-cycle instructions. The three units are arranged in parallel, maximizing computational throughput. Single multifunction instructions execute parallel ALU and multiplier operations. These computation units support IEEE 32-bit single-precision floating-point, extended precision 40-bit floating-point, and 32-bit fixed-point data formats.

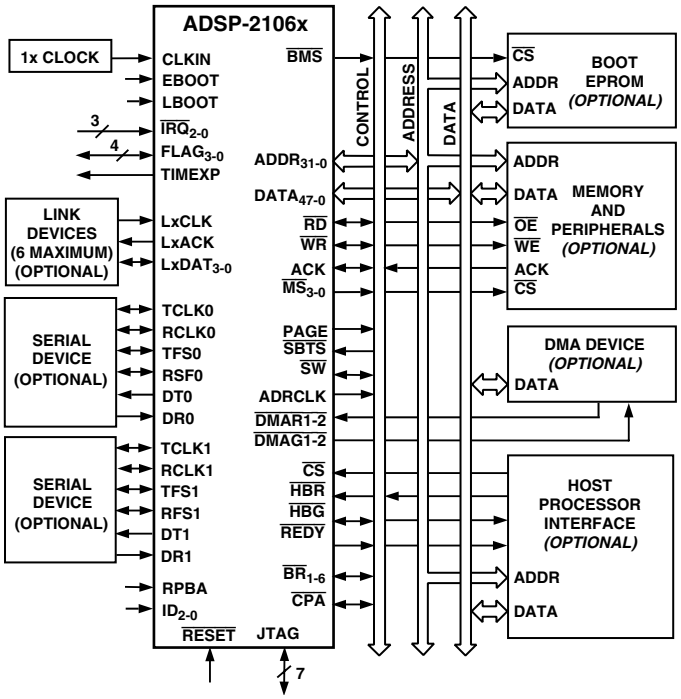


Figure 2. ADSP-2106x System

Data Register File

A general purpose data register file is used for transferring data between the computation units and the data buses, and for storing intermediate results. This 10-port, 32-register (16 primary, 16 secondary) register file, combined with the ADSP-21000 Harvard architecture, allows unconstrained data flow between computation units and internal memory.

Single-Cycle Fetch of Instruction and Two Operands

The ADSP-2106x features an enhanced Harvard architecture in which the data memory (DM) bus transfers data and the program memory (PM) bus transfers both instructions and data (see Figure 1). With its separate program and data memory buses and on-chip instruction cache, the processor can simultaneously fetch two operands and an instruction (from the cache), all in a single cycle.

Instruction Cache

The ADSP-2106x includes an on-chip instruction cache that enables three-bus operation for fetching an instruction and two data values. The cache is selective—only the instructions whose fetches conflict with PM bus data accesses are cached. This allows full-speed execution of core, looped operations such as digital filter multiply-accumulates and FFT butterfly processing.

Data Address Generators with Hardware Circular Buffers

The ADSP-2106x's two data address generators (DAGs) implement circular data buffers in hardware. Circular buffers allow efficient programming of delay lines and other data structures required in digital signal processing, and are commonly used in digital filters and Fourier transforms. The two DAGs of the ADSP-2106x contain sufficient registers to allow the creation of up to 32 circular buffers (16 primary register sets, 16 secondary). The DAGs automatically handle address pointer wrap-around, reducing overhead, increasing performance, and simplifying implementation. Circular buffers can start and end at any memory location.

Flexible Instruction Set

The 48-bit instruction word accommodates a variety of parallel operations, for concise programming. For example, the ADSP-2106x can conditionally execute a multiply, an add, a subtract and a branch, all in a single instruction.

ADSP-21060C/ADSP-21060LC FEATURES

Augmenting the ADSP-21000 family core, the ADSP-21060 adds the following architectural features:

Dual-Ported On-Chip Memory

The ADSP-21060C contains four megabits of on-chip SRAM, organized as two blocks of 2 Mbits each, which can be configured for different combinations of code and data storage. Each memory block is dual-ported for single-cycle, independent accesses by the core processor and I/O processor or DMA controller. The dual-ported memory and separate on-chip buses allow two data transfers from the core and one from I/O, all in a single cycle.

On the ADSP-21060C, the memory can be configured as a maximum of 128K words of 32-bit data, 256K words of 16-bit data, 80K words of 48-bit instructions (or 40-bit data), or combinations of different word sizes up to four megabits. All of the memory can be accessed as 16-bit, 32-bit, or 48-bit words.

A 16-bit floating-point storage format is supported that effectively doubles the amount of data that may be stored on-chip. Conversion between the 32-bit floating-point and 16-bit floating-point formats is done in a single instruction.

While each memory block can store combinations of code and data, accesses are most efficient when one block stores data, using the DM bus for transfers, and the other block stores instructions and data, using the PM bus for transfers. Using the DM bus and PM bus in this way, with one dedicated to each memory block, assures single-cycle execution with two data transfers. In this case, the instruction must be available in the cache. Single-cycle execution is also maintained when one of the data operands is transferred to or from off-chip, via the ADSP-2106x's external port.

Off-Chip Memory and Peripherals Interface
The ADSP-2106x's external port provides the processor's interface to off-chip memory and peripherals. The 4-gigaword off-chip address space is included in the ADSP-2106x's unified address space. The separate on-chip buses—for PM addresses, PM data, DM addresses, DM data, I/O addresses, and I/O data—are multiplexed at the external port to create an external system bus with a single 32-bit address bus and a single 48-bit (or 32-bit) data bus.

Addressing of external memory devices is facilitated by on-chip decoding of high-order address lines to generate memory bank select signals. Separate control lines are also generated for simplified addressing of page-mode DRAM. The ADSP-2106x provides programmable memory wait states and external memory acknowledge controls to allow interfacing to DRAM and peripherals with variable access, hold, and disable time requirements.

Host Processor Interface
The ADSP-2106x's host interface allows easy connection to standard microprocessor buses, both 16-bit and 32-bit, with little additional hardware required. Asynchronous transfers at speeds up to the full clock rate of the processor are supported. The host interface is accessed through the ADSP-2106x's external port and is memory-mapped into the unified address space. Four channels of DMA are available for the host interface; code and data transfers are accomplished with low software overhead.

The host processor requests the ADSP-2106x's external bus with the host bus request ($\overline{\text{HBR}}$), host bus grant ($\overline{\text{HBG}}$), and ready (REDY) signals. The host can directly read and write the internal memory of the ADSP-2106x, and can access the DMA channel setup and mailbox registers. Vector interrupt support is provided for efficient execution of host commands.

DMA Controller
The ADSP-2106x's on-chip DMA controller allows zero-overhead data transfers without processor intervention. The DMA controller operates independently and invisibly to the processor core, allowing DMA operations to occur while the core is simultaneously executing its program instructions.

DMA transfers can occur between the ADSP-2106x's internal memory and either external memory, external peripherals or a host processor. DMA transfers can also occur between the ADSP-2106x's internal memory and its serial ports or link ports. DMA transfers between external memory and external peripheral devices are another option. External bus packing to 16-, 32-, or 48-bit words is performed during DMA transfers.

Ten channels of DMA are available on the ADSP-2106x—two via the link ports, four via the serial ports, and four via the processor's external port (for either host processor, other ADSP-2106xs, memory or I/O transfers). Four additional link port DMA channels are shared with serial port 1 and the external port. Programs can be downloaded to the ADSP-2106x using DMA transfers. Asynchronous off-chip peripherals can control two DMA channels using DMA Request/Grant lines ($\overline{\text{DMAR1-2}}$, $\overline{\text{DMAG1-2}}$). Other DMA features include interrupt generation upon completion of DMA transfers and DMA chaining for automatic linked DMA transfers.

Serial Ports
The ADSP-2106x features two synchronous serial ports that provide an inexpensive interface to a wide variety of digital and mixed-signal peripheral devices. The serial ports can operate at the full clock rate of the processor, providing each with a maximum data rate of 40 Mbit/s. Independent transmit and receive functions provide greater flexibility for serial communications. Serial port data can be automatically transferred to and from on-chip memory via DMA. Each of the serial ports offers TDM multichannel mode.

The serial ports can operate with little-endian or big-endian transmission formats, with word lengths selectable from 3 bits to 32 bits. They offer selectable synchronization and transmit modes as well as optional μ-law or A-law companding. Serial port clocks and frame syncs can be internally or externally generated.

Multiprocessing
The ADSP-2106x offers powerful features tailored to multiprocessing DSP systems. The unified address space (see Figure 4) allows direct interprocessor accesses of each ADSP-2106x's internal memory. Distributed bus arbitration logic is included on-chip for simple, glueless connection of systems containing up to six ADSP-2106xs and a host processor. Master processor changeover incurs only one cycle of overhead. Bus arbitration is selectable as either fixed or rotating priority. Bus lock allows indivisible *read-modify-write* sequences for semaphores. A vector interrupt is provided for interprocessor commands. Maximum throughput for interprocessor data transfer is 240 Mbytes/s over the link ports or external port. *Broadcast writes* allow simultaneous transmission of data to all ADSP-2106xs and can be used to implement reflective semaphores.

Link Ports
The ADSP-2106x features six 4-bit link ports that provide additional I/O capabilities. The link ports can be clocked twice per cycle, allowing each to transfer eight bits per cycle. Link port I/O is especially useful for point-to-point interprocessor communication in multiprocessing systems.

The link ports can operate independently and simultaneously, with a maximum data throughput of 240 Mbytes/s. Link port data is packed into 32- or 48-bit words, and can be directly read by the core processor or DMA-transferred to on-chip memory.

Each link port has its own double-buffered input and output registers. Clock/acknowledge handshaking controls link port transfers. Transfers are programmable as either transmit or receive.

Program Booting
The internal memory of the ADSP-2106x can be booted at system power-up from either an 8-bit EPROM, a host processor, or through one of the link ports. Selection of the boot source is controlled by the $\overline{\text{BMS}}$ (Boot Memory Select), EBOOT (EPROM Boot), and LBOOT (Link/Host Boot) pins. 32-bit and 16-bit host processors can be used for booting.

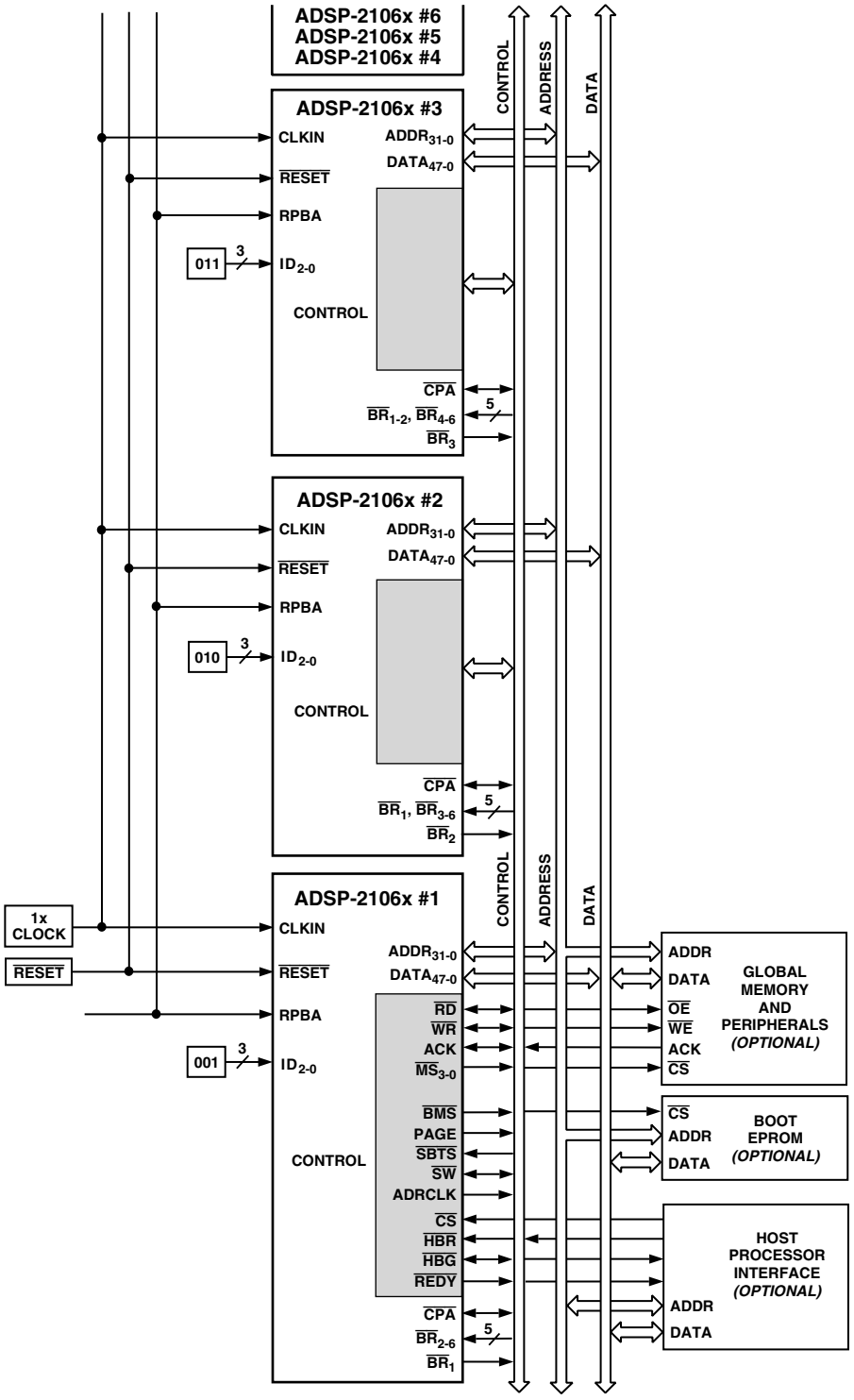


Figure 3. Shared Memory Multiprocessing System

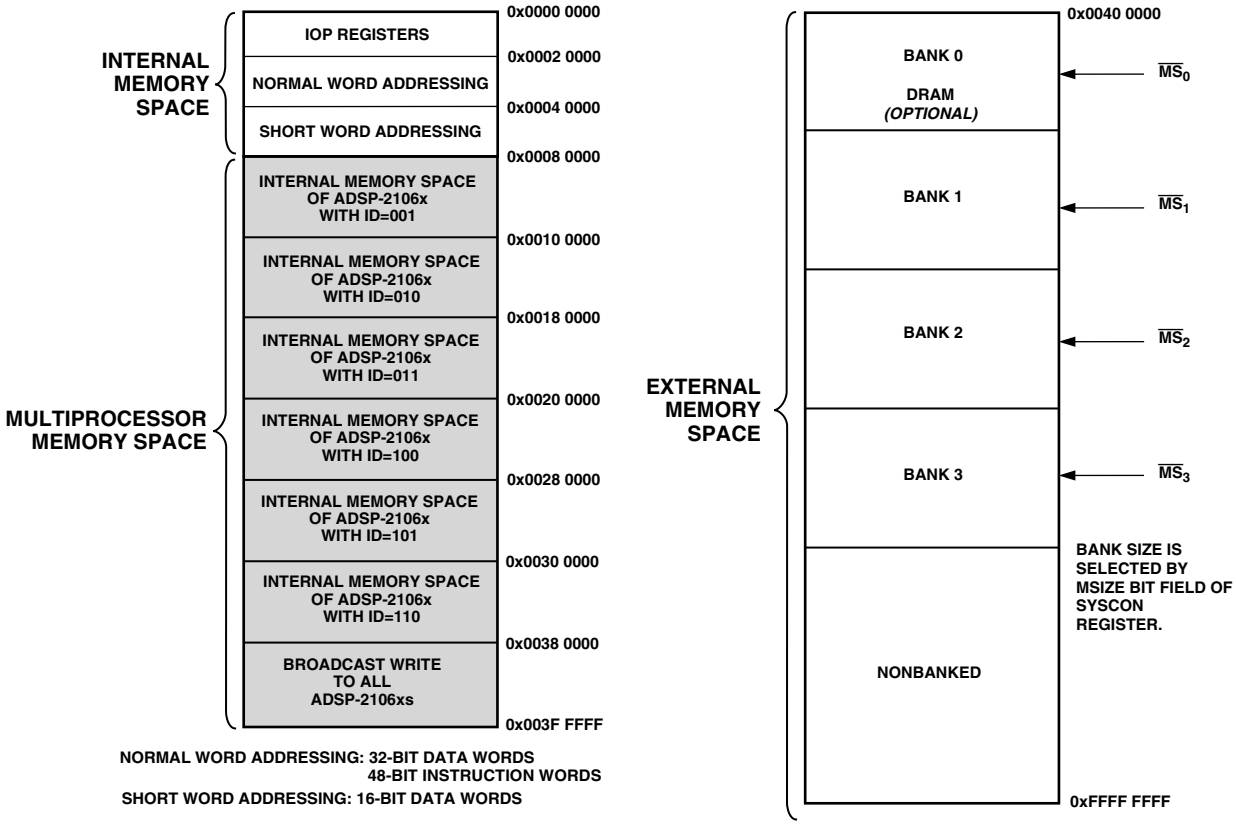


Figure 4. ADSP-21060C/ADSP-21060LC Memory Map

DEVELOPMENT TOOLS

The ADSP-21060C is supported with a complete set of software and hardware development tools, including an EZ-ICE In-Circuit Emulator, EZ-Kit, and development software. The SHARC EZ-Kit is a complete low cost package for DSP evaluation and prototyping. The EZ-Kit contains a PC plug-in card (EZ-LAB®) with an ADSP-21062 (5 V) processor. The EZ-Kit also includes an optimizing compiler, assembler, instruction level simulator, run-time libraries, diagnostic utilities and a complete set of example programs.

Analog Devices ADSP-21000 Family Development Software includes an easy to use Assembler based on an algebraic syntax, Assembly Library/Librarian, Linker, instruction-level Simulator, an ANSI C optimizing Compiler, the CBug™ C Source—Level Debugger and a C Runtime Library including DSP and mathematical functions. The ADSP-21000 Family Development Software is available for both the PC and Sun platforms.

The ADSP-2106x EZ-ICE Emulator uses the IEEE 1149.1 JTAG test access port of the ADSP-2106x processor to monitor and control the target board processor during emulation. The EZ-ICE provides full-speed emulation, allowing inspection and modification of memory, registers, and processor stacks. Nonintrusive in-circuit emulation is assured by the use of the processor's JTAG interface—the emulator does not affect target system loading or timing.

Further details and ordering information are available in the *ADSP-21000 Family Hardware and Software Development Tools* data sheet (ADDS-210xx-TOOLS). This data sheet can be requested from any Analog Devices sales office or distributor.

In addition to the software and hardware development tools available from Analog Devices, third parties provide a wide range of tools supporting the SHARC processor family. Hardware tools include SHARC PC plug-in cards multiprocessor SHARC VME boards, and daughter and modules with multiple SHARCs and additional memory. These modules are based on the SHARCPAC™ module specification. Third Party software tools include an Ada compiler, DSP libraries, operating systems and block diagram design tools.

ADDITIONAL INFORMATION

This data sheet provides a general overview of the ADSP-21060C architecture and functionality. For detailed information on the ADSP-21000 Family core architecture and instruction set, refer to the *ADSP-2106x SHARC User's Manual, Second Edition.*

PIN FUNCTION DESCRIPTIONS

ADSP-21060C pin definitions are listed below. All pins are identical on the ADSP-21060C and ADSP-21060LC. Inputs identified as synchronous (S) must meet timing requirements with respect to CLKIN (or with respect to TCK for TMS, TDI). Inputs identified as asynchronous (A) can be asserted asynchronously to CLKIN (or to TCK for $\overline{\text{TRST}}$).

Unused inputs should be tied or pulled to VDD or GND, except for $ADDR_{31-0}$, $DATA_{47-0}$, $FLAG_{3-0}$, $\overline{\text{SW}}$, and inputs that have internal pull-up or pull-down resistors ($\overline{\text{CPA}}$, ACK, DTx, DRx, TCLKx, RCLKx, $LxDAT_{3-0}$, LxCLK, LxACK, TMS and TDI)—these pins can be left floating. These pins have a logic-level hold circuit that prevents the input from floating internally.

A = Asynchronous G = Ground I = Input
O = Output P = Power Supply S = Synchronous
(A/D) = Active Drive (O/D) = Open Drain
T = Three-State (when $\overline{\text{SBTS}}$ is asserted, or when the ADSP-2106x is a bus slave)

Pin	Type	Function
$ADDR_{31-0}$	I/O/T	**External Bus Address**. The ADSP-2106x outputs addresses for external memory and peripherals on these pins. In a multiprocessor system the bus master outputs addresses for read/writes of the internal memory or IOP registers of other ADSP-2106xs. The ADSP-2106x inputs addresses when a host processor or multiprocessing bus master is reading or writing its internal memory or IOP registers.
$DATA_{47-0}$	I/O/T	**External Bus Data**. The ADSP-2106x inputs and outputs data and instructions on these pins. 32-bit single-precision floating-point data and 32-bit fixed-point data is transferred over bits 47–16 of the bus. 40-bit extended-precision floating-point data is transferred over bits 47–8 of the bus. 16-bit short word data is transferred over bits 31–16 of the bus. In PROM boot mode, 8-bit data is transferred over bits 23–16. Pull-up resistors on unused DATA pins are not necessary.
$\overline{\text{MS}}_{3-0}$	O/T	**Memory Select Lines**. These lines are asserted (low) as chip selects for the corresponding banks of external memory. Memory bank size must be defined in the ADSP-2106x's system control register (SYSCON). The $\overline{\text{MS}}_{3-0}$ lines are decoded memory address lines that change at the same time as the other address lines. When no external memory access is occurring the $\overline{\text{MS}}_{3-0}$ lines are inactive; they are active however when a conditional memory access instruction is executed, whether or not the condition is true. $\overline{\text{MS}}_0$ can be used with the PAGE signal to implement a bank of DRAM memory (Bank 0). In a multiprocessing system the $\overline{\text{MS}}_{3-0}$ lines are output by the bus master.
$\overline{\text{RD}}$	I/O/T	**Memory Read Strobe**. This pin is asserted (low) when the ADSP-2106x reads from external memory devices or from the internal memory of other ADSP-2106xs. External devices (including other ADSP-2106xs) must assert $\overline{\text{RD}}$ to read from the ADSP-2106x's internal memory. In a multiprocessing system $\overline{\text{RD}}$ is output by the bus master and is input by all other ADSP-2106xs.
$\overline{\text{WR}}$	I/O/T	**Memory Write Strobe**. This pin is asserted (low) when the ADSP-2106x writes to external memory devices or to the internal memory of other ADSP-2106xs. External devices must assert $\overline{\text{WR}}$ to write to the ADSP-2106x's internal memory. In a multiprocessing system $\overline{\text{WR}}$ is output by the bus master and is input by all other ADSP-2106xs.
PAGE	O/T	**DRAM Page Boundary**. The ADSP-2106x asserts this pin to signal that an external DRAM page boundary has been crossed. DRAM page size must be defined in the ADSP-2106x's memory control register (WAIT). DRAM can only be implemented in external memory Bank 0; the PAGE signal can only be activated for Bank 0 accesses. In a multiprocessing system PAGE is output by the bus master.
ADRCLK	O/T	**Clock Output Reference**. In a multiprocessing system ADRCLK is output by the bus master.
$\overline{\text{SW}}$	I/O/T	**Synchronous Write Select**. This signal is used to interface the ADSP-2106x to synchronous memory devices (including other ADSP-2106xs). The ADSP-2106x asserts $\overline{\text{SW}}$ (low) to provide an early indication of an impending write cycle, which can be aborted if $\overline{\text{WR}}$ is not later asserted (e.g., in a conditional write instruction). In a multiprocessing system, $\overline{\text{SW}}$ is output by the bus master and is input by all other ADSP-2106xs to determine if the multiprocessor memory access is a read or write. $\overline{\text{SW}}$ is asserted at the same time as the address output. A host processor using synchronous writes must assert this pin when writing to the ADSP-2106x(s).
ACK	I/O/S	**Memory Acknowledge**. External devices can deassert ACK (low) to add wait states to an external memory access. ACK is used by I/O devices, memory controllers, or other peripherals to hold off completion of an external memory access. The ADSP-2106x deasserts ACK as an output to add wait states to a synchronous access of its internal memory. In a multiprocessing system, a slave ADSP-2106x deasserts the bus master's ACK input to add wait state(s) to an access of its internal memory. The bus master has a keeper latch on its ACK pin that maintains the input at the level to which it was last driven.

Pin	Type	Function
$\overline{SBTS}$	I/S	**Suspend Bus Three-State**. External devices can assert $\overline{SBTS}$ (low) to place the external bus address, data, selects and strobes in a high impedance state for the following cycle. If the ADSP-2106x attempts to access external memory while $\overline{SBTS}$ is asserted, the processor will halt and the memory access will not be completed until $\overline{SBTS}$ is deasserted. $\overline{SBTS}$ should only be used to recover from host processor/ADSP-2106x deadlock, or used with a DRAM controller.
$\overline{IRQ}_{2-0}$	I/A	**Interrupt Request Lines**. May be either edge-triggered or level-sensitive.
$FLAG_{3-0}$	I/O/A	**Flag Pins**. Each is configured via control bits as either an input or output. As an input, it can be tested as a condition. As an output, it can be used to signal external peripherals.
TIMEXP	O	**Timer Expired**. Asserted for four cycles when the timer is enabled and TCOUNT decrements to zero.
$\overline{HBR}$	I/A	**Host Bus Request**. Must be asserted by a host processor to request control of the ADSP-2106x's external bus. When $\overline{HBR}$ is asserted in a multiprocessing system, the ADSP-2106x that is bus master will relinquish the bus and assert $\overline{HBG}$. To relinquish the bus, the ADSP-2106x places the address, data, select and strobe lines in a high impedance state. $\overline{HBR}$ has priority over all ADSP-2106x bus requests ($\overline{BR}_{6-1}$) in a multiprocessing system.
$\overline{HBG}$	I/O	**Host Bus Grant**. Acknowledges an $\overline{HBR}$ bus request, indicating that the host processor may take control of the external bus. $\overline{HBG}$ is asserted (held low) by the ADSP-2106x until $\overline{HBR}$ is released. In a multiprocessing system, $\overline{HBG}$ is output by the ADSP-2106x bus master and is monitored by all others.
$\overline{CS}$	I/A	**Chip Select**. Asserted by host processor to select the ADSP-2106x.
REDY (O/D)	O	**Host Bus Acknowledge**. The ADSP-2106x deasserts REDY (low) to add wait states to an asynchronous access of its internal memory or IOP registers by a host. Open drain output (O/D) by default; can be programmed in ADREDY bit of SYSCON register to be active drive (A/D). REDY will only be output if the $\overline{CS}$ and $\overline{HBR}$ inputs are asserted.
$\overline{DMAR1}$	I/A	**DMA Request 1** (DMA Channel 7).
$\overline{DMAR2}$	I/A	**DMA Request 2** (DMA Channel 8).
$\overline{DMAG1}$	O/T	**DMA Grant 1** (DMA Channel 7).
$\overline{DMAG2}$	O/T	**DMA Grant 2** (DMA Channel 8).
$\overline{BR}_{6-1}$	I/O/S	**Multiprocessing Bus Requests**. Used by multiprocessing ADSP-2106xs to arbitrate for bus mastership. An ADSP-2106x only drives its own $\overline{BR}$x line (corresponding to the value of its ID_{2-0} inputs) and monitors all others. In a multiprocessor system with less than six ADSP-2106xs, the unused $\overline{BR}$x pins should be pulled high; the processor's own $\overline{BR}$x line must not be pulled high or low because it is an output.
ID_{2-0}	I	**Multiprocessing ID**. Determines which multiprocessing bus request ($\overline{BR1}$ – $\overline{BR6}$) is used by ADSP-2106x. ID = 001 corresponds to $\overline{BR1}$, ID = 010 corresponds to $\overline{BR2}$, etc. ID = 000 in single-processor systems. These lines are a system configuration selection which should be hardwired or only changed at reset.
RPBA	I/S	**Rotating Priority Bus Arbitration Select**. When RPBA is high, rotating priority for multiprocessor bus arbitration is selected. When RPBA is low, fixed priority is selected. This signal is a system configuration selection which must be set to the same value on every ADSP-2106x. If the value of RPBA is changed during system operation, it must be changed in the same CLKIN cycle on every ADSP-2106x.
$\overline{CPA}$ (O/D)	I/O	**Core Priority Access**. Asserting its $\overline{CPA}$ pin allows the core processor of an ADSP-2106x bus slave to interrupt background DMA transfers and gain access to the external bus. $\overline{CPA}$ is an open drain output that is connected to all ADSP-2106xs in the system. The $\overline{CPA}$ pin has an internal 5 kΩ pull-up resistor. If core access priority is not required in a system, the $\overline{CPA}$ pin should be left unconnected.
DTx	O	**Data Transmit** (Serial Ports 0, 1). Each DT pin has a 50 kΩ internal pull-up resistor.
DRx	I	**Data Receive** (Serial Ports 0, 1). Each DR pin has a 50 kΩ internal pull-up resistor.
TCLKx	I/O	**Transmit Clock** (Serial Ports 0, 1). Each TCLK pin has a 50 kΩ internal pull-up resistor.
RCLKx	I/O	**Receive Clock** (Serial Ports 0, 1). Each RCLK pin has a 50 kΩ internal pull-up resistor.

Pin	Type	Function
TFSx	I/O	**Transmit Frame Sync** (Serial Ports 0, 1).
RFSx	I/O	**Receive Frame Sync** (Serial Ports 0, 1).
$LxDAT_{3-0}$	I/O	**Link Port Data** (Link Ports 0–5). Each LxCLK pin has a 50 kΩ internal pull-down resistor that is enabled or disabled by the LPDRD bit of the LCOM register.
LxCLK	I/O	**Link Port Clock** (Link Ports 0–5). Each LxCLK pin has a 50 kΩ internal pull-down resistor that is enabled or disabled by the LPDRD bit of the LCOM register.
LxACK	I/O	**Link Port Acknowledge** (Link Ports 0–5). Each LxACK pin has a 50 kΩ internal pull-down resistor that is enabled or disabled by the LPDRD bit of the LCOM register.
EBOOT	I	**EPROM Boot Select**. When EBOOT is high, the ADSP-2106x is configured for booting from an 8-bit EPROM. When EBOOT is low, the LBOOT and $\overline{BMS}$ inputs determine booting mode. See table below. This signal is a system configuration selection that should be hardwired.
LBOOT	I	**Link Boot**. When LBOOT is high, the ADSP-2106x is configured for link port booting. When LBOOT is low, the ADSP-2106x is configured for host processor booting or no booting. See table below. This signal is a system configuration selection that should be hardwired.
$\overline{BMS}$	I/O/T*	**Boot Memory Select**. *Output*: Used as chip select for boot EPROM devices (when EBOOT = 1, LBOOT = 0). In a multiprocessor system, $\overline{BMS}$ is output by the bus master. *Input:* When low, indicates that no booting will occur and that ADSP-2106x will begin executing instructions from external memory. See table below. This input is a system configuration selection that should be hardwired. *Three-statable only in EPROM boot mode (when $\overline{BMS}$ is an output). *EBOOT* / *LBOOT* / *$\overline{BMS}$* / *Booting Mode* 1 / 0 / Output / EPROM (Connect $\overline{BMS}$ to EPROM chip select.) 0 / 0 / 1 (Input) / Host Processor 0 / 1 / 1 (Input) / Link Port 0 / 0 / 0 (Input) / No Booting. Processor executes from external memory. 0 / 1 / 0 (Input) / Reserved 1 / 1 / x (Input) / Reserved
CLKIN	I	**Clock In**. External clock input to the ADSP-2106x. The instruction cycle rate is equal to CLKIN. CLKIN may not be halted, changed, or operated below the minimum specified frequency.
$\overline{RESET}$	I/A	**Processor Reset**. Resets the ADSP-2106x to a known state and begins execution at the program memory location specified by the hardware reset vector address. This input must be asserted (low) at power-up.
TCK	I	**Test Clock (JTAG)**. Provides an asynchronous clock for JTAG boundary scan.
TMS	I/S	**Test Mode Select (JTAG)**. Used to control the test state machine. TMS has a 20 kΩ internal pull-up resistor.
TDI	I/S	**Test Data Input (JTAG)**. Provides serial data for the boundary scan logic. TDI has a 20 kΩ internal pull-up resistor.
TDO	O	**Test Data Output (JTAG)**. Serial scan output of the boundary scan path.
$\overline{TRST}$	I/A	**Test Reset (JTAG)**. Resets the test state machine. $\overline{TRST}$ must be asserted (pulsed low) after power-up or held low for proper operation of the ADSP-2106x. $\overline{TRST}$ has a 20 kΩ internal pull-up resistor.
$\overline{EMU}$ (O/D)	O	**Emulation Status**. Must be connected to the ADSP-2106x EZ-ICE target board connector *only*.
ICSA	O	**Reserved**, leave unconnected.
VDD	P	**Power Supply**; nominally 5.0 V dc for 5 V devices or 3.3 V dc for 3.3 V devices. (30 pins).
GND	G	**Power Supply Return**. (30 pins).
NC		**Do Not Connect**. Reserved pins which must be left open and unconnected.

TARGET BOARD CONNECTOR FOR EZ-ICE PROBE

The ADSP-2106x EZ-ICE Emulator uses the IEEE 1149.1 JTAG test access port of the ADSP-2106x to monitor and control the target board processor during emulation. The EZ-ICE probe requires the ADSP-2106x's CLKIN, TMS, TCK, $\overline{\text{TRST}}$, TDI, TDO, $\overline{\text{EMU}}$, and GND signals be made accessible on the target system via a 14-pin connector (a 2 row × 7 pin strip header) such as that shown in Figure 5. The EZ-ICE probe plugs directly onto this connector for chip-on-board emulation. You must add this connector to your target board design if you intend to use the ADSP-2106x EZ-ICE. The total trace length between the EZ-ICE connector and the furthest device sharing the EZ-ICE JTAG pins should be limited to 15 inches maximum for guaranteed operation. This length restriction must include EZ-ICE JTAG signals that are routed to one or more ADSP-2106x devices, or a combination of ADSP-2106x devices and other JTAG devices on the chain.

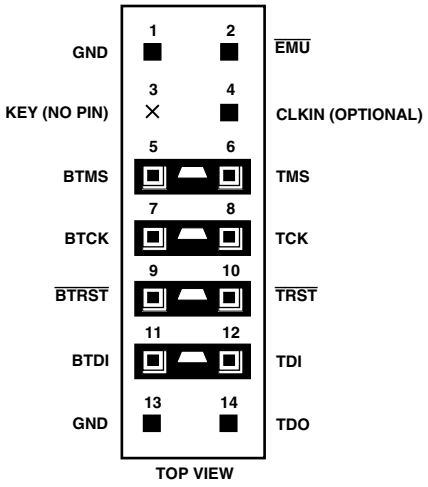


Figure 5. Target Board Connector for ADSP-2106x EZ-ICE Emulator (Jumpers in Place)

The 14-pin, 2-row pin strip header is keyed at the Pin 3 location — Pin 3 must be removed from the header. The pins must be 0.025 inch square and at least 0.20 inch in length. Pin spacing should be 0.1 × 0.1 inches. Pin strip headers are available from vendors such as 3M, McKenzie and Samtec.

The BTMS, BTCK, $\overline{\text{BTRST}}$ and BTDI signals are provided so the test access port can also be used for board-level testing. When the connector is not being used for emulation, place jumpers between the Bxxx pins and the xxx pins. If the test access port will not be used for board testing, tie $\overline{\text{BTRST}}$ to GND and tie or pull BTCK up to VDD. The $\overline{\text{TRST}}$ pin must be asserted after power-up (through $\overline{\text{BTRST}}$ on the connector) or held low for proper operation of the ADSP-2106x. None of the Bxxx pins (Pins 5, 7, 9, 11) are connected on the EZ-ICE probe.

The JTAG signals are terminated on the EZ-ICE probe as follows:

Signal	Termination
TMS	Driven through 22 Ω Resistor (16 mA Driver)
TCK	Driven at 10 MHz through 22 Ω Resistor (16 mA Driver)
$\overline{\text{TRST}}$*	Active Low Driven through 22 Ω Resistor (16 mA Driver) (Pulled Up by On-Chip 20 kΩ Resistor)
TDI	Driven by 22 Ω Resistor (16 mA Driver)
TDO	One TTL Load, Split Termination (160/220)
CLKIN	One TTL Load, Split Termination (160/220)
$\overline{\text{EMU}}$	Active Low 4.7 kΩ Pull-Up Resistor, One TTL Load (Open-Drain Output from the DSP)

*$\overline{\text{TRST}}$ is driven low until the EZ-ICE probe is turned on by the emulator at software start-up. After software start-up, $\overline{\text{TRST}}$ is driven high.

Figure 6 shows JTAG scan path connections for systems that contain multiple ADSP-2106x processors.

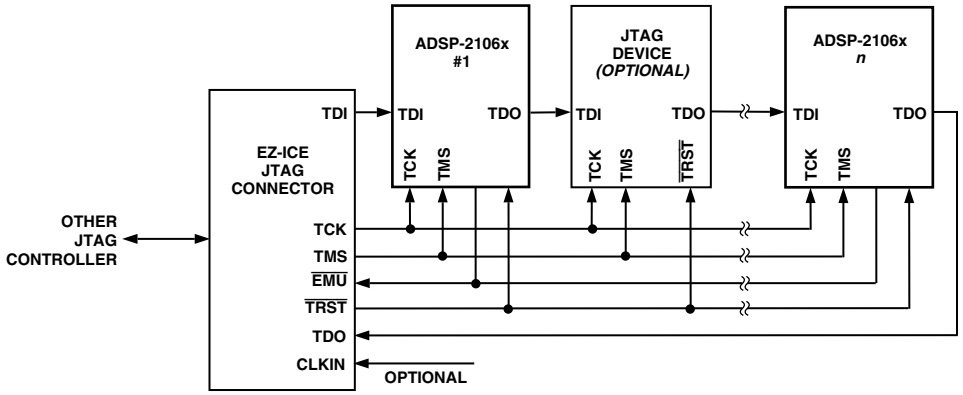


Figure 6. JTAG Scan Path Connections for Multiple ADSP-2106x Systems

Connecting CLKIN to Pin 4 of the EZ-ICE header is optional. The emulator only uses CLKIN when directed to perform operations such as starting, stopping and single-stepping multiple ADSP-21060 in a *synchronous* manner. If you do not need these operations to occur synchronously on the multiple processors, simply tie Pin 4 of the EZ-ICE header to ground.

If synchronous multiprocessor operations are needed and CLKIN is connected, clock skew between the multiple ADSP-21060C/ADSP-21060LC processors and the CLKIN pin on the EZ-ICE header *must be minimal*. If the skew is too large, synchronous operations may be off by one or more cycles between processors. For synchronous multiprocessor operation TCK, TMS, CLKIN and $\overline{\text{EMU}}$ should be treated as critical signals in terms of skew, and should be laid out as short as possible on your board. If TCK, TMS and CLKIN are driving a large number of ADSP-21060 (more than eight) in your system, then treat them as a clock tree using multiple drivers to minimize skew. (See Figure 7, JTAG Clock Tree, and Clock Distribution in the High Frequency Design Considerations section of the *ADSP-2106x User's Manual, Second Edition.*)

If synchronous multiprocessor operations are not needed (i.e., CLKIN is not connected), just use appropriate parallel termination on TCK and TMS. TDI, TDO, $\overline{\text{EMU}}$, and $\overline{\text{TRST}}$ are not critical signals in terms of skew.

For complete information on the SHARC EZ-ICE, see the *ADSP-2100 Family JTAG EZ-ICE User's Guide and Reference.*

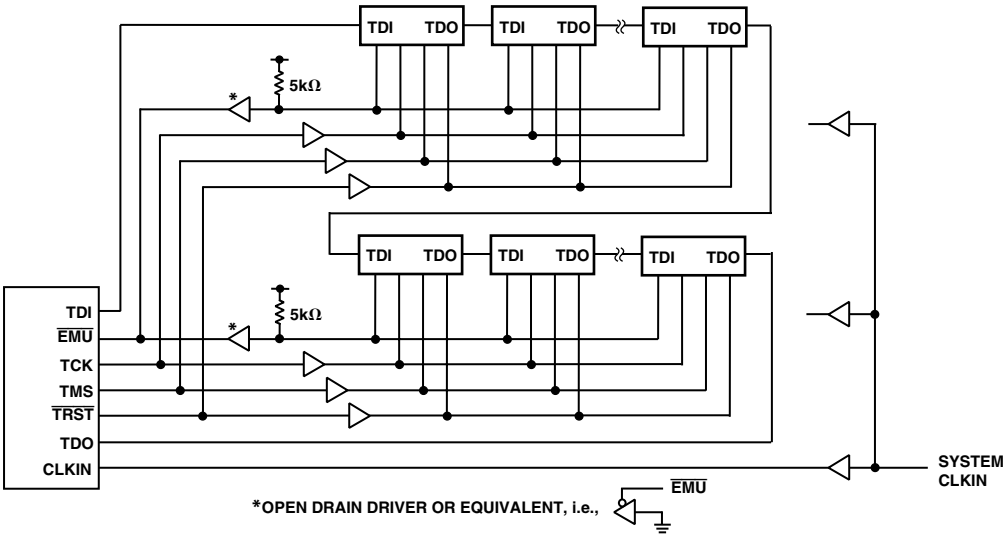


Figure 7. JTAG Clocktree for Multiple ADSP-2106x Systems

ADSP-21060C–SPECIFICATIONS

RECOMMENDED OPERATING CONDITIONS (5 V)

Parameter		Test Conditions	K Grade Min	K Grade Max	Unit
V_{DD}	Supply Voltage		4.75	5.25	V
T_{CASE}	Case Operating Temperature		–40	+100	°C
V_{IH1}	High Level Input Voltage[1]	@ V_{DD} = max	2.0	V_{DD} + 0.5	V
V_{IH2}	High Level Input Voltage[2]	@ V_{DD} = max	2.2	V_{DD} + 0.5	V
V_{IL}	Low Level Input Voltage[1, 2]	@ V_{DD} = min	–0.5	+0.8	V

NOTES
[1]Applies to input and bidirectional pins: $DATA_{47-0}$, $ADDR_{31-0}$, $\overline{RD}$, $\overline{WR}$, $\overline{SW}$, ACK, $\overline{SBTS}$, $\overline{IRQ}_{2-0}$, $FLAG_{3-0}$, $\overline{HBG}$, $\overline{CS}$, $\overline{DMAR1}$, $\overline{DMAR2}$, $\overline{BR}_{6-1}$, ID_{2-0}, RPBA, $\overline{CPA}$, TFS0, TFS1, RFS0, RFS1, $LxDAT_{3-0}$, LxCLK, LxACK, EBOOT, LBOOT, $\overline{BMS}$, TMS, TDI, TCK, $\overline{HBR}$, DR0, DR1, TCLK0, TCLK1, RCLK0, RCLK1.
[2]Applies to input pins: CLKIN, $\overline{RESET}$, $\overline{TRST}$.

ELECTRICAL CHARACTERISTICS (5 V)

Parameter		Test Conditions	Min	Max	Unit
V_{OH}	High Level Output Voltage[1]	@ V_{DD} = min, I_{OH} = –2.0 mA[2]	4.1		V
V_{OL}	Low Level Output Voltage[1]	@ V_{DD} = min, I_{OL} = 4.0 mA[2]		0.4	V
I_{IH}	High Level Input Current[3, 4]	@ V_{DD} = max, V_{IN} = V_{DD} max		10	µA
I_{IL}	Low Level Input Current[3]	@ V_{DD} = max, V_{IN} = 0 V		10	µA
I_{ILP}	Low Level Input Current[4]	@ V_{DD} = max, V_{IN} = 0 V		150	µA
I_{OZH}	Three-State Leakage Current[5, 6, 7, 8]	@ V_{DD} = max, V_{IN} = V_{DD} max		10	µA
I_{OZL}	Three-State Leakage Current[5, 9]	@ V_{DD} = max, V_{IN} = 0 V		10	µA
I_{OZHP}	Three-State Leakage Current[9]	@ V_{DD} = max, V_{IN} = V_{DD} max		350	µA
I_{OZLC}	Three-State Leakage Current[7]	@ V_{DD} = max, V_{IN} = 0 V		1.5	mA
I_{OZLA}	Three-State Leakage Current[10]	@ V_{DD} = max, V_{IN} = 1.5 V		350	µA
I_{OZLAR}	Three-State Leakage Current[8]	@ V_{DD} = max, V_{IN} = 0 V		4.2	mA
I_{OZLS}	Three-State Leakage Current[6]	@ V_{DD} = max, V_{IN} = 0 V		150	µA
C_{IN}	Input Capacitance[11, 12]	f_{IN} = 1 MHz, T_{CASE} = 25°C, V_{IN} = 2.5 V		4.7	pF

NOTES
[1]Applies to output and bidirectional pins: $DATA_{47-0}$, $ADDR_{31-0}$, $\overline{MS}_{3-0}$, $\overline{RD}$, $\overline{WR}$, PAGE, ADRCLK, $\overline{SW}$, ACK, $FLAG_{3-0}$, TIMEXP, $\overline{HBG}$, REDY, $\overline{DMAG1}$, $\overline{DMAG2}$, $\overline{BR}_{6-1}$, $\overline{CPA}$, DT0, DT1, TCLK0, TCLK1, RCLK0, RCLK1, TFS0, TFS1, RFS0, RFS1, $LxDAT_{3-0}$, LxCLK, LxACK, $\overline{BMS}$, TDO, $\overline{EMU}$, ICSA.
[2]See "Output Drive Currents" for typical drive current capabilities.
[3]Applies to input pins: $\overline{SBTS}$, $\overline{IRQ}_{2-0}$, $\overline{HBR}$, $\overline{CS}$, $\overline{DMAR1}$, $\overline{DMAR2}$, ID_{2-0}, RPBA, EBOOT, LBOOT, CLKIN, $\overline{RESET}$, TCK.
[4]Applies to input pins with internal pull-ups: DR0, DR1, $\overline{TRST}$, TMS, TDI.
[5]Applies to three-statable pins: $DATA_{47-0}$, $ADDR_{31-0}$, $\overline{MS}_{3-0}$, $\overline{RD}$, $\overline{WR}$, PAGE, ADRCLK, $\overline{SW}$, ACK, $FLAG_{3-0}$, REDY, $\overline{HBG}$, $\overline{DMAG1}$, $\overline{DMAG2}$, $\overline{BMS}$, $\overline{BR}_{6-1}$, TFS_X, RFS_X, TDO, $\overline{EMU}$. (Note that ACK is pulled up internally with 2 kΩ during reset in a multiprocessor system, when ID_{2-0} = 001 and another ADSP-21060 is not requesting bus mastership.)
[6]Applies to three-statable pins with internal pull-ups: DT0, DT1, TCLK0, TCLK1, RCLK0, RCLK1.
[7]Applies to $\overline{CPA}$ pin.
[8]Applies to ACK pin when pulled up. (Note that ACK is pulled up internally with 2 kΩ during reset in a multiprocessor system, when ID_{2-0} = 001 and another ADSP-21060 is not requesting bus mastership).
[9]Applies to three-statable pins with internal pull-downs: $LxDAT_{3-0}$, LxCLK, LxACK.
[10]Applies to ACK pin when keeper latch enabled.
[11]Applies to all signal pins.
[12]Guaranteed but not tested.

Specifications subject to change without notice.

POWER DISSIPATION ADSP-21060C (5 V)

These specifications apply to the internal power portion of V_{DD} only. See the Power Dissipation section of this data sheet for calculation of external supply current and total supply current. For a complete discussion of the code used to measure power dissipation, see the technical note "SHARC Power Dissipation Measurements."

Specifications are based on the following operating scenarios:

Operation	**Peak Activity ($I_{DDINPEAK}$)**	**High Activity ($I_{DDINHIGH}$)**	**Low Activity ($I_{DDINLOW}$)**
Instruction Type	Multifunction	Multifunction	Single Function
Instruction Fetch	Cache	Internal Memory	Internal Memory
Core Memory Access	2 per Cycle (DM and PM)	1 per Cycle (DM)	None
Internal Memory DMA	1 per Cycle	1 per 2 Cycles	1 per 2 Cycles

To estimate power consumption for a specific application, use the following equation where % is the amount of time your program spends in that state:

$$\%PEAK \times I_{DDINPEAK} + \%HIGH \times I_{DDINHIGH} + \%LOW \times I_{DDINLOW} + \%IDLE \times I_{DDIDLE} = power\ consumption$$

Parameter		**Test Conditions**	**Max**	**Unit**
$I_{DDINPEAK}$	Supply Current (Internal)[1]	t_{CK} = 30 ns, V_{DD} = max t_{CK} = 25 ns, V_{DD} = max	745 850	mA mA
$I_{DDINHIGH}$	Supply Current (Internal)[2]	t_{CK} = 30 ns, V_{DD} = max t_{CK} = 25 ns, V_{DD} = max	575 670	mA mA
$I_{DDINLOW}$	Supply Current (Internal)[2]	t_{CK} = 30 ns, V_{DD} = max t_{CK} = 25 ns, V_{DD} = max	340 390	mA mA
I_{DDIDLE}	Supply Current (Idle)[3]	V_{DD} = max	200	mA

NOTES

[1]The test program used to measure $I_{DDINPEAK}$ represents worst case processor operation and is not sustainable under normal application conditions. Actual internal power measurements made using typical applications are less than specified.

[2]$I_{DDINHIGH}$ is a composite average based on a range of high activity code. $I_{DDINLOW}$ is a composite average based on a range of low activity code.

[3]Idle denotes ADSP-21060C state during execution of IDLE instruction.

ADSP-21060LC–SPECIFICATIONS

RECOMMENDED OPERATING CONDITIONS (3.3 V)

Parameter		Test Conditions	K Grade Min	K Grade Max	Unit
V_{DD}	Supply Voltage		3.15	3.45	V
T_{CASE}	Case Operating Temperature		–40	+100	°C
V_{IH1}	High Level Input Voltage[1]	@ V_{DD} = max	2.0	V_{DD} + 0.5	V
V_{IH2}	High Level Input Voltage[2]	@ V_{DD} = max	2.2	V_{DD} + 0.5	V
V_{IL}	Low Level Input Voltage[1, 2]	@ V_{DD} = min	–0.5	0.8	V

NOTES
[1]Applies to input and bidirectional pins: $DATA_{47-0}$, $ADDR_{31-0}$, $\overline{RD}$, $\overline{WR}$, $\overline{SW}$, ACK, $\overline{SBTS}$, $\overline{IRQ}_{2-0}$, $FLAG_{3-0}$, $\overline{HBG}$, $\overline{CS}$, $\overline{DMAR1}$, $\overline{DMAR2}$, $\overline{BR}_{6-1}$, ID_{2-0}, RPBA, $\overline{CPA}$, TFS0, TFS1, RFS0, RFS1, $LxDAT_{3-0}$, LxCLK, LxACK, EBOOT, LBOOT, $\overline{BMS}$, TMS, TDI, TCK, $\overline{HBR}$, DR0, DR1, TCLK0, TCLK1, RCLK0, RCLK1.
[2]Applies to input pins: CLKIN, $\overline{RESET}$, $\overline{TRST}$.

ELECTRICAL CHARACTERISTICS (3.3 V)

Parameter		Test Conditions	Min	Max	Unit
V_{OH}	High Level Output Voltage[1]	@ V_{DD} = min, I_{OH} = –2.0 mA[2]	2.4		V
V_{OL}	Low Level Output Voltage[1]	@ V_{DD} = min, I_{OL} = 4.0 mA[2]		0.4	V
I_{IH}	High Level Input Current[3, 4]	@ V_{DD} = max, V_{IN} = V_{DD} max		10	µA
I_{IL}	Low Level Input Current[3]	@ V_{DD} = max, V_{IN} = 0 V		10	µA
I_{ILP}	Low Level Input Current[4]	@ V_{DD} = max, V_{IN} = 0 V		150	µA
I_{OZH}	Three-State Leakage Current[5, 6, 7, 8]	@ V_{DD} = max, V_{IN} = V_{DD} max		10	µA
I_{OZL}	Three-State Leakage Current[5, 9]	@ V_{DD} = max, V_{IN} = 0 V		10	µA
I_{OZHP}	Three-State Leakage Current[9]	@ V_{DD} = max, V_{IN} = V_{DD} max		350	µA
I_{OZLC}	Three-State Leakage Current[7]	@ V_{DD} = max, V_{IN} = 0 V		1.5	mA
I_{OZLA}	Three-State Leakage Current[10]	@ V_{DD} = max, V_{IN} = 2 V		350	µA
I_{OZLAR}	Three-State Leakage Current[8]	@ V_{DD} = max, V_{IN} = 0 V		4.2	mA
I_{OZLS}	Three-State Leakage Current[6]	@ V_{DD} = max, V_{IN} = 0 V		150	µA
C_{IN}	Input Capacitance[11, 12]	f_{IN} = 1 MHz, T_{CASE} = 25°C, V_{IN} = 2.5 V		4.7	pF

NOTES
[1]Applies to output and bidirectional pins: $DATA_{47-0}$, $ADDR_{31-0}$, $\overline{MS}_{3-0}$, $\overline{RD}$, $\overline{WR}$, PAGE, ADRCLK, $\overline{SW}$, ACK, $FLAG_{3-0}$, TIMEXP, $\overline{HBG}$, REDY, $\overline{DMAG1}$, $\overline{DMAG2}$, $\overline{BR}_{6-1}$, $\overline{CPA}$, DT0, DT1, TCLK0, TCLK1, RCLK0, RCLK1, TFS0, TFS1, RFS0, RFS1, $LxDAT_{3-0}$, LxCLK, LxACK, $\overline{BMS}$, TDO, $\overline{EMU}$, ICSA.
[2]See "Output Drive Currents" for typical drive current capabilities.
[3]Applies to input pins: ACK $\overline{SBTS}$, $\overline{IRQ}_{2-0}$, $\overline{HBR}$, $\overline{CS}$, $\overline{DMAR1}$, $\overline{DMAR2}$, ID_{2-0}, RPBA, EBOOT, LBOOT, CLKIN, $\overline{RESET}$, TCK.
[4]Applies to input pins with internal pull-ups: DR0, DR1, $\overline{TRST}$, TMS, TDI.
[5]Applies to three-statable pins: $DATA_{47-0}$, $ADDR_{31-0}$, $\overline{MS}_{3-0}$, $\overline{RD}$, $\overline{WR}$, PAGE, ADRCLK, $\overline{SW}$, ACK, $FLAG_{3-0}$, REDY, $\overline{HBG}$, $\overline{DMAG1}$, $\overline{DMAG2}$, $\overline{BMS}$, $\overline{BR}_{6-1}$, TFS_X, RFS_X, TDO, $\overline{EMU}$. (Note that ACK is pulled up internally with 2 kΩ during reset in a multiprocessor system, when ID_{2-0} = 001 and another ADSP-21060LC is not requesting bus mastership.)
[6]Applies to three-statable pins with internal pull-ups: DT0, DT1, TCLK0, TCLK1, RCLK0, RCLK1.
[7]Applies to $\overline{CPA}$ pin.
[8]Applies to ACK pin when pulled up. (Note that ACK is pulled up internally with 2 kΩ during reset in a multiprocessor system, when ID_{2-0} = 001 and another ADSP-21060LC is not requesting bus mastership).
[9]Applies to three-statable pins with internal pull-downs: $LxDAT_{3-0}$, LxCLK, LxACK.
[10]Applies to ACK pin when keeper latch enabled.
[11]Applies to all signal pins.
[12]Guaranteed but not tested.

Specifications subject to change without notice.

POWER DISSIPATION ADSP-21060LC (3.3 V)

These specifications apply to the internal power portion of V_{DD} only. See the Power Dissipation section of this data sheet for calculation of external supply current and total supply current. For a complete discussion of the code used to measure power dissipation, see the technical note "SHARC Power Dissipation Measurements."

Specifications are based on the following operating scenarios:

Operation	**Peak Activity ($I_{DDINPEAK}$)**	**High Activity ($I_{DDINHIGH}$)**	**Low Activity ($I_{DDINLOW}$)**
Instruction Type	Multifunction	Multifunction	Single Function
Instruction Fetch	Cache	Internal Memory	Internal Memory
Core Memory Access	2 per Cycle (DM and PM)	1 per Cycle (DM)	None
Internal Memory DMA	1 per Cycle	1 per 2 Cycles	1 per 2 Cycles

To estimate power consumption for a specific application, use the following equation where % is the amount of time your program spends in that state:

$$\%PEAK \times I_{DDINPEAK} + \%HIGH \times I_{DDINHIGH} + \%LOW \times I_{DDINLOW} + \%IDLE \times I_{DDIDLE} = power\ consumption$$

Parameter		**Test Conditions**	**Max**	**Unit**
$I_{DDINPEAK}$	Supply Current (Internal)[1]	t_{CK} = 30 ns, V_{DD} = max t_{CK} = 25 ns, V_{DD} = max	540 600	mA mA
$I_{DDINHIGH}$	Supply Current (Internal)[2]	t_{CK} = 30 ns, V_{DD} = max t_{CK} = 25 ns, V_{DD} = max	425 475	mA mA
$I_{DDINLOW}$	Supply Current (Internal)[2]	t_{CK} = 30 ns, V_{DD} = max t_{CK} = 25 ns, V_{DD} = max	250 275	mA mA
I_{DDIDLE}	Supply Current (Idle)[3]	V_{DD} = max	180	mA

NOTES

[1]The test program used to measure $I_{DDINPEAK}$ represents worst-case processor operation and is not sustainable under normal application conditions. Actual internal power measurements made using typical applications are less than specified.

[2]$I_{DDINHIGH}$ is a composite average based on a range of high activity code. $I_{DDINLOW}$ is a composite average based on a range of low activity code.

[3]Idle denotes ADSP-21060LC state during execution of IDLE instruction.

ABSOLUTE MAXIMUM RATINGS (5 V)*

Supply Voltage	–0.3 V to +7 V
Input Voltage	–0.5 V to V_{DD} + 0.5 V
Output Voltage Swing	–0.5 V to V_{DD} + 0.5 V
Load Capacitance	200 pF
Junction Temperature Under Bias	130°C
Storage Temperature Range	–65°C to +150°C
Lead Temperature (5 seconds)	280°C

*Stresses greater than those listed above may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions greater than those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ABSOLUTE MAXIMUM RATINGS (3.3 V)*

Supply Voltage	–0.3 V to +4.6 V
Input Voltage	–0.5 V to V_{DD} + 0.5 V
Output Voltage Swing	–0.5 V to V_{DD} + 0.5 V
Load Capacitance	200 pF
Junction Temperature Under Bias	130°C
Storage Temperature Range	–65°C to +150°C
Lead Temperature (5 seconds)	280°C

*Stresses greater than those listed above may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions greater than those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD SENSITIVITY

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the ADSP-21060C/ADSP-21060LC features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high-energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

TIMING SPECIFICATIONS

Two speed grades of the ADSP-21060C are offered, 40 MHz and 33.3 MHz. The specifications shown are based on a CLKIN frequency of 40 MHz (t_{CK} = 25 ns). The DT derating allows specifications at other CLKIN frequencies (within the min–max range of the t_{CK} specification; see Clock Input below). DT is the difference between the actual CLKIN period and a CLKIN period of 25 ns:

$$DT = t_{CK} - 25\ ns$$

Use the exact timing information given. Do not attempt to derive parameters from the addition or subtraction of others. While addition or subtraction would yield meaningful results for an individual device, the values given in this data sheet reflect statistical variations and worst cases. Consequently, you cannot meaningfully add parameters to derive longer times.

See Figure 28 under Test Conditions for voltage reference levels.

Switching Characteristics specify how the processor changes its signals. You have no control over this timing—circuitry external to the processor must be designed for compatibility with these signal characteristics. Switching characteristics tell you what the processor will do in a given circumstance. You can also use switching characteristics to ensure that any timing requirement of a device connected to the processor (such as memory) is satisfied.

Timing Requirements apply to signals that are controlled by circuitry external to the processor, such as the data input for a read operation. Timing requirements guarantee that the processor operates correctly with other devices.

(O/D) = Open Drain
(A/D) = Active Drive

Parameter		ADSP-21060C 40 MHz Min	ADSP-21060C 40 MHz Max	ADSP-21060C 33 MHz Min	ADSP-21060C 33 MHz Max	ADSP-21060LC 40 MHz Min	ADSP-21060LC 40 MHz Max	ADSP-21060LC 33 MHz Min	ADSP-21060LC 33 MHz Max	Unit
Clock Input										
Timing Requirements:										
t_{CK}	CLKIN Period	25	100	30	100	25	100	30	100	ns
t_{CKL}	CLKIN Width Low	7		7		9.5		9.5		ns
t_{CKH}	CLKIN Width High	5		5		5		5		ns
t_{CKRF}	CLKIN Rise/Fall (0.4 V–2.0 V)		3		3		3		3	ns

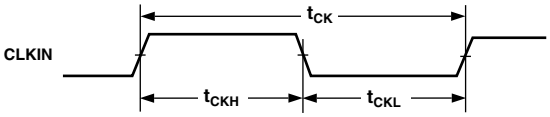


Figure 8. Clock Input

Parameter		ADSP-21060C Min	ADSP-21060C Max	ADSP-21060LC Min	ADSP-21060LC Max	Unit
Reset						
Timing Requirements:						
t_{WRST}	$\overline{\text{RESET}}$ Pulsewidth Low[1]	$4t_{CK}$		$4t_{CK}$		ns
t_{SRST}	$\overline{\text{RESET}}$ Setup before CLKIN High[2]	14 + DT/2	t_{CK}	14 + DT/2	t_{CK}	ns

NOTES
[1]Applies after the power-up sequence is complete. At power-up, the processor's internal phase-locked loop requires no more than 2000 CLKIN cycles while RESET is low, assuming stable V_{DD} and CLKIN (not including start-up time of external clock oscillator).
[2]Only required if multiple ADSP-2106xs must come out of reset synchronous to CLKIN with program counters (PC) equal (i.e., for a SIMD system). Not required for multiple ADSP-2106xs communicating over the shared bus (through the external port), because the bus arbitration logic synchronizes itself automatically after reset.

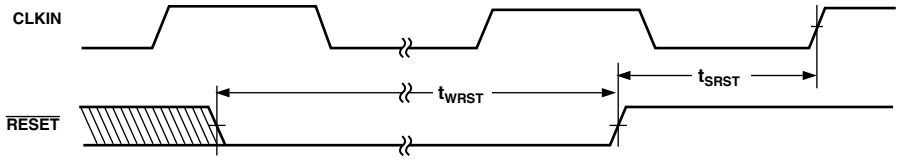


Figure 9. Reset

Parameter		ADSP-21060C Min	ADSP-21060C Max	ADSP-21060LC Min	ADSP-21060LC Max	Unit
Interrupts						
Timing Requirements:						
t_{SIR}	$\overline{\text{IRQ2-0}}$ Setup before CLKIN High[1]	18 + 3DT/4		18 + 3DT/4		ns
t_{HIR}	$\overline{\text{IRQ2-0}}$ Hold before CLKIN High[1]		12 + 3DT/4		12 + 3DT/4	ns
t_{IPW}	$\overline{\text{IRQ2-0}}$ Pulsewidth[2]	2 + t_{CK}		2 + t_{CK}		ns

NOTES
[1]Only required for $\overline{\text{IRQx}}$ recognition in the following cycle.
[2]Applies only if t_{SIR} and t_{HIR} requirements are not met.

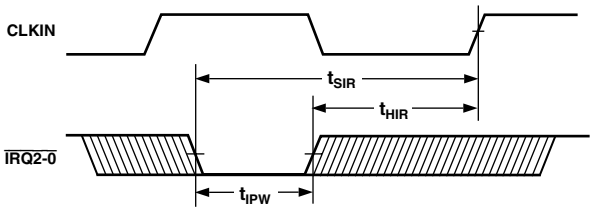


Figure 10. Interrupts

Parameter		ADSP-21060C Min	ADSP-21060C Max	ADSP-21060LC Min	ADSP-21060LC Max	Unit
Timer						
Switching Characteristic:						
t_{DTEX}	CLKIN High to TIMEXP		15		15	ns

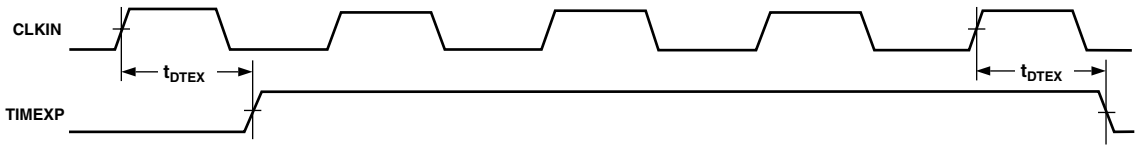


Figure 11. Timer

Parameter		ADSP-21060C Min	ADSP-21060C Max	ADSP-21060LC Min	ADSP-21060LC Max	Unit
Flags						
Timing Requirements:						
t_{SFI}	FLAG3-0$_{IN}$ Setup before CLKIN High[1]	8 + 5DT/16		8 + 5DT/16		ns
t_{HFI}	FLAG3-0$_{IN}$ Hold after CLKIN High[1]	0 – 5DT/16		0 – 5DT/16		ns
t_{DWRFI}	FLAG3-0$_{IN}$ Delay after $\overline{RD}$/$\overline{WR}$ Low[1]		5 + 7DT/16		5 + 7DT/16	ns
t_{HFIWR}	FLAG3-0$_{IN}$ Hold after $\overline{RD}$/$\overline{WR}$ Deasserted[1]	0		0		ns
Switching Characteristics:						
t_{DFO}	FLAG3-0$_{OUT}$ Delay after CLKIN High		16		16	ns
t_{HFO}	FLAG3-0$_{OUT}$ Hold after CLKIN High	4		4		ns
t_{DFOE}	CLKIN High to FLAG3-0$_{OUT}$ Enable	3		3		ns
t_{DFOD}	CLKIN High to FLAG3-0$_{OUT}$ Disable		14		14	ns

NOTE
[1]Flag inputs meeting these setup and hold times will affect conditional instructions in the following instruction cycle.

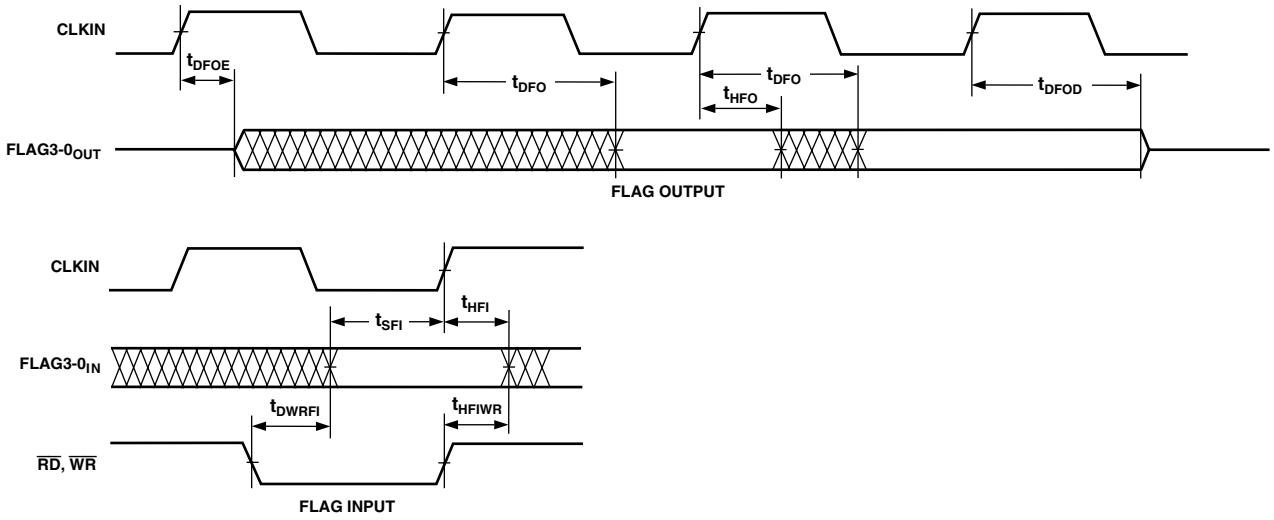


Figure 12. Flags

Memory Read—Bus Master

Use these specifications for asynchronous interfacing to memories (and memory-mapped peripherals) without reference to CLKIN. These specifications apply when the ADSP-2106x is the bus master accessing external memory space. These switching characteristics also apply for bus master synchronous read/write timing (see Synchronous Read/Write – Bus Master below). If these timing requirements are met, the synchronous read/write timing can be ignored (and vice versa).

Parameter		ADSP-21060C Min	ADSP-21060C Max	ADSP-21060LC Min	ADSP-21060LC Max	Unit
Timing Requirements:						
t_{DAD}	Address, Selects Delay to Data Valid[1, 2]		18 + DT + W		18 + DT + W	ns
t_{DRLD}	$\overline{RD}$ Low to Data Valid[1]		12 + 5DT/8 + W		12 + 5DT/8 + W	ns
t_{HDA}	Data Hold from Address, Selects[3]	0.5		0.5		ns
t_{HDRH}	Data Hold from $\overline{RD}$ High[3]	2.0		2.0		ns
t_{DAAK}	ACK Delay from Address, Selects[2, 4]		14 + 7DT/8 + W		14 + 7DT/8 + W	ns
t_{DSAK}	ACK Delay from $\overline{RD}$ Low[4]		8 + DT/2 + W		8 + DT/2 + W	ns
Switching Characteristics:						
t_{DRHA}	Address, Selects Hold after $\overline{RD}$ High	0 + H		0 + H		ns
t_{DARL}	Address, Selects to $\overline{RD}$ Low[2]	2 + 3DT/8		2 + 3DT/8		ns
t_{RW}	$\overline{RD}$ Pulsewidth	12.5 + 5DT/8 + W		12.5 + 5DT/8 + W		ns
t_{RWR}	$\overline{RD}$ High to $\overline{WR}$, $\overline{RD}$, $\overline{DMAG}$x Low	8 + 3DT/8 + HI		8 + 3DT/8 + HI		ns
t_{SADADC}	Address, Selects Setup before ADRCLK High[2]	0 + DT/4		0 + DT/4		ns

W = (number of wait states specified in WAIT register) × t_{CK}.
HI = t_{CK} (if an address hold cycle or bus idle cycle occurs, as specified in WAIT register; otherwise HI = 0).
H = t_{CK} (if an address hold cycle occurs as specified in WAIT register; otherwise H = 0).

NOTES
[1]Data Delay/Setup: User must meet t_{DAD} or t_{DRLD} or synchronous spec t_{SSDATI}.
[2]The falling edge of $\overline{MS}$x, $\overline{SW}$, $\overline{BMS}$ is referenced.
[3]Data Hold: User must meet t_{HDA} or t_{HDRH} or synchronous spec t_{HSDATI}. See *System Hold Time Calculation* under Test Conditions for the calculation of hold times given capacitive and dc loads.
[4]ACK Delay/Setup: User must meet t_{DAAK} or t_{DSAK} or synchronous specification t_{SACKC} for deassertion of ACK (Low), all three specifications must be met for assertion of ACK (High).

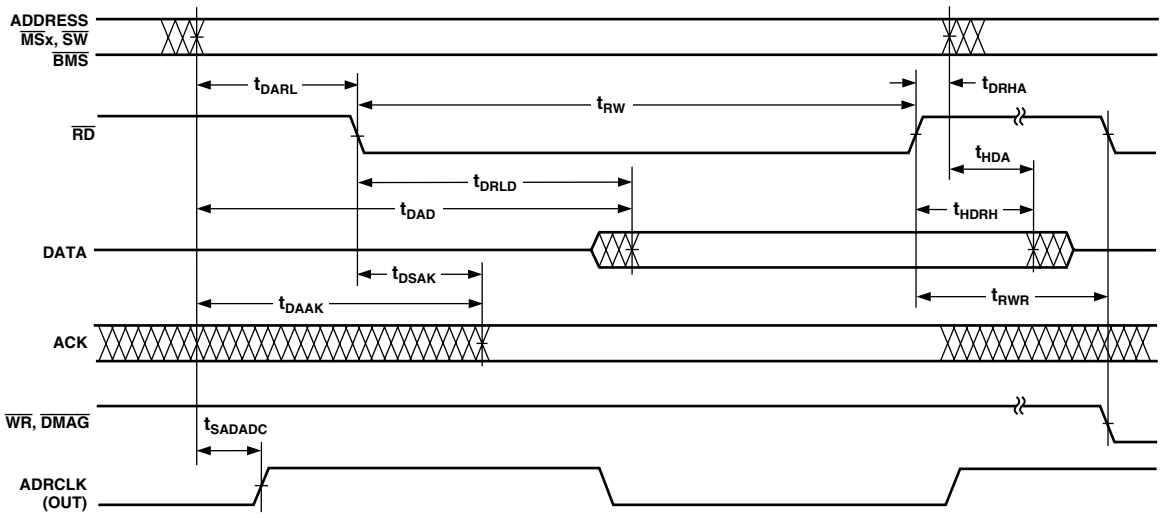


Figure 13. Memory Read—Bus Master

Memory Write—Bus Master

Use these specifications for asynchronous interfacing to memories (and memory-mapped peripherals) without reference to CLKIN. These specifications apply when the ADSP-2106x is the bus master accessing external memory space. These switching characteristics also apply for bus master synchronous read/write timing (see Synchronous Read/Write–Bus Master). If these timing requirements are met, the synchronous read/write timing can be ignored (and vice versa).

Parameter		ADSP-21060C Min	ADSP-21060C Max	ADSP-21060LC Min	ADSP-21060LC Max	Unit
Timing Requirements:						
t_{DAAK}	ACK Delay from Address, Selects[1, 2]		14 + 7DT/8 + W		14 + 7DT/8 + W	ns
t_{DSAK}	ACK Delay from $\overline{WR}$ Low[1]		8 + DT/2 + W		8 + DT/2 + W	ns
Switching Characteristics:						
t_{DAWH}	Address, Selects to $\overline{WR}$ Deasserted[2]	17 + 15DT/16 + W		17 + 15DT/16 + W		ns
t_{DAWL}	Address, Selects to $\overline{WR}$ Low[2]	3 + 3DT/8		3 + 3DT/8		ns
t_{WW}	$\overline{WR}$ Pulsewidth	12 + 9DT/16 + W		12 + 9DT/16 + W		ns
t_{DDWH}	Data Setup before $\overline{WR}$ High	7 + DT/2 + W		7 + DT/2 + W		ns
t_{DWHA}	Address Hold after $\overline{WR}$ Deasserted	0.5 + DT/16 + H		0.5 + DT/16 + H		ns
t_{DATRWH}	Data Disable after $\overline{WR}$ Deasserted[3]	1 + DT/16 + H	6 + DT/16 + H	1 + DT/16 + H	6 + DT/16 + H	ns
t_{WWR}	$\overline{WR}$ High to $\overline{WR}$, $\overline{RD}$, $\overline{DMAG}$x Low	8 + 7DT/16 + H		8 + 7DT/16 + H		ns
t_{DDWR}	Data Disable before $\overline{WR}$ or $\overline{RD}$ Low	5 + 3DT/8 + I		5 + 3DT/8 + I		ns
t_{WDE}	$\overline{WR}$ Low to Data Enabled	–1 + DT/16		–1 + DT/16		ns
t_{SADADC}	Address, Selects to ADRCLK High[2]	0 + DT/4		0 + DT/4		ns

W = (number of wait states specified in WAIT register) × t_{CK}.
H = t_{CK} (if an address hold cycle occurs, as specified in WAIT register; otherwise H = 0).
I = t_{CK} (if a bus idle cycle occurs, as specified in WAIT register; otherwise I = 0).

NOTES
[1]ACK Delay/Setup: User must meet t_{DAAK} or t_{DSAK} or synchronous specification t_{SACKC} for deassertion of ACK (Low), all three specifications must be met for assertion of ACK (High).
[2]The falling edge of $\overline{MS}$x, $\overline{SW}$, $\overline{BMS}$ is referenced.
[3]See *System Hold Time Calculation* under Test Conditions for calculation of hold times given capacitive and dc loads.

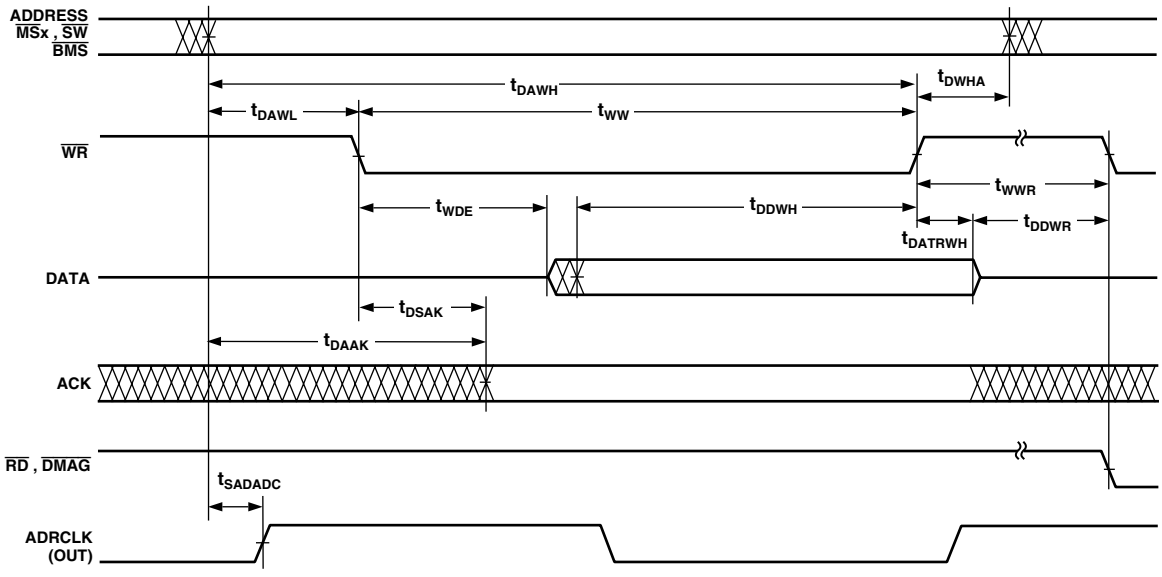


Figure 14. Memory Write—Bus Master

Synchronous Read/Write—Bus Master

Use these specifications for interfacing to external memory systems that require CLKIN—relative timing or for accessing a slave ADSP-2106x (in multiprocessor memory space). These synchronous switching characteristics are also valid during asynchronous memory reads and writes (see Memory Read—Bus Master and Memory Write—Bus Master).

When accessing a slave ADSP-2106x, these switching characteristics must meet the slave's timing requirements for synchronous read/writes (see Synchronous Read/Write—Bus Slave). The slave ADSP-2106x must also meet these (bus master) timing requirements for data and acknowledge setup and hold times.

Parameter		ADSP-21060C Min	ADSP-21060C Max	ADSP-21060LC Min	ADSP-21060LC Max	Unit
Timing Requirements:						
t_{SSDATI}	Data Setup before CLKIN	3 + DT/8		3 + DT/8		ns
t_{HSDATI}	Data Hold after CLKIN	3.5 – DT/8		3.5 – DT/8		ns
t_{DAAK}	ACK Delay after Address, $\overline{MS}$x, $\overline{SW}$, $\overline{BMS}$[1, 2]		14 + 7 DT/8 + W		14 + 7 DT/8 + W	ns
t_{SACKC}	ACK Setup before CLKIN[2]	6.5 + DT/4		6.5 + DT/4		ns
t_{HACK}	ACK Hold after CLKIN	–1 – DT/4		–1 – DT/4		ns
Switching Characteristics:						
t_{DADRO}	Address, $\overline{MS}$x, $\overline{BMS}$, $\overline{SW}$ Delay after CLKIN[1]		7 – DT/8		7 – DT/8	ns
t_{HADRO}	Address, $\overline{MS}$x, $\overline{BMS}$, $\overline{SW}$ Hold after CLKIN	–1 – DT/8		–1 – DT/8		ns
t_{DPGC}	PAGE Delay after CLKIN	9 + DT/8	16 + DT/8	9 + DT/8	16 + DT/8	ns
t_{DRDO}	$\overline{RD}$ High Delay after CLKIN	–2 – DT/8	4 – DT/8	–2 – DT/8	4 – DT/8	ns
t_{DWRO}	$\overline{WR}$ High Delay after CLKIN	–3 – 3DT/16	4 – 3DT/16	–3 – 3DT/16	4 – 3DT/16	ns
t_{DRWL}	$\overline{RD}$/$\overline{WR}$ Low Delay after CLKIN	8 + DT/4	12.5 + DT/4	8 + DT/4	12.5 + DT/4	ns
t_{SDDATO}	Data Delay after CLKIN		19 + 5DT/16		19.25 + 5DT/16	ns
t_{DATTR}	Data Disable after CLKIN[3]	0 – DT/8	7 – DT/8	0 – DT/8	7 – DT/8	ns
t_{DADCCK}	ADRCLK Delay after CLKIN	4 + DT/8	10 + DT/8	4 + DT/8	10 + DT/8	ns
t_{ADRCK}	ADRCLK Period	t_{CK}		t_{CK}		ns
t_{ADRCKH}	ADRCLK Width High	(t_{CK}/2 – 2)		(t_{CK}/2 – 2)		ns
t_{ADRCKL}	ADRCLK Width Low	(t_{CK}/2 – 2)		(t_{CK}/2 – 2)		ns

W = (number of Wait states specified in WAIT register) × t_{CK}.

NOTES

[1]The falling edge of $\overline{MS}$x, $\overline{SW}$, $\overline{BMS}$ is referenced.

[2]ACK Delay/Setup: User must meet t_{DAAK} or t_{DSAK} or synchronous specification t_{SACKC} for deassertion of ACK (Low), all three specifications must be met for assertion of ACK (High).

[3]See *System Hold Time Calculation* under Test Conditions for calculation of hold times given capacitive and dc loads.

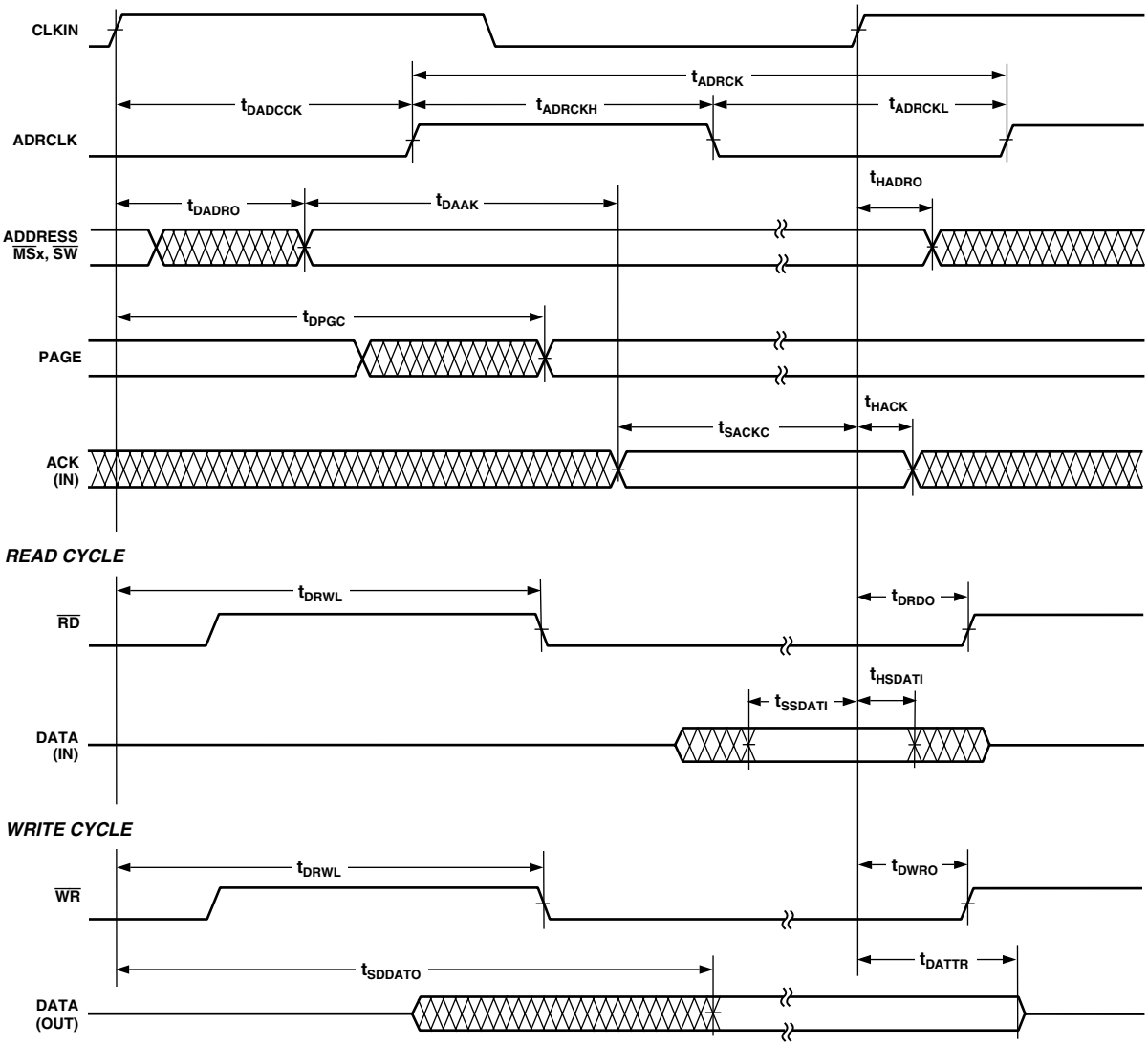


Figure 15. Synchronous Read/Write—Bus Master

Synchronous Read/Write—Bus Slave
Use these specifications for ADSP-2106x bus master accesses of a slave's IOP registers or internal memory (in multiprocessor memory space). The bus master must meet these (bus slave) timing requirements.

Parameter		ADSP-21060C Min	ADSP-21060C Max	ADSP-21060LC Min	ADSP-21060LC Max	Unit
Timing Requirements:						
t_{SADRI}	Address, $\overline{SW}$ Setup before CLKIN	15 + DT/2		15 + DT/2		ns
t_{HADRI}	Address, $\overline{SW}$ Hold before CLKIN		5 + DT/2		5 + DT/2	ns
t_{SRWLI}	$\overline{RD}$/$\overline{WR}$ Low Setup before CLKIN[1]	9.5 + 5DT/16		9.5 + 5DT/16		ns
t_{HRWLI}	$\overline{RD}$/$\overline{WR}$ Low Hold after CLKIN	–3.5 – 5DT/16	8 + 7DT/16	–3.75 – 5DT/16	8 + 7DT/16	ns
t_{RWHPI}	$\overline{RD}$/$\overline{WR}$ Pulse High	3		3		ns
t_{SDATWH}	Data Setup before $\overline{WR}$ High	5		5		ns
t_{HDATWH}	Data Hold after $\overline{WR}$ High	1		1		ns
Switching Characteristics:						
t_{SDDATO}	Data Delay after CLKIN		19 + 5DT/16		19.25 + 5DT/16	ns
t_{DATTR}	Data Disable after CLKIN[2]	0 – DT/8	7 – DT/8	0 – DT/8	7 – DT/8	ns
t_{DACKAD}	ACK Delay after Address, $\overline{SW}$[3]		9		9	ns
t_{ACKTR}	ACK Disable after CLKIN[3]	–1 – DT/8	6 – DT/8	–1 – DT/8	6 – DT/8	ns

NOTES
[1]t_{SRWLI} (min) = 9.5 + 5DT/16 when Multiprocessor Memory Space Wait State (MMSWS bit in WAIT register) is disabled; when MMSWS is enabled, t_{SRWLI} (min) = 4 + DT/8.
[2]See *System Hold Time Calculation* under Test Conditions for calculation of hold times given capacitive and dc loads.
[3]t_{DACKAD} is true only if the address and $\overline{SW}$ inputs have setup times (before CLKIN) greater than 10 + DT/8 and less than 19 + 3DT/4. If the address and $\overline{SW}$ inputs have setup times greater than 19 + 3DT/4, then ACK is valid 14 + DT/4 (max) after CLKIN. A slave that sees an address with an M field match will respond with ACK regardless of the state of MMSWS or strobes. A slave will three-state ACK every cycle with t_{ACKTR}.

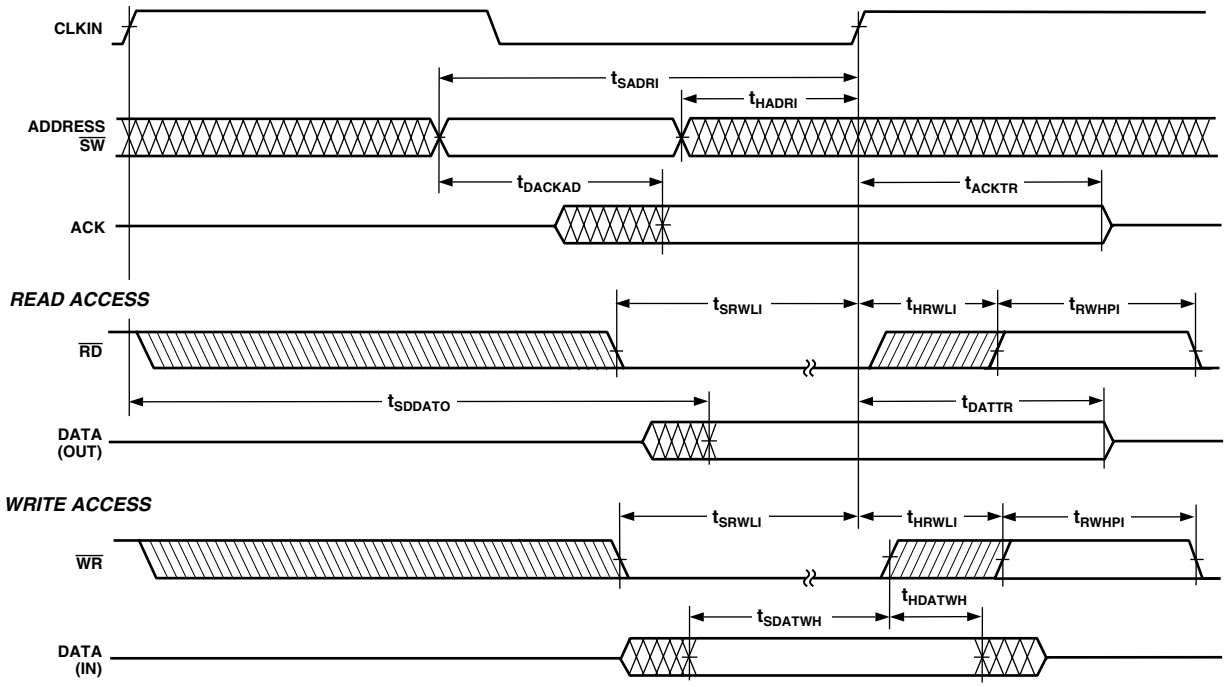


Figure 16. Synchronous Read/Write—Bus Slave

Multiprocessor Bus Request and Host Bus Request
Use these specifications for passing of bus mastership between multiprocessing ADSP-2106xs ($\overline{BR}$x) or a host processor ($\overline{HBR}$, $\overline{HBG}$).

Parameter		ADSP-21060C Min	ADSP-21060C Max	ADSP-21060LC Min	ADSP-21060LC Max	Unit
Timing Requirements:						
$t_{HBGRCSV}$	$\overline{HBG}$ Low to $\overline{RD}$/$\overline{WR}$/$\overline{CS}$ Valid[1]		20+ 5DT/4		20+ 5DT/4	ns
t_{SHBRI}	$\overline{HBR}$ Setup before CLKIN[2]	20 + 3DT/4		20 + 3DT/4		ns
t_{HHBRI}	$\overline{HBR}$ Hold before CLKIN[2]		14 + 3DT/4		14 + 3DT/4	ns
t_{SHBGI}	$\overline{HBG}$ Setup before CLKIN	13 + DT/2		13 + DT/2		ns
t_{HHBGI}	$\overline{HBG}$ Hold before CLKIN High		6 + DT/2		6 + DT/2	ns
t_{SBRI}	$\overline{BR}$x, $\overline{CPA}$ Setup before CLKIN[3]	13 + DT/2		13 + DT/2		ns
t_{HBRI}	$\overline{BR}$x, $\overline{CPA}$ Hold before CLKIN High		6 + DT/2		6 + DT/2	ns
t_{SRPBAI}	RPBA Setup before CLKIN	21 + 3DT/4		21 + 3DT/4		ns
t_{HRPBAI}	RPBA Hold before CLKIN		12 + 3DT/4		12 + 3DT/4	ns
Switching Characteristics:						
t_{DHBGO}	$\overline{HBG}$ Delay after CLKIN		7 – DT/8		7 – DT/8	ns
t_{HHBGO}	$\overline{HBG}$ Hold after CLKIN	–2 – DT/8		–2 – DT/8		ns
t_{DBRO}	$\overline{BR}$x Delay after CLKIN		7 – DT/8		7 – DT/8	ns
t_{HBRO}	$\overline{BR}$x Hold after CLKIN	–2 – DT/8		–2 – DT/8		ns
t_{DCPAO}	$\overline{CPA}$ Low Delay after CLKIN		8 – DT/8		8.5 – DT/8	ns
t_{TRCPA}	$\overline{CPA}$ Disable after CLKIN	–2 – DT/8	4.5 – DT/8	–2 – DT/8	4.5 – DT/8	ns
t_{DRDYCS}	REDY (O/D) or (A/D) Low from $\overline{CS}$ and $\overline{HBR}$ Low[4]		8.5		11.0	ns
t_{TRDYHG}	REDY (O/D) Disable or REDY (A/D) High from $\overline{HBG}$[4]	40 + 23DT/16		40 + 23DT/16		ns
t_{ARDYTR}	REDY (A/D) Disable from $\overline{CS}$ or $\overline{HBR}$ High[4]		10		10	ns

NOTES
[1]For first asynchronous access after $\overline{HBR}$ and $\overline{CS}$ asserted, $ADDR_{31-0}$ must be a non-MMS value 1/2 t_{CK} before $\overline{RD}$ or $\overline{WR}$ goes low or by $t_{HBGRCSV}$ after $\overline{HBG}$ goes low. This is easily accomplished by driving an upper address signal high when $\overline{HBG}$ is asserted. See the "Host Processor Control of the ADSP-2106x" section in the *ADSP-2106x SHARC User's Manual, Second Edition*.
[2]Only required for recognition in the current cycle.
[3]$\overline{CPA}$ assertion must meet the setup to CLKIN; deassertion does not need to meet the setup to CLKIN.
[4](O/D) = open drain, (A/D) = active drive.

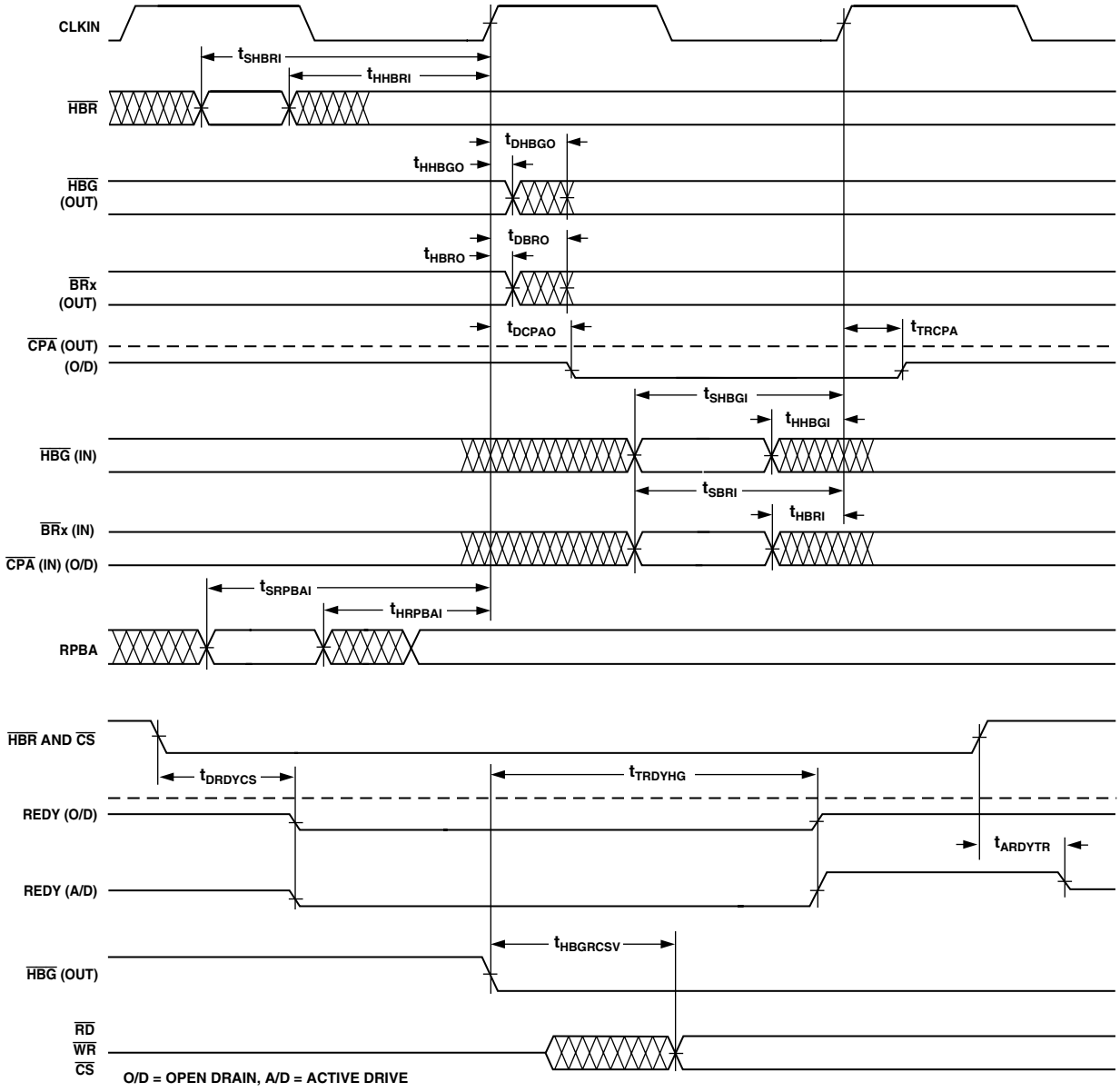


Figure 17. Multiprocessor Bus Request and Host Bus Request

Asynchronous Read/Write—Host to ADSP-2106x
Use these specifications for asynchronous host processor accesses of an ADSP-2106x, after the host has asserted $\overline{CS}$ and $\overline{HBR}$ (low). After $\overline{HBG}$ is returned by the ADSP-2106x, the host can drive the $\overline{RD}$ and $\overline{WR}$ pins to access the ADSP-2106x's internal memory or IOP registers. $\overline{HBR}$ and $\overline{HBG}$ are assumed low for this timing.

Parameter		ADSP-21060C Min	ADSP-21060C Max	ADSP-21060LC Min	ADSP-21060LC Max	Unit
Read Cycle						
Timing Requirements:						
t_{SADRDL}	Address Setup/$\overline{CS}$ Low before $\overline{RD}$ Low[1]	0		0		ns
t_{HADRDH}	Address Hold/$\overline{CS}$ Hold Low after $\overline{RD}$	0		0		ns
t_{WRWH}	$\overline{RD}$/$\overline{WR}$ High Width	6		6		ns
$t_{DRDHRDY}$	$\overline{RD}$ High Delay after REDY (O/D) Disable	0		0		ns
$t_{DRDHRDY}$	$\overline{RD}$ High Delay after REDY (A/D) Disable	0		0		ns
Switching Characteristics:						
$t_{SDATRDY}$	Data Valid before REDY Disable from Low	2		2		ns
$t_{DRDYRDL}$	REDY (O/D) or (A/D) Low Delay after $\overline{RD}$ Low		10		12.5	ns
t_{RDYPRD}	REDY (O/D) or (A/D) Low Pulsewidth for Read	45 + 21DT/16		45 + 21DT/16		ns
t_{HDARWH}	Data Disable after $\overline{RD}$ High	2	8	2	8.5	ns
Write Cycle						
Timing Requirements:						
t_{SCSWRL}	$\overline{CS}$ Low Setup before $\overline{WR}$ Low	0		0		ns
t_{HCSWRH}	$\overline{CS}$ Low Hold after $\overline{WR}$ High	0		0		ns
t_{SADWRH}	Address Setup before $\overline{WR}$ High	5		5		ns
t_{HADWRH}	Address Hold after $\overline{WR}$ High	2		2		ns
t_{WWRL}	$\overline{WR}$ Low Width	7		7		ns
t_{WRWH}	$\overline{RD}$/$\overline{WR}$ High Width	6		6		ns
$t_{DWRHRDY}$	$\overline{WR}$ High Delay after REDY (O/D) or (A/D) Disable	0		0		ns
t_{SDATWH}	Data Setup before $\overline{WR}$ High	5		5		ns
t_{HDATWH}	Data Hold after $\overline{WR}$ High	1		1		ns
Switching Characteristics:						
$t_{DRDYWRL}$	REDY (O/D) or (A/D) Low Delay after $\overline{WR}$/$\overline{CS}$ Low		10		12.5	ns
t_{RDYPWR}	REDY (O/D) or (A/D) Low Pulsewidth for Write	15 + 7DT/16		15 + 7DT/16		ns
t_{SRDYCK}	REDY (O/D) or (A/D) Disable to CLKIN	1 + 7DT/16	8 + 7DT/16	1 + 7DT/16	8 + 7DT/16	ns

NOTE
[1]Not required if $\overline{RD}$ and address are valid $t_{HBGRCSV}$ after $\overline{HBG}$ goes low. For first access after $\overline{HBR}$ asserted, $ADDR_{31-0}$ must be a non-MMS value 1/2 t_{CLK} before $\overline{RD}$ or $\overline{WR}$ goes low or by $t_{HBGRCSV}$ after HBG goes low. This is easily accomplished by driving an upper address signal high when $\overline{HBG}$ is asserted. See the "Host Processor Control of the ADSP-2106x" section in the *ADSP-2106x SHARC User's Manual, Second Edition.*

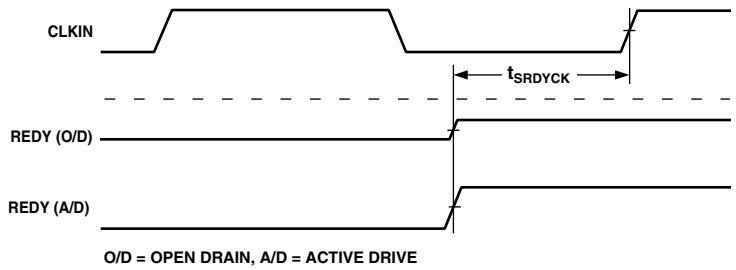


Figure 18a. Synchronous REDY Timing

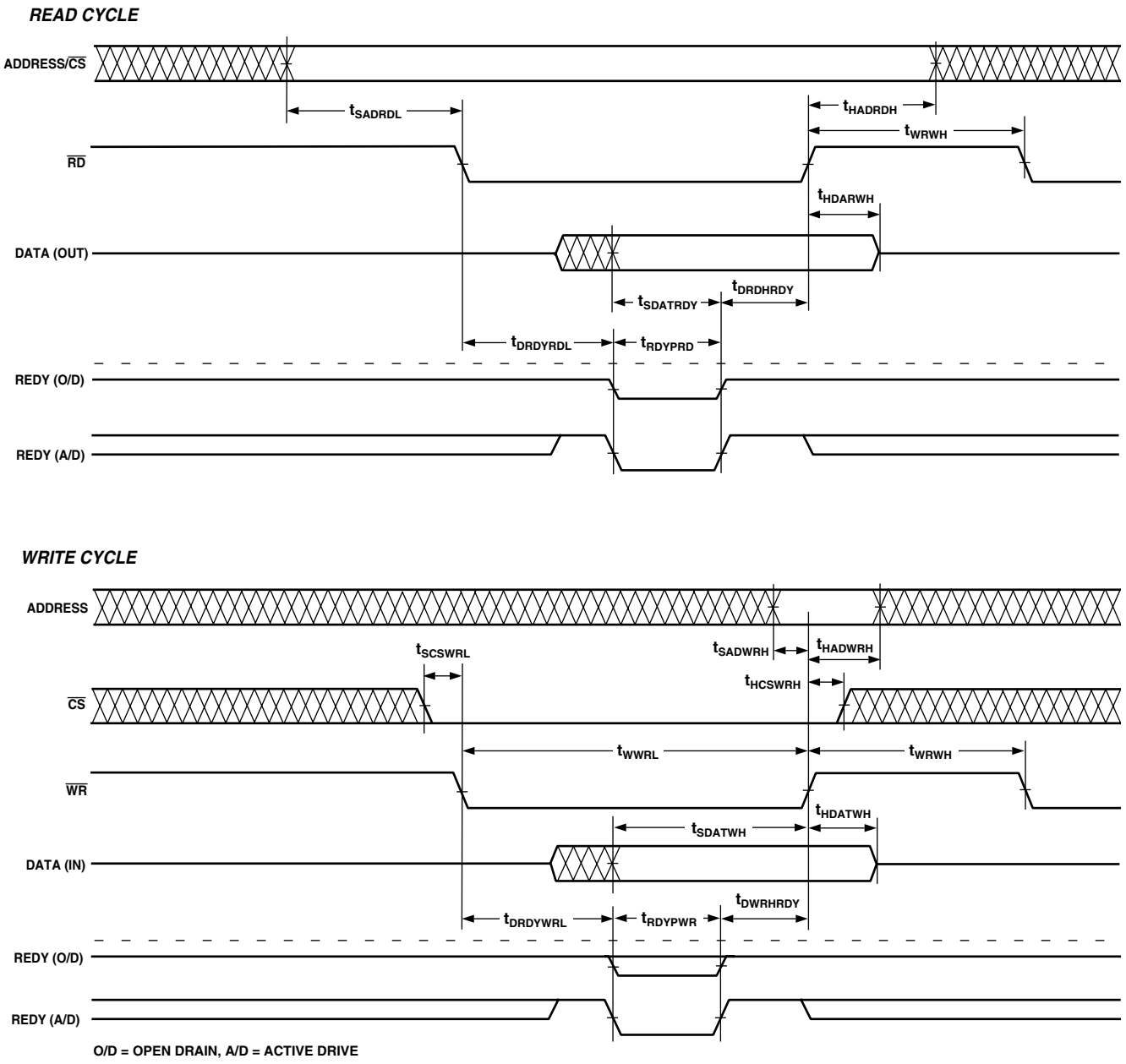


Figure 18b. Asynchronous Read/Write—Host to ADSP-2106x

Three-State Timing—Bus Master, Bus Slave, $\overline{\text{HBR}}$, $\overline{\text{SBTS}}$
These specifications show how the memory interface is disabled (stops driving) or enabled (resumes driving) relative to CLKIN and the $\overline{\text{SBTS}}$ pin. This timing is applicable to bus master transition cycles (BTC) and host transition cycles (HTC) as well as the $\overline{\text{SBTS}}$ pin.

Parameter		ADSP-21060C Min	ADSP-21060C Max	ADSP-21060LC Min	ADSP-21060LC Max	Unit
Timing Requirements:						
t_{STSCK}	$\overline{\text{SBTS}}$ Setup before CLKIN	12 + DT/2		12 + DT/2		ns
t_{HTSCK}	$\overline{\text{SBTS}}$ Hold before CLKIN		6 + DT/2		6 + DT/2	ns
Switching Characteristics:						
t_{MIENA}	Address/Select Enable after CLKIN	–1.5 – DT/8		–1.25 – DT/8		ns
t_{MIENS}	Strobes Enable after CLKIN[1]	–1.5 – DT/8		–1.5 – DT/8		ns
t_{MIENHG}	$\overline{\text{HBG}}$ Enable after CLKIN	–1.5 – DT/8		–1.5 – DT/8		ns
t_{MITRA}	Address/Select Disable after CLKIN		0 – DT/4		0.25 – DT/4	ns
t_{MITRS}	Strobes Disable after CLKIN[1]		1.5 – DT/4		1.5 – DT/4	ns
t_{MITRHG}	$\overline{\text{HBG}}$ Disable after CLKIN		2.0 – DT/4		2.0 – DT/4	ns
t_{DATEN}	Data Enable after CLKIN[2]	9 + 5DT/16		9 + 5DT/16		ns
t_{DATTR}	Data Disable after CLKIN[2]	0 – DT/8	7 – DT/8	0 – DT/8	7 – DT/8	ns
t_{ACKEN}	ACK Enable after CLKIN[2]	7.5 + DT/4		7.5 + DT/4		ns
t_{ACKTR}	ACK Disable after CLKIN[2]	–1 – DT/8	6 – DT/8	–1 – DT/8	6 – DT/8	ns
t_{ADCEN}	ADRCLK Enable after CLKIN	–2 – DT/8		–2 – DT/8		ns
t_{ADCTR}	ADRCLK Disable after CLKIN		8 – DT/4		8 – DT/4	ns
t_{MTRHBG}	Memory Interface Disable before $\overline{\text{HBG}}$ Low[3]	0 + DT/8		0 + DT/8		ns
t_{MENHBG}	Memory Interface Enable after $\overline{\text{HBG}}$ High[3]	19 + DT		19 + DT		ns

NOTES
[1]Strobes = $\overline{\text{RD}}$, $\overline{\text{WR}}$, $\overline{\text{SW}}$, PAGE, $\overline{\text{DMAG}}$.
[2]In addition to bus master transition cycles, these specs also apply to bus master and bus slave synchronous read/write.
[3]Memory Interface = Address, $\overline{\text{RD}}$, $\overline{\text{WR}}$, $\overline{\text{MS}}$x, $\overline{\text{SW}}$, $\overline{\text{HBG}}$, PAGE, $\overline{\text{DMAG}}$x, $\overline{\text{BMS}}$ (in EPROM boot mode).

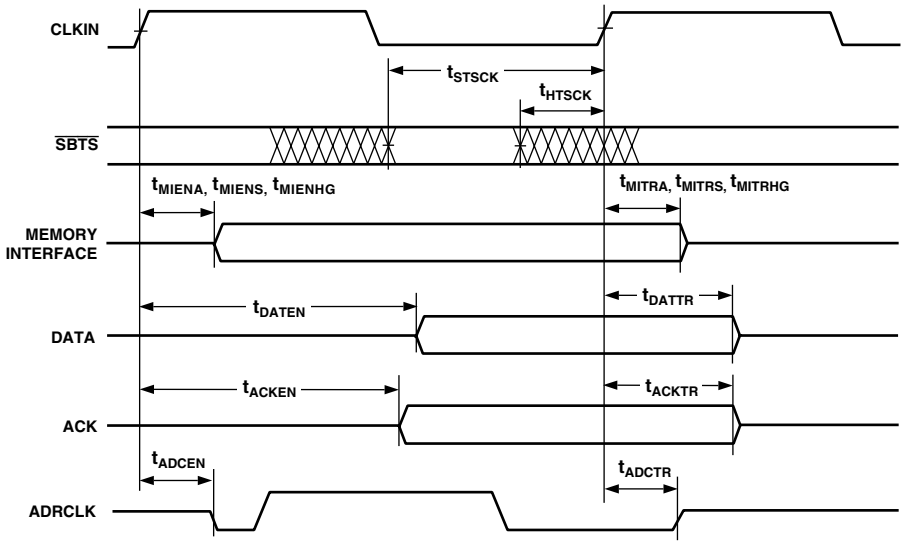


Figure 19a. Three-State Timing (Bus Transition Cycle, $\overline{\text{SBTS}}$ Assertion)

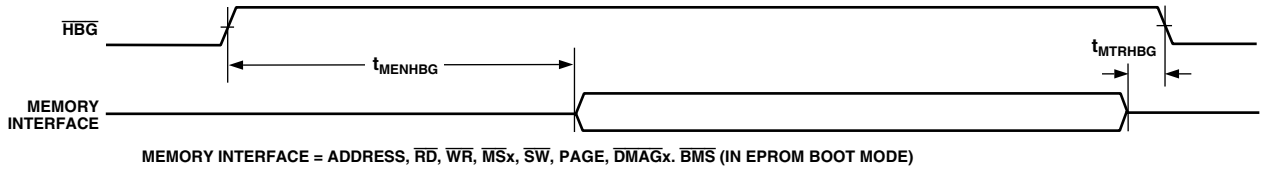


Figure 19b. Three-State Timing (Host Transition Cycle)

DMA Handshake

These specifications describe the three DMA handshake modes. In all three modes DMAR is used to initiate transfers. For handshake mode, DMAG controls the latching or enabling of data externally. For external handshake mode, the data transfer is controlled by the $ADDR_{31-0}$, $\overline{RD}$, $\overline{WR}$, $\overline{SW}$, PAGE, $\overline{MS}_{3-0}$, ACK, and $\overline{DMAG}$ signals. For Paced Master mode, the data transfer is controlled by $ADDR_{31-0}$, $\overline{RD}$, $\overline{WR}$, $\overline{MS}_{3-0}$, and ACK (not $\overline{DMAG}$). For Paced Master mode, the Memory Read–Bus Master, Memory Write–Bus Master, and Synchronous Read/Write–Bus Master timing specifications for $ADDR_{31-0}$, $\overline{RD}$, $\overline{WR}$, $\overline{MS}_{3-0}$, $\overline{SW}$, PAGE, $DATA_{47-0}$, and ACK also apply.

Parameter		ADSP-21060C Min	ADSP-21060C Max	ADSP-21060LC Min	ADSP-21060LC Max	Unit
Timing Requirements:						
t_{SDRLC}	$\overline{DMAR}$x Low Setup before CLKIN[1]	5		5		ns
t_{SDRHC}	$\overline{DMAR}$x High Setup before CLKIN[1]	5		5		ns
t_{WDR}	$\overline{DMAR}$x Width Low (Nonsynchronous)	6		6		ns
$t_{SDATDGL}$	Data Setup after $\overline{DMAG}$x Low[2]		10 + 5DT/8		10 + 5DT/8	ns
$t_{HDATIDG}$	Data Hold after $\overline{DMAG}$x High	2		2		ns
t_{DATDRH}	Data Valid after $\overline{DMAR}$x High[2]		16 + 7DT/8		16 + 7DT/8	ns
t_{DMARLL}	$\overline{DMAR}$x Low Edge to Low Edge	23 + 7DT/8		23 + 7DT/8		ns
t_{DMARH}	$\overline{DMAR}$x Width High	6		6		ns
Switching Characteristics:						
t_{DDGL}	$\overline{DMAG}$x Low Delay after CLKIN	9 + DT/4	15 + DT/4	9 + DT/4	15 + DT/4	ns
t_{WDGH}	$\overline{DMAG}$x High Width	6 + 3DT/8		6 + 3DT/8		ns
t_{WDGL}	$\overline{DMAG}$x Low Width	12 + 5DT/8		12 + 5DT/8		ns
t_{HDGC}	$\overline{DMAG}$x High Delay after CLKIN	–2 – DT/8	6 – DT/8	–2 – DT/8	6 – DT/8	ns
$t_{VDATDGH}$	Data Valid before $\overline{DMAG}$x High[3]	8 + 9DT/16		8 + 9DT/16		ns
$t_{DATRDGH}$	Data Disable after $\overline{DMAG}$x High[4]	0	7	0	7	ns
t_{DGWRL}	$\overline{WR}$ Low before $\overline{DMAG}$x Low	0	2	0	2	ns
t_{DGWRH}	$\overline{DMAG}$x Low before $\overline{WR}$ High	10 + 5DT/8 + W		10 + 5DT/8 + W		ns
t_{DGWRR}	$\overline{WR}$ High before $\overline{DMAG}$x High	1 + DT/16	3 + DT/16	1 + DT/16	3 + DT/16	ns
t_{DGRDL}	$\overline{RD}$ Low before $\overline{DMAG}$x Low	0	2	0	2	ns
t_{DRDGH}	$\overline{RD}$ Low before $\overline{DMAG}$x High	11 + 9DT/16 + W		11 + 9DT/16 + W		ns
t_{DGRDR}	$\overline{RD}$ High before $\overline{DMAG}$x High	0	3	0	3	ns
t_{DGWR}	$\overline{DMAG}$x High to $\overline{WR}$, $\overline{RD}$, $\overline{DMAG}$x Low	5 + 3DT/8 + HI		5 + 3DT/8 + HI		ns
t_{DADGH}	Address/Select Valid to $\overline{DMAG}$x High	17 + DT		17 + DT		ns
t_{DDGHA}	Address/Select Hold after $\overline{DMAG}$x High	–0.5		–0.5		ns

W = (number of wait states specified in WAIT register) × t_{CK}.
HI = t_{CK} (if an address hold cycle or bus idle cycle occurs, as specified in WAIT register; otherwise HI = 0).

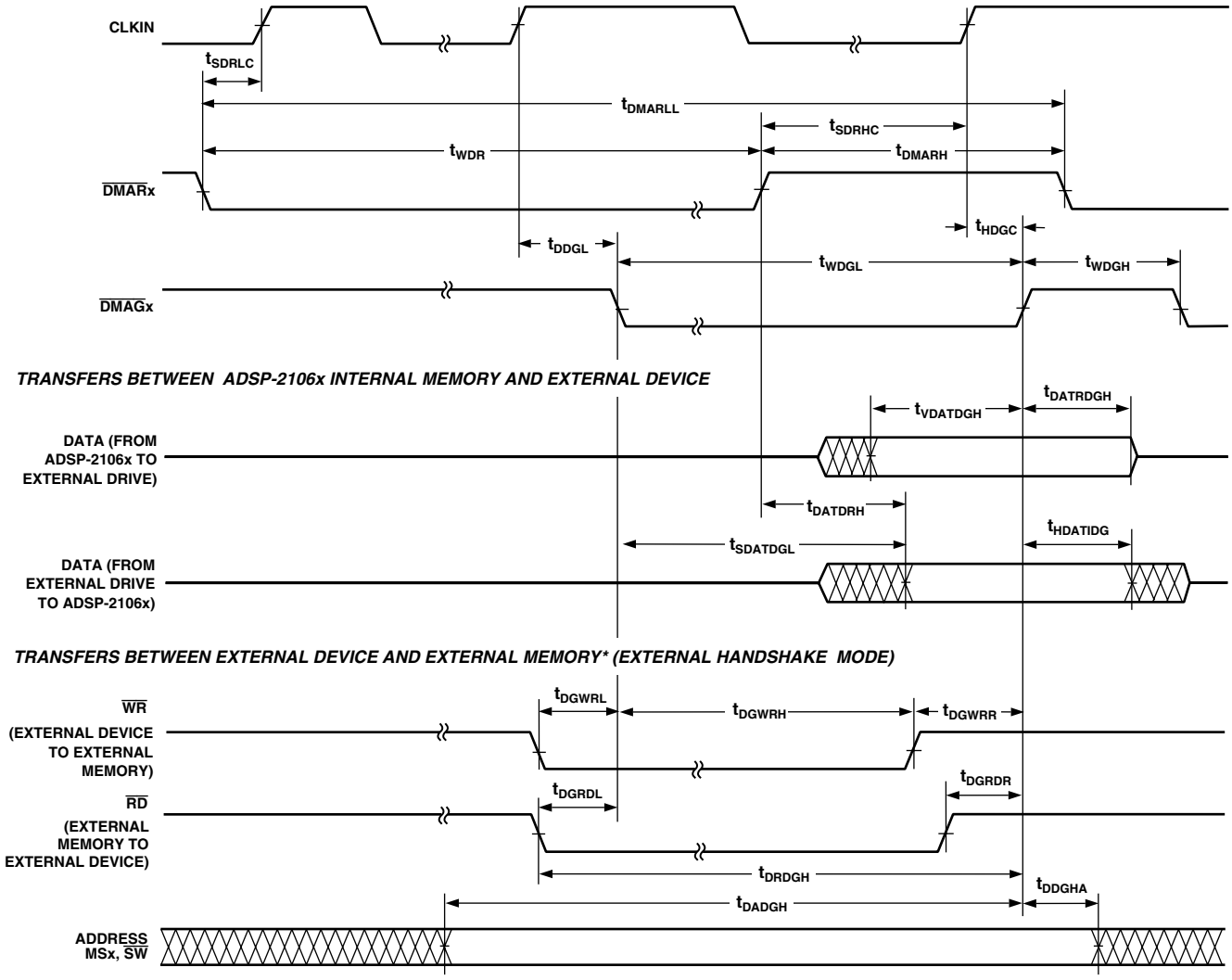
NOTES

[1]Only required for recognition in the current cycle.

[2]$t_{SDATDGL}$ is the data setup requirement if $\overline{DMAR}$x is not being used to hold off completion of a write. Otherwise, if $\overline{DMAR}$x low holds off completion of the write, the data can be driven t_{DATDRH} after $\overline{DMAR}$x is brought high.

[3]$t_{VDATDGH}$ is valid if $\overline{DMAR}$x is not being used to hold off completion of a read. If $\overline{DMAR}$x is used to prolong the read, then $t_{VDATDGH} = 8 + 9DT/16 + (n \times t_{CK})$ where *n* equals the number of extra cycles that the access is prolonged.

[4]See *System Hold Time Calculation* under Test Conditions for calculation of hold times given capacitive and dc loads.



* MEMORY READ – BUS MASTER, MEMORY WRITE – BUS MASTER, AND SYNCHRONOUS READ/WRITE – BUS MASTER TIMING SPECIFICATIONS FOR $ADDR_{31-0}$, $\overline{RD}$, $\overline{WR}$, $\overline{SW}$, $\overline{MS}_{3-0}$ AND ACK ALSO APPLY HERE.

Figure 20. DMA Handshake Timing

Link Ports: 1 × CLK Speed Operation

Parameter		ADSP-21060C Min	ADSP-21060C Max	ADSP-21060LC Min	ADSP-21060LC Max	Unit
Receive						
Timing Requirements:						
t_{SLDCL}	Data Setup before LCLK Low	3.5		3		ns
t_{HLDCL}	Data Hold after LCLK Low	3		3		ns
t_{LCLKIW}	LCLK Period (1 × Operation)	t_{CK}		t_{CK}		ns
$t_{LCLKRWL}$	LCLK Width Low	6		6		ns
$t_{LCLKRWH}$	LCLK Width High	5		5		ns
Switching Characteristics:						
t_{DLAHC}	LACK High Delay after CLKIN High	18 + DT/2	28.5 + DT/2	18 + DT/2	29.0 + DT/2	ns
t_{DLALC}	LACK Low Delay after LCLK High[1]	–3	13	–3	13	ns
t_{ENDLK}	LACK Enable from CLKIN	5 + DT/2		5 + DT/2		ns
t_{TDLK}	LACK Disable from CLKIN		20 + DT/2		20 + DT/2	ns
Transmit						
Timing Requirements:						
t_{SLACH}	LACK Setup before LCLK High	18		20		ns
t_{HLACH}	LACK Hold after LCLK High	–7		–7		ns
Switching Characteristics:						
t_{DLCLK}	LCLK Delay after CLKIN (1 × Operation)		15.5		16.75	ns
t_{DLDCH}	Data Delay after LCLK High		3		2.5	ns
t_{HLDCH}	Data Hold after LCLK High	–3		–3		ns
$t_{LCLKTWL}$	LCLK Width Low	$(t_{CK}/2) - 2$	$(t_{CK}/2) + 2$	$(t_{CK}/2) - 1$	$(t_{CK}/2) + 2.25$	ns
$t_{LCLKTWH}$	LCLK Width High	$(t_{CK}/2) - 2$	$(t_{CK}/2) + 2$	$(t_{CK}/2) - 2.25$	$(t_{CK}/2) + 1.0$	ns
t_{DLACLK}	LCLK Low Delay after LACK High	$(t_{CK}/2) + 8.5$	$(3 \times t_{CK}/2) + 17$	$(t_{CK}/2) + 8.0$	$(3 \times t_{CK}/2) + 18.5$	ns
t_{ENDLK}	LDAT, LCLK Enable after CLKIN	5 + DT/2		5 + DT/2		ns
t_{TDLK}	LDAT, LCLK Disable after CLKIN		20 + DT/2		20 + DT/2	ns
Link Port Service Request Interrupts: 1 × and 2 × Speed Operations						
Timing Requirements:						
t_{SLCK}	LACK/LCLK Setup before CLKIN Low[2]	10		10		ns
t_{HLCK}	LACK/LCLK Hold after CLKIN Low[2]	2		2		ns

NOTES
[1]LACK will go low with t_{DLALC} relative to rising edge of LCLK after first nibble is received. LACK will not go low if the receiver's link buffer is not about to fill.
[2]Only required for interrupt recognition in the current cycle.

Link Ports: 2 × CLK Speed Operation

Calculation of link receiver data setup and hold relative to link clock is required to determine the maximum allowable skew that can be introduced in the transmission path between LDATA and LCLK. Setup skew is the maximum delay that can be introduced in LDATA relative to LCLK, (setup skew = $t_{LCLKTWH}$ min – t_{DLDCH} – t_{SLDCL}). Hold skew is the maximum delay that can be introduced in LCLK relative to LDATA, (hold skew = $t_{LCLKTWL}$ min – t_{HLDCH} – t_{HLDCL}). Calculations made directly from 2 × speed specifications will result in unrealistically small skew times because they include multiple tester guardbands. The setup and hold skew times shown below are calculated to include only one tester guardband.

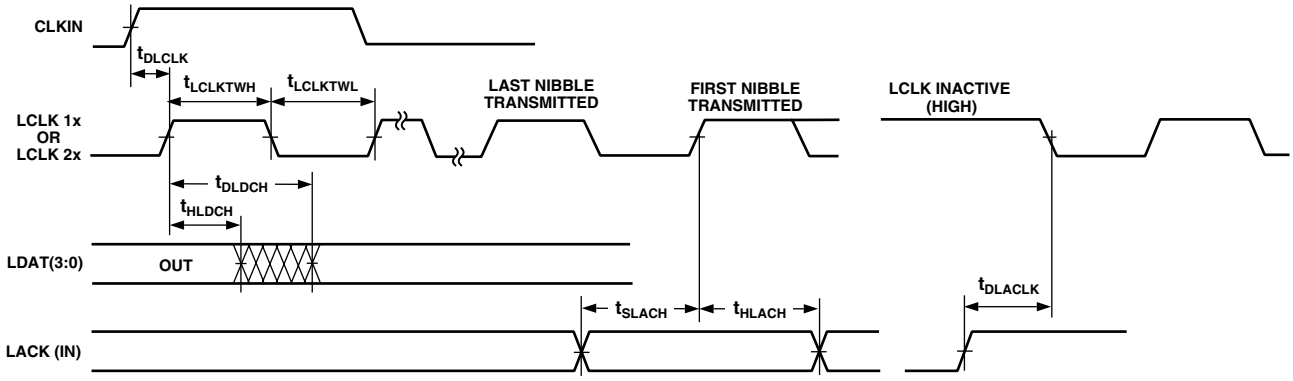
ADSP-21060C Setup Skew = 0.62 ns max (If port 2 is transmitter, setup skew is 0.39)
ADSP-21060C Hold Skew = 2.40 ns max

ADSP-21060LC Setup Skew = 1.23 ns max
ADSP-21060LC Hold Skew = 2.76 ns max

Parameter		ADSP-21060C Min	ADSP-21060C Max	ADSP-21060LC Min	ADSP-21060LC Max	Unit
Receive						
Timing Requirements:						
t_{SLDCL}	Data Setup before LCLK Low	2.5		2.25		ns
t_{HLDCL}	Data Hold after LCLK Low	2.25		2.25		ns
t_{LCLKIW}	LCLK Period (2 × Operation)	$t_{CK}/2$		$t_{CK}/2$		ns
$t_{LCLKRWL}$	LCLK Width Low	4.5		5.25		ns
$t_{LCLKRWH}$	LCLK Width High	4.25		4.5		ns
Switching Characteristics:						
t_{DLAHC}	LACK High Delay after CLKIN High	18 + DT/2	28.5 + DT/2	18 + DT/2	29.5 + DT/2	ns
t_{DLALC}	LACK Low Delay after LCLK High[1]	6	16.5	6	18.5	ns
Transmit						
Timing Requirements:						
t_{SLACH}	LACK Setup before LCLK High	19		19		ns
t_{HLACH}	LACK Hold after LCLK High	–6.75		–6.5		ns
Switching Characteristics:						
t_{DLCLK}	LCLK Delay after CLKIN		8		8	ns
t_{DLDCH}	Data Delay after LCLK High		2.5		2.25	ns
t_{HLDCH}	Data Hold after LCLK High	–2.0		–2.0		ns
$t_{LCLKTWL}$	LCLK Width Low	$(t_{CK}/4) – 1$	$(t_{CK}/4) + 1.5$	$(t_{CK}/4) – 0.75$	$(t_{CK}/4) + 1.5$	ns
$t_{LCLKTWH}$	LCLK Width High	$(t_{CK}/4) – 1.5$	$(t_{CK}/4) + 1$	$(t_{CK}/4) – 1.5$	$(t_{CK}/4) + 1$	ns
t_{DLACLK}	LCLK Low Delay after LACK High	$(t_{CK}/4) + 9$	$(3 * t_{CK}/4) + 16.5$	$(t_{CK}/4) + 9$	$(3 * t_{CK}/4) + 16.5$	ns

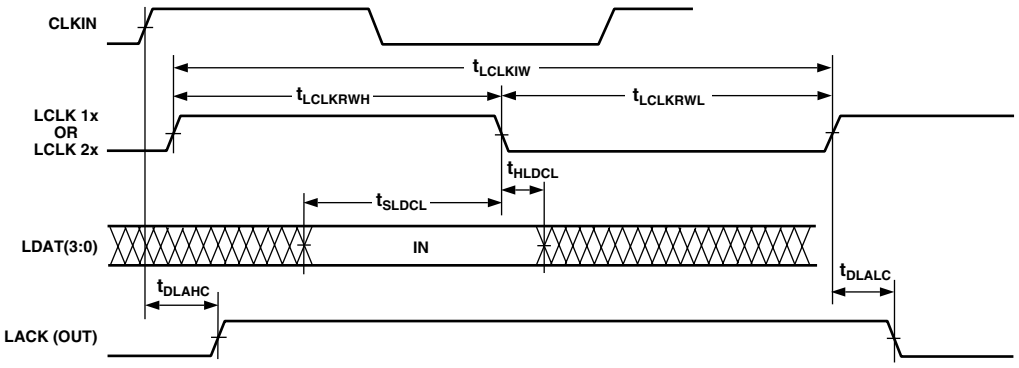
NOTE
[1]LACK will go low with t_{DLALC} relative to rising edge of LCLK after first nibble is received. LACK will not go low if the receiver's link buffer is not about to fill.

TRANSMIT

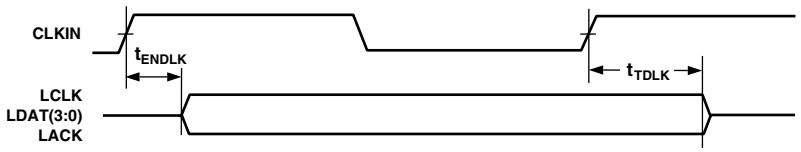


THE t_{SLACH} REQUIREMENT APPLIES TO THE RISING EDGE OF LCLK ONLY FOR THE FIRST NIBBLE TRANSMITTED.

RECEIVE



LINK PORT ENABLE/THREE-STATE DELAY FROM INSTRUCTION



LINK PORT ENABLE OR THREE-STATE TAKES EFFECT 2 CYCLES AFTER A WRITE TO A LINK PORT CONTROL REGISTER.

LINK PORT INTERRUPT SETUP TIME

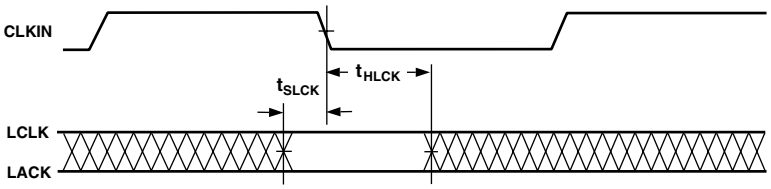


Figure 21. Link Ports

Serial Ports

Parameter		ADSP-21060C Min	ADSP-21060C Max	ADSP-21060LC Min	ADSP-21060LC Max	Unit
External Clock						
Timing Requirements:						
t_{SFSE}	TFS/RFS Setup before TCLK/RCLK[1]	3.5		3.5		ns
t_{HFSE}	TFS/RFS Hold after TCLK/RCLK[1, 2]	4		4		ns
t_{SDRE}	Receive Data Setup before RCLK[1]	1.5		1.5		ns
t_{HDRE}	Receive Data Hold after RCLK[1]	4		4		ns
t_{SCLKW}	TCLK/RCLK Width	9.5		9.5		ns
t_{SCLK}	TCLK/RCLK Period	t_{CK}		t_{CK}		ns
Internal Clock						
Timing Requirements:						
t_{SFSI}	TFS Setup before TCLK[1]; RFS Setup before RCLK[1]	8		8		ns
t_{HFSI}	TFS/RFS Hold after TCLK/RCLK[1, 2]	1		1		ns
t_{SDRI}	Receive Data Setup before RCLK[1]	3		3		ns
t_{HDRI}	Receive Data Hold after RCLK[1]	3		3		ns
External or Internal Clock						
Switching Characteristics:						
t_{DFSE}	RFS Delay after RCLK (Internally Generated RFS)[3]		13		13	ns
t_{HOFSE}	RFS Hold after RCLK (Internally Generated RFS)[3]	3		3		ns
External Clock						
Switching Characteristics:						
t_{DFSE}	TFS Delay after TCLK (Internally Generated TFS)[3]		13		13	ns
t_{HOFSE}	TFS Hold after TCLK (Internally Generated TFS)[3]	3		3		ns
t_{DDTE}	Transmit Data Delay after TCLK[3]		16		16	ns
t_{HODTE}	Transmit Data Hold after TCLK[3]	5		5		ns
Internal Clock						
Switching Characteristics:						
t_{DFSI}	TFS Delay after TCLK (Internally Generated TFS)[3]		4.5		4.5	ns
t_{HOFSI}	TFS Hold after TCLK (Internally Generated TFS)[3]	–1.5		–1.5		ns
t_{DDTI}	Transmit Data Delay after TCLK[3]		7.5		7.5	ns
t_{HDTI}	Transmit Data Hold after TCLK[3]	0		0		ns
t_{SCLKIW}	TCLK/RCLK Width	$(t_{SCLK}/2) - 2$	$(t_{SCLK}/2) + 2$	$(t_{SCLK}/2) - 2.5$	$(t_{SCLK}/2) + 2.5$	ns
Enable and Three-State						
Switching Characteristics:						
t_{DDTEN}	Data Enable from External TCLK[3]	3.5		4.0		ns
t_{DDTTE}	Data Disable from External TCLK[3]		10.5		10.5	ns
t_{DDTIN}	Data Enable from Internal TCLK[3]	0		0		ns
t_{DDTTI}	Data Disable from Internal TCLK[3]		3		3	ns
t_{DCLK}	TCLK/RCLK Delay from CLKIN		22 + 3DT/8		22 + 3DT/8	ns
t_{DPTR}	SPORT Disable after CLKIN		17		17	ns
Gated SCLK with External TFS (Mesh Multiprocessing)[4]						
Timing Requirements:						
t_{STFSCK}	TFS Setup before CLKIN	5		5		ns
t_{HTFSCK}	TFS Hold after CLKIN	$t_{CK}/2$		$t_{CK}/2$		ns
External Late Frame Sync						
Switching Characteristics:						
$t_{DDTLFSE}$	Data Delay from Late External TFS or External RFS with MCE = 1, MFD = 0[5]		12		12.8	ns
$t_{DDTENFS}$	Data Enable from late FS or MCE = 1, MFD = 0[5]	3		3.5		ns

To determine whether communication is possible between two devices at clock speed *n*, the following specifications must be confirmed: 1) frame sync delay & frame sync setup and hold, 2) data delay & data setup and hold, and 3) SCLK width.

NOTES
[1]Referenced to sample edge.
[2]RFS hold after RCK when MCE = 1, MFD = 0 is 0 ns minimum from drive edge. TFS hold after TCK for late external TFS is 0 ns minimum from drive edge.
[3]Referenced to drive edge.
[4]Applies only to gated serial clock mode used for serial port system I/O in mesh multiprocessing systems.
[5]MCE = 1, TFS enable and TFS valid follow $t_{DDTLFSE}$ and $t_{DDTENFS}$.

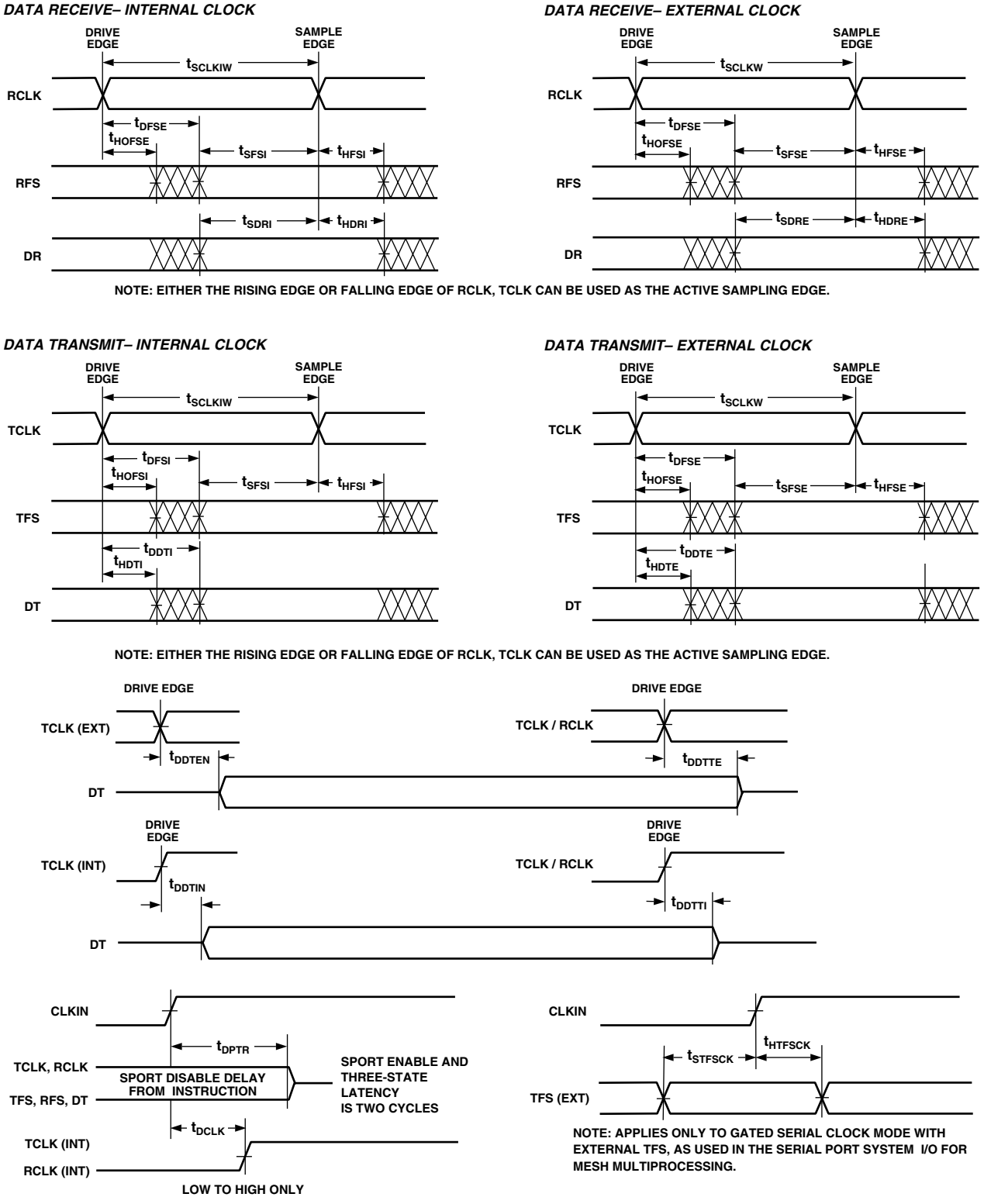
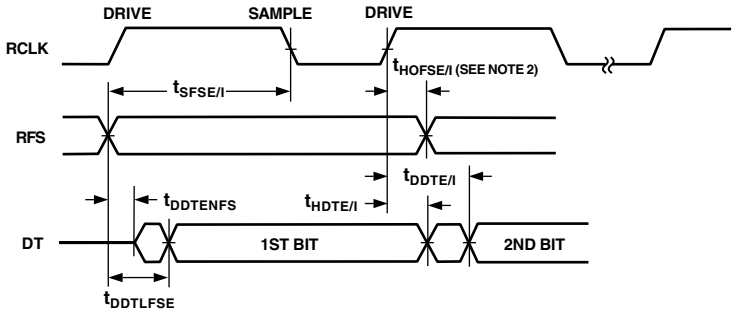


Figure 22. Serial Ports

EXTERNAL RFS with MCE = 1, MFD = 0



LATE EXTERNAL TFS

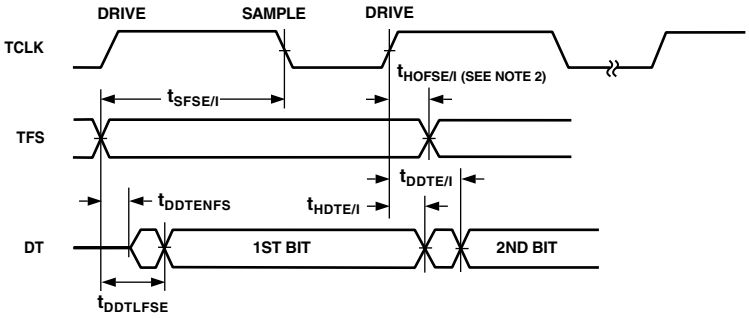


Figure 23. External Late Frame Sync

JTAG Test Access Port and Emulation

Parameter		ADSP-21060C Min	ADSP-21060C Max	ADSP-21060LC Min	ADSP-21060LC Max	Unit
Timing Requirements:						
t_{TCK}	TCK Period	t_{CK}		t_{CK}		ns
t_{STAP}	TDI, TMS Setup before TCK High	5		5		ns
t_{HTAP}	TDI, TMS Hold after TCK High	6		6		ns
t_{SSYS}	System Inputs Setup before TCK Low[1]	7		7		ns
t_{HSYS}	System Inputs Hold after TCK Low[1]	18		18.5		ns
t_{TRSTW}	$\overline{\text{TRST}}$ Pulsewidth	$4t_{CK}$		$4t_{CK}$		ns
Switching Characteristics:						
t_{DTDO}	TDO Delay from TCK Low		13		13	ns
t_{DSYS}	System Outputs Delay after TCK Low[2]		18.5		18.5	ns

NOTES
[1]System Inputs = $DATA_{47-0}$, $ADDR_{31-0}$, $\overline{RD}$, $\overline{WR}$, ACK, $\overline{SBTS}$, $\overline{SW}$, $\overline{HBR}$, $\overline{HBG}$, $\overline{CS}$, $\overline{DMAR1}$, $\overline{DMAR2}$, $\overline{BR}_{6-1}$, ID_{2-0}, RPBA, $\overline{IRQ}_{2-0}$, $FLAG_{3-0}$, DR0, DR1, TCLK0, TCLK1, RCLK0, RCLK1, TFS0, TFS1, RFS0, RFS1, $LxDAT_{3-0}$, LxCLK, LxACK, EBOOT, LBOOT, $\overline{BMS}$, CLKIN, $\overline{RESET}$.
[2]System Outputs = $DATA_{47-0}$, $ADDR_{31-0}$, $\overline{MS}_{3-0}$, $\overline{RD}$, $\overline{WR}$, ACK, PAGE, ADRCLK, $\overline{SW}$, $\overline{HBG}$, REDY, $\overline{DMAG1}$, $\overline{DMAG2}$, $\overline{BR}_{6-1}$, $\overline{CPA}$, $FLAG_{3-0}$, TIMEXP, DT0, DT1, TCLK0, TCLK1, RCLK0, RCLK1, TFS0, TFS1, RFS0, RFS1, $LxDAT_{3-0}$, LxCLK, LxACK, $\overline{BMS}$.

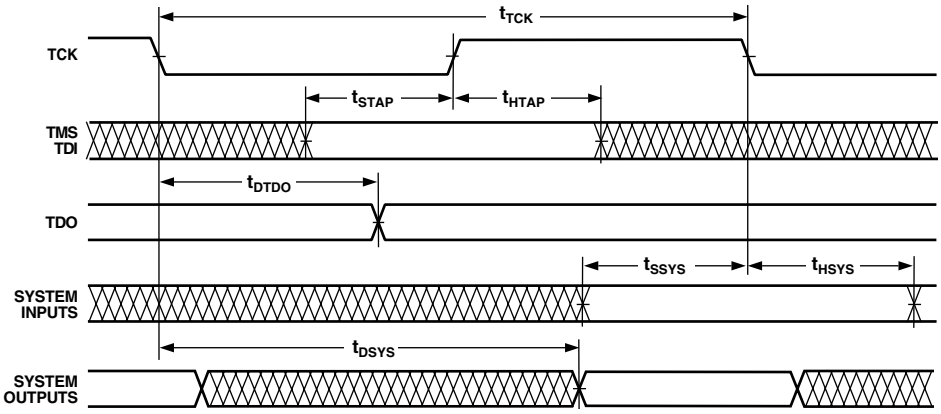


Figure 24. IEEE 11499.1 JTAG Test Access Port

OUTPUT DRIVE CURRENTS

Figure 28 shows typical I-V characteristics for the output drivers of the ADSP-2106x. The curves represent the current drive capability of the output drivers as a function of output voltage.

POWER DISSIPATION

Total power dissipation has two components, one due to internal circuitry and one due to the switching of external output drivers. Internal power dissipation is dependent on the instruction execution sequence and the data operands involved. Internal power dissipation is calculated in the following way:

$$P_{INT} = I_{DDIN} \times V_{DD}$$

The external component of total power dissipation is caused by the switching of output pins. Its magnitude depends on:

– the number of output pins that switch during each cycle (O)
– the maximum frequency at which they can switch (f)
– their load capacitance (C)
– their voltage swing (V_{DD})

and is calculated by:

$$P_{EXT} = O \times C \times V_{DD}^2 \times f$$

The load capacitance should include the processor's package capacitance (C_{IN}). The switching frequency includes driving the load high and then back low. Address and data pins can drive high and low at a maximum rate of $1/(2t_{CK})$. The write strobe can switch every cycle at a frequency of $1/t_{CK}$. Select pins switch at $1/(2t_{CK})$, but selects can switch on each cycle.

Example:

Estimate P_{EXT} with the following assumptions:

–A system with one bank of external data memory RAM (32-bit)
–Four 128K × 8 RAM chips are used, each with a load of 10 pF
–External data memory writes occur every other cycle, a rate of $1/(4t_{CK})$, with 50% of the pins switching
–The instruction cycle rate is 40 MHz (t_{CK} = 25 ns).

The P_{EXT} equation is calculated for each class of pins that can drive:

Table II. External Power Calculations (5 V Device)

Pin Type	# of Pins	% Switching	× C	× f	× V_{DD}^2	= P_{EXT}
Address	15	50	× 44.7 pF	× 10 MHz	× 25 V	= 0.084 W
$\overline{MS0}$	1	0	× 44.7 pF	× 10 MHz	× 25 V	= 0.000 W
$\overline{WR}$	1	–	× 44.7 pF	× 20 MHz	× 25 V	= 0.022 W
Data	32	50	× 14.7 pF	× 10 MHz	× 25 V	= 0.059 W
ADDRCLK	1	–	× 4.7 pF	× 20 MHz	× 25 V	= 0.002 W

P_{EXT} = 0.167 W

Table III. External Power Calculations (3.3 V Device)

Pin Type	# of Pins	% Switching	× C	× f	× V_{DD}^2	= P_{EXT}
Address	15	50	× 44.7 pF	× 10 MHz	× 10.9 V	= 0.037 W
$\overline{MS0}$	1	0	× 44.7 pF	× 10 MHz	× 10.9 V	= 0.000 W
$\overline{WR}$	1	–	× 44.7 pF	× 20 MHz	× 10.9 V	= 0.010 W
Data	32	50	× 14.7 pF	× 10 MHz	× 10.9 V	= 0.026 W
ADDRCLK	1	–	× 4.7 pF	× 20 MHz	× 10.9 V	= 0.001 W

P_{EXT} = 0.074 W

A typical power consumption can now be calculated for these conditions by adding a typical internal power dissipation:

$$P_{TOTAL} = P_{EXT} + (I_{DDIN2} \times 5.0\ V)$$

Note that the conditions causing a worst-case P_{EXT} are different from those causing a worst-case P_{INT}. Maximum P_{INT} cannot occur while 100% of the output pins are switching from all ones to all zeros. Note also that it is not common for an application to have 100% or even 50% of the outputs switching simultaneously.

TEST CONDITIONS

Output Disable Time

Output pins are considered to be disabled when they stop driving, go into a high impedance state, and start to decay from their output high or low voltage. The time for the voltage on the bus to decay by ΔV is dependent on the capacitive load, C_L and the load current, I_L. This decay time can be approximated by the following equation:

$$t_{DECAY} = \frac{C_L \Delta V}{I_L}$$

The output disable time t_{DIS} is the difference between $t_{MEASURED}$ and t_{DECAY} as shown in Figure 25. The time $t_{MEASURED}$ is the interval from when the reference signal switches to when the output voltage decays ΔV from the measured output high or output low voltage. t_{DECAY} is calculated with test loads C_L and I_L, and with ΔV equal to 0.5 V.

Output Enable Time

Output pins are considered to be enabled when they have made a transition from a high impedance state to when they start driving. The output enable time t_{ENA} is the interval from when a reference signal reaches a high or low voltage level to when the output has reached a specified high or low trip point, as shown in the Output Enable/Disable diagram (Figure 25). If multiple pins (such as the data bus) are enabled, the measurement value is that of the first pin to start driving.

Example System Hold Time Calculation

To determine the data output hold time in a particular system, first calculate t_{DECAY} using the equation given above. Choose ΔV to be the difference between the ADSP-2106x's output voltage and the input threshold for the device requiring the hold time. A typical ΔV will be 0.4 V. C_L is the total bus capacitance (per data line), and I_L is the total leakage or three-state current (per data line). The hold time will be t_{DECAY} plus the minimum disable time (i.e., t_{DATRWH} for the write cycle).

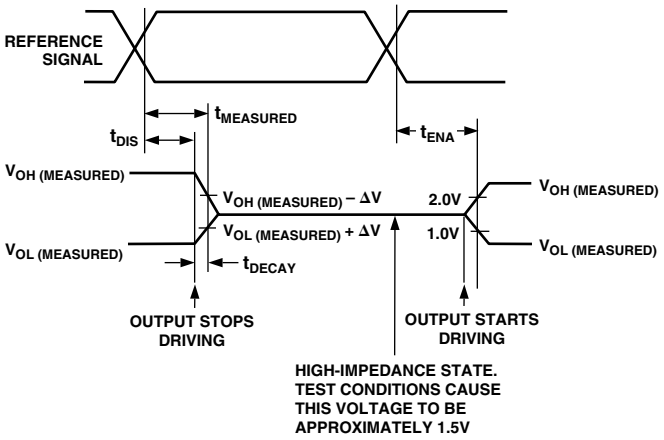


Figure 25. Output Enable/Disable

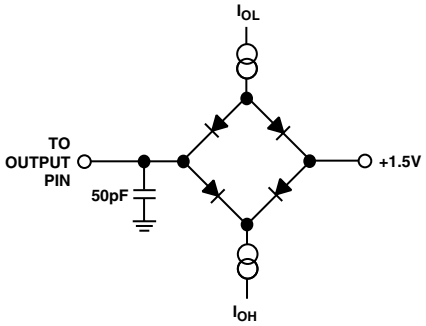


Figure 26. Equivalent Device Loading for AC Measurements (Includes All Fixtures)

Figure 27. Voltage Reference Levels for AC Measurements (Except Output Enable/Disable)

Capacitive Loading

Output delays and holds are based on standard capacitive loads: 50 pF on all pins (see Figure 26). The delay and hold specifications given should be derated by a factor of 1.5 ns/50 pF for loads other than the nominal value of 50 pF. Figures 29–30, 33–34 show how output rise time varies with capacitance. Figures 31, 35 show graphically how output delays and holds vary with load capacitance. (Note that this graph or derating does not apply to output disable delays; see the previous section *Output Disable Time* under Test Conditions.) The graphs of Figures 29, 30 and 31 may not be linear outside the ranges shown.

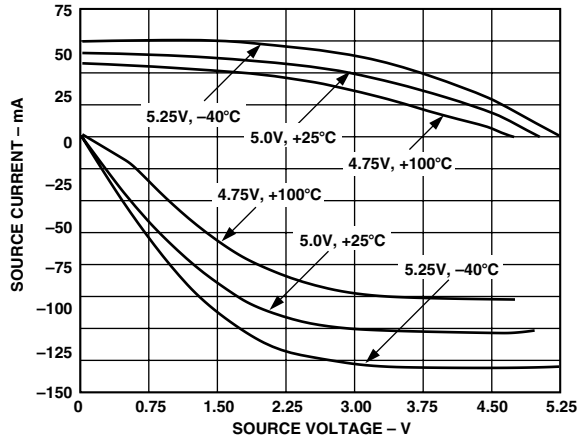


Figure 28. ADSP-2106x Typical Drive Currents (V_{DD} = 5 V)

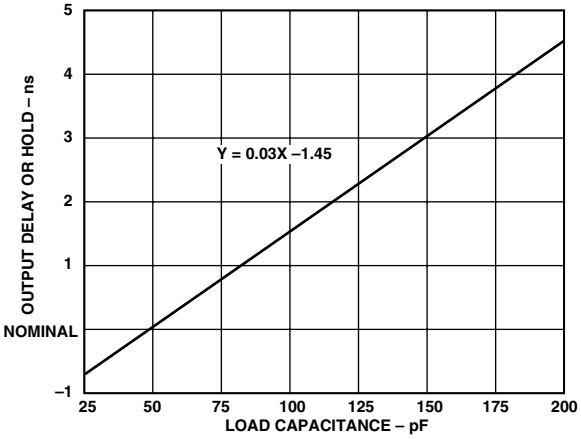


Figure 31. Typical Output Delay or Hold vs. Load Capacitance (at Maximum Case Temperature) (V_{DD} = 5 V)

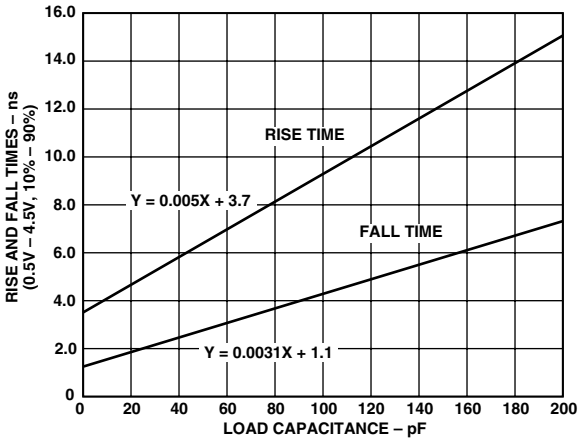


Figure 29. Typical Output Rise Time (10%–90% V_{DD}) vs. Load Capacitance (V_{DD} = 5 V)

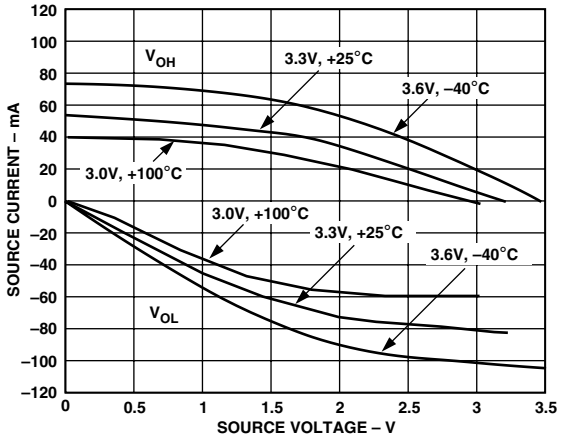


Figure 32. ADSP-2106x Typical Drive Currents (V_{DD} = 3.3 V)

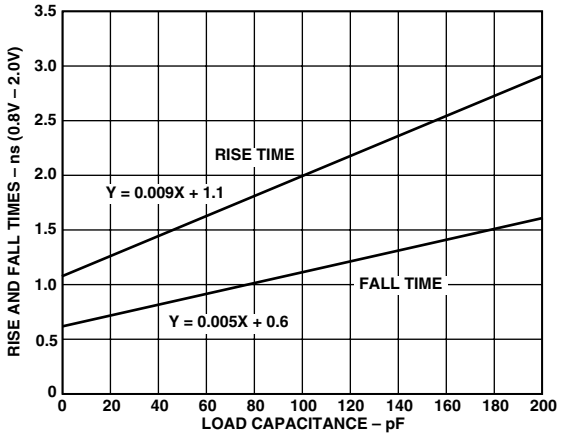


Figure 30. Typical Output Rise Time (0.8 V–2.0 V) vs. Load Capacitance (V_{DD} = 5 V)

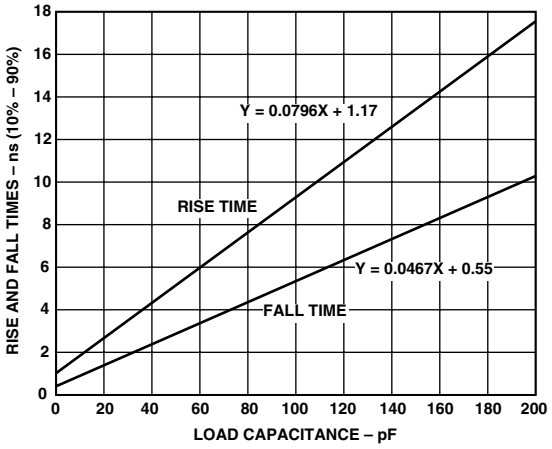


Figure 33. Typical Output Rise Time (10%–90% V_{DD}) vs. Load Capacitance (V_{DD} = 3.3 V)

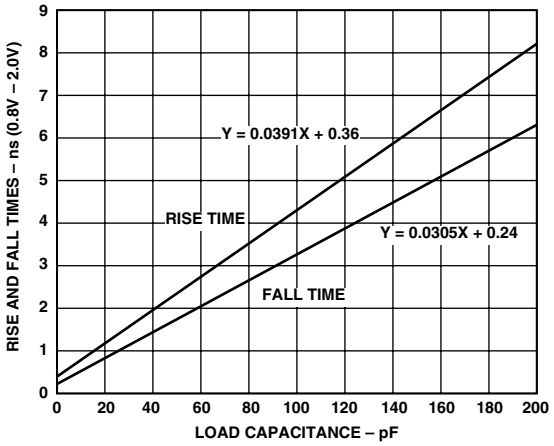


Figure 34. Typical Output Rise Time (0.8 V–2.0 V) vs. Load Capacitance (V_{DD} = 3.3 V)

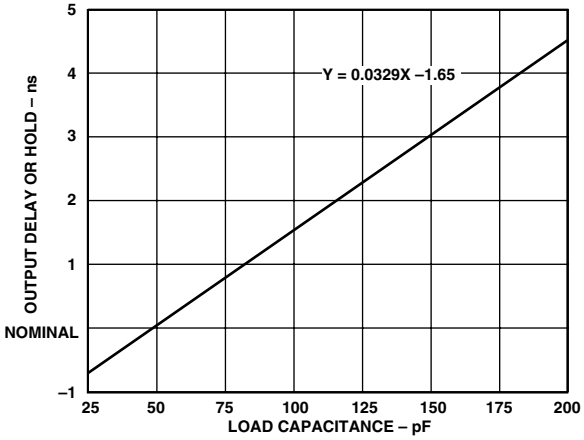


Figure 35. Typical Output Delay or Hold vs. Load Capacitance (at Maximum Case Temperature) (V_{DD} = 3.3 V)

ENVIRONMENTAL CONDITIONS

Thermal Characteristics

The ADSP-2106x is packaged in a 240-lead thermally enhanced ceramic QFP (CQFP). There are two package versions, one with a copper/tungsten heat slug on top of the package (CZ) for air cooling, and one with the heat slug on the bottom (CW) for cooling through the board. The ADSP-2106x is specified for a case temperature (T_{CASE}). To ensure that the T_{CASE} data sheet specification is not exceeded, a heatsink and/or an air flow source may be used. A heatsink should be attached with a thermal adhesive.

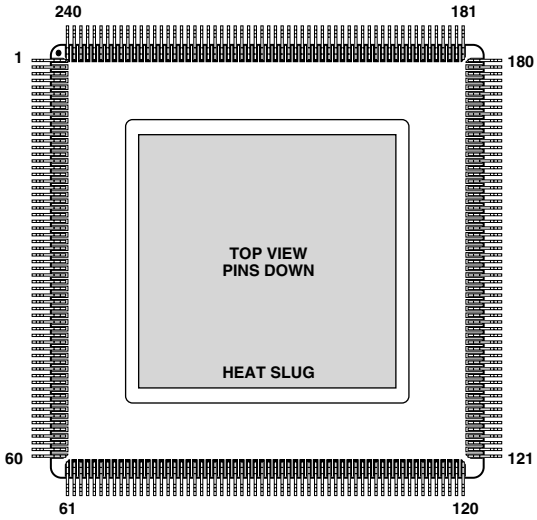
$$T_{CASE} = T_{AMB} + (PD \times \theta_{CA})$$

T_{CASE} = Case temperature (measured on the heat slug surface)
PD = Power dissipation in W (this value depends upon the specific application; a method for calculating PD is shown under Power Dissipation).
θ_{CA} = Value from the following table.

Airflow (Linear Ft./Min.)		**0**	**100**	**200**	**400**	**600**
θ_{CA} (°C/W)	21060CW/LCW	19.5	16	14	12	10
	21060CZ/LCZ	20	16	14	11.5	9.5

NOTES
This represents thermal resistance at total power of 5 W. With air flow, no variance is seen in θ_{CA} of 5 W.
θ_{CA} at 0 LFM varies with power
21060CW/LCW: at 2 W, θ_{CA} = 23°C/W; at 3 W, θ_{CA} = 21.5°C/W.
21060CZ/LCZ: at 2 W, θ_{CA} = 24°C/W; at 3 W, θ_{CA} = 21.5°C/W.
θ_{JC}= 0.24°C/W.

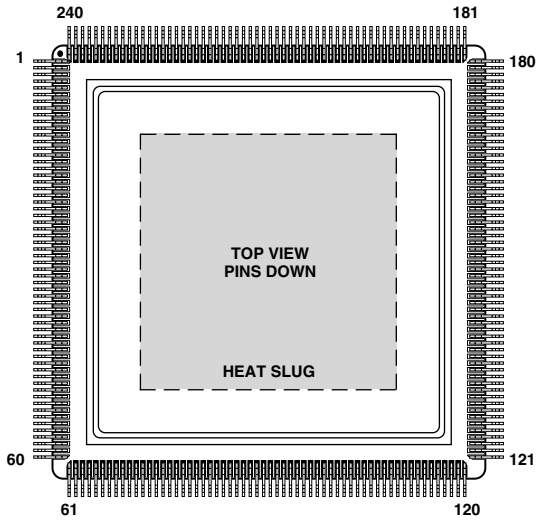
240-LEAD METRIC CQFP PIN CONFIGURATION
HEAT SLUG UP VERSION (CZ)



THE 240–LEAD PACKAGE CONTAINS A COPPER/TUNGSTEN HEAT SLUG ON ITS TOP SURFACE. HEAT SLUG AND PACKAGE LID ARE ELECTRICALLY ISOLATED.

Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name
1	TDI	41	ADDR20	81	TCLK0	121	DATA41	161	DATA14	201	L2DAT0
2	TRST	42	ADDR21	82	TFS0	122	DATA40	162	DATA13	202	L2CLK
3	VDD	43	GND	83	DR0	123	DATA39	163	DATA12	203	L2ACK
4	TDO	44	ADDR22	84	RCLK0	124	VDD	164	GND	204	NC
5	TIMEXP	45	ADDR23	85	RFS0	125	DATA38	165	DATA11	205	VDD
6	EMU	46	ADDR24	86	VDD	126	DATA37	166	DATA10	206	L3DAT3
7	ICSA	47	VDD	87	VDD	127	DATA36	167	DATA9	207	L3DAT2
8	FLAG3	48	GND	88	GND	128	GND	168	VDD	208	L3DAT1
9	FLAG2	49	VDD	89	ADRCLK	129	NC	169	DATA8	209	L3DAT0
10	FLAG1	50	ADDR25	90	REDY	130	DATA35	170	DATA7	210	L3CLK
11	FLAG0	51	ADDR26	91	HBG	131	DATA34	171	DATA6	211	L3ACK
12	GND	52	ADDR27	92	CS	132	DATA33	172	GND	212	GND
13	ADDR0	53	GND	93	RD	133	VDD	173	DATA5	213	L4DAT3
14	ADDR1	54	MS3	94	WR	134	VDD	174	DATA4	214	L4DAT2
15	VDD	55	MS2	95	GND	135	GND	175	DATA3	215	L4DAT1
16	ADDR2	56	MS1	96	VDD	136	DATA32	176	VDD	216	L4DAT0
17	ADDR3	57	MS0	97	GND	137	DATA31	177	DATA2	217	L4CLK
18	ADDR4	58	SW	98	CLKIN	138	DATA30	178	DATA1	218	L4ACK
19	GND	59	BMS	99	ACK	139	GND	179	DATA0	219	VDD
20	ADDR5	60	ADDR28	100	DMAG2	140	DATA29	180	GND	220	GND
21	ADDR6	61	GND	101	DMAG1	141	DATA28	181	GND	221	VDD
22	ADDR7	62	VDD	102	PAGE	142	DATA27	182	L0DAT3	222	L5DAT3
23	VDD	63	VDD	103	VDD	143	VDD	183	L0DAT2	223	L5DAT2
24	ADDR8	64	ADDR29	104	BR6	144	VDD	184	L0DAT1	224	L5DAT1
25	ADDR9	65	ADDR30	105	BR5	145	DATA26	185	L0DAT0	225	L5DAT0
26	ADDR10	66	ADDR31	106	BR4	146	DATA25	186	L0CLK	226	L5CLK
27	GND	67	GND	107	BR3	147	DATA24	187	L0ACK	227	L5ACK
28	ADDR11	68	SBTS	108	BR2	148	GND	188	VDD	228	GND
29	ADDR12	69	DMAR2	109	BR1	149	DATA23	189	L1DAT3	229	ID2
30	ADDR13	70	DMAR1	110	GND	150	DATA22	190	L1DAT2	230	ID1
31	VDD	71	HBR	111	VDD	151	DATA21	191	L1DAT1	231	ID0
32	ADDR14	72	DT1	112	GND	152	VDD	192	L1DAT0	232	LBOOT
33	ADDR15	73	TCLK1	113	DATA47	153	DATA20	193	L1CLK	233	RPBA
34	GND	74	TFS1	114	DATA46	154	DATA19	194	L1ACK	234	RESET
35	ADDR16	75	DR1	115	DATA45	155	DATA18	195	GND	235	EBOOT
36	ADDR17	76	RCLK1	116	VDD	156	GND	196	GND	236	IRQ2
37	ADDR18	77	RFS1	117	DATA44	157	DATA17	197	VDD	237	IRQ1
38	VDD	78	GND	118	DATA43	158	DATA16	198	L2DAT3	238	IRQ0
39	VDD	79	CPA	119	DATA42	159	DATA15	199	L2DAT2	239	TCK
40	ADDR19	80	DT0	120	GND	160	VDD	200	L2DAT1	240	TMS

240-LEAD METRIC CQFP PIN CONFIGURATION
HEAT SLUG DOWN VERSION (CW)



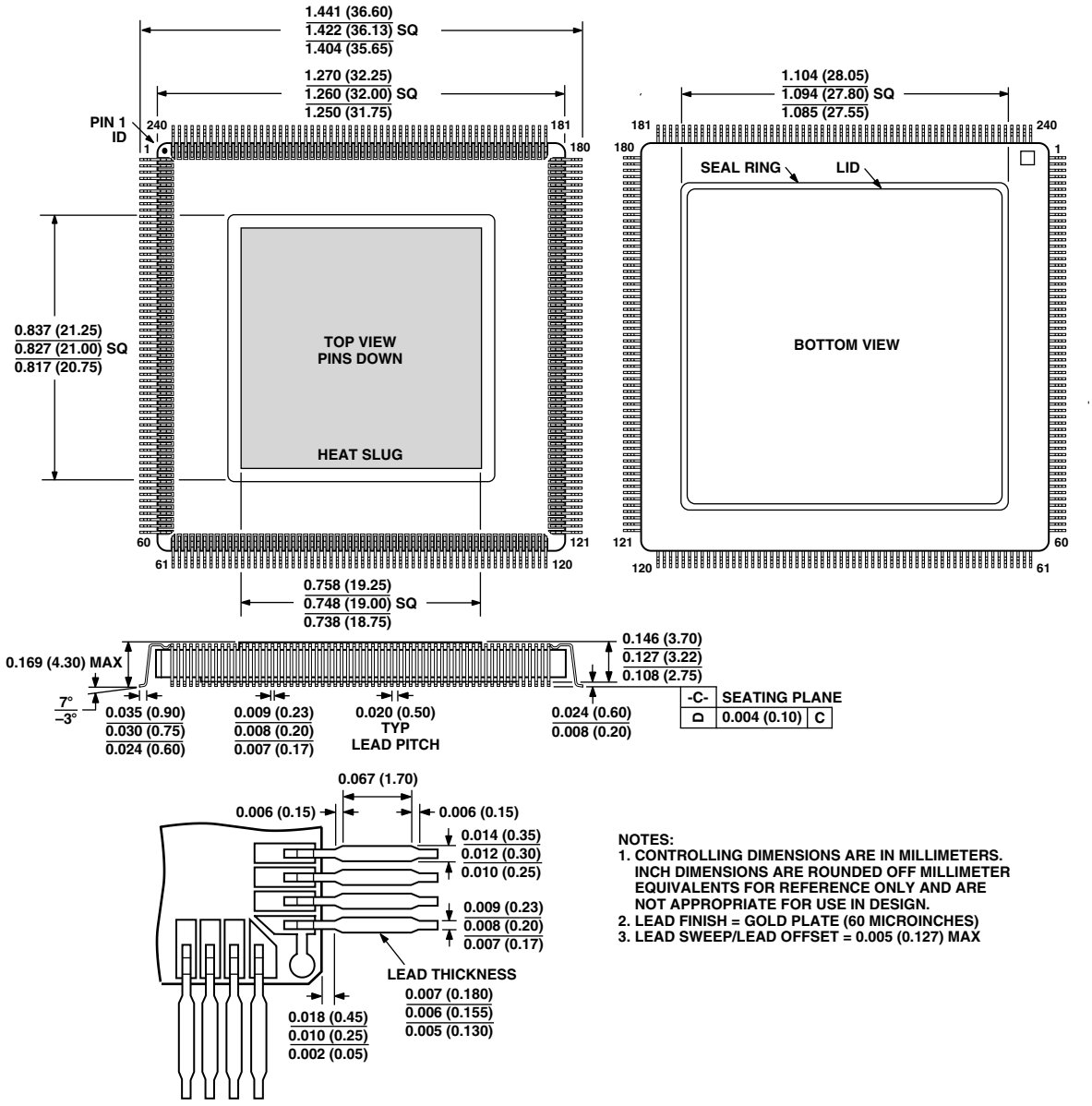
THE 240–LEAD PACKAGE CONTAINS A COPPER/TUNGSTEN HEAT SLUG ON ITS BOTTOM SURFACE. HEAT SLUG AND PACKAGE LID ARE ELECTRICALLY ISOLATED.

Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name
1	GND	41	DATA29	81	DMAG2	121	ADDR28	161	ADDR5	201	GND
2	DATA0	42	GND	82	ACK	122	BMS	162	GND	202	VDD
3	DATA1	43	DATA30	83	CLKIN	123	SW	163	ADDR4	203	L4ACK
4	DATA2	44	DATA31	84	GND	124	MS0	164	ADDR3	204	L4CLK
5	VDD	45	DATA32	85	VDD	125	MS1	165	ADDR2	205	L4DAT0
6	DATA3	46	GND	86	GND	126	MS2	166	VDD	206	L4DAT1
7	DATA4	47	VDD	87	WR	127	MS3	167	ADDR1	207	L4DAT2
8	DATA5	48	VDD	88	RD	128	GND	168	ADDR0	208	L4DAT3
9	GND	49	DATA33	89	CS	129	ADDR27	169	GND	209	GND
10	DATA6	50	DATA34	90	HBG	130	ADDR26	170	FLAG0	210	L3ACK
11	DATA7	51	DATA35	91	REDY	131	ADDR25	171	FLAG1	211	L3CLK
12	DATA8	52	NC	92	ADRCLK	132	VDD	172	FLAG2	212	L3DAT0
13	VDD	53	GND	93	GND	133	GND	173	FLAG3	213	L3DAT1
14	DATA9	54	DATA36	94	VDD	134	VDD	174	ICSA	214	L3DAT2
15	DATA10	55	DATA37	95	VDD	135	ADDR24	175	EMU	215	L3DAT3
16	DATA11	56	DATA38	96	RFS0	136	ADDR23	176	TIMEXP	216	VDD
17	GND	57	VDD	97	RCLK0	137	ADDR22	177	TDO	217	NC
18	DATA12	58	DATA39	98	DR0	138	GND	178	VDD	218	L2ACK
19	DATA13	59	DATA40	99	TFS0	139	ADDR21	179	TRST	219	L2CLK
20	DATA14	60	DATA41	100	TCLK0	140	ADDR20	180	TDI	220	L2DAT0
21	VDD	61	GND	101	DT0	141	ADDR19	181	TMS	221	L2DAT1
22	DATA15	62	DATA42	102	CPA	142	VDD	182	TCK	222	L2DAT2
23	DATA16	63	DATA43	103	GND	143	VDD	183	IRQ0	223	L2DAT3
24	DATA17	64	DATA44	104	RFS1	144	ADDR18	184	IRQ1	224	VDD
25	GND	65	VDD	105	RCLK1	145	ADDR17	185	IRQ2	225	GND
26	DATA18	66	DATA45	106	DR1	146	ADDR16	186	EBOOT	226	GND
27	DATA19	67	DATA46	107	TFS1	147	GND	187	RESET	227	L1ACK
28	DATA20	68	DATA47	108	TCLK1	148	ADDR15	188	RPBA	228	L1CLK
29	VDD	69	GND	109	DT1	149	ADDR14	189	LBOOT	229	L1DAT0
30	DATA21	70	VDD	110	HBR	150	VDD	190	ID0	230	L1DAT1
31	DATA22	71	GND	111	DMAR1	151	ADDR13	191	ID1	231	L1DAT2
32	DATA23	72	BR1	112	DMAR2	152	ADDR12	192	ID2	232	L1DAT3
33	GND	73	BR2	113	SBTS	153	ADDR11	193	GND	233	VDD
34	DATA24	74	BR3	114	GND	154	GND	194	L5ACK	234	L0ACK
35	DATA25	75	BR4	115	ADDR31	155	ADDR10	195	L5CLK	235	L0CLK
36	DATA26	76	BR5	116	ADDR30	156	ADDR9	196	L5DAT0	236	L0DAT0
37	VDD	77	BR6	117	ADDR29	157	ADDR8	197	L5DAT1	237	L0DAT1
38	VDD	78	VDD	118	VDD	158	VDD	198	L5DAT2	238	L0DAT2
39	DATA27	79	PAGE	119	VDD	159	ADDR7	199	L5DAT3	239	L0DAT3
40	DATA28	80	DMAG1	120	GND	160	ADDR6	200	VDD	240	GND

OUTLINE DIMENSIONS

Dimensions shown in inches and (millimeters within parentheses).

240-Lead CQFP with Heat Slug Up and Formed Leads (QS-240)

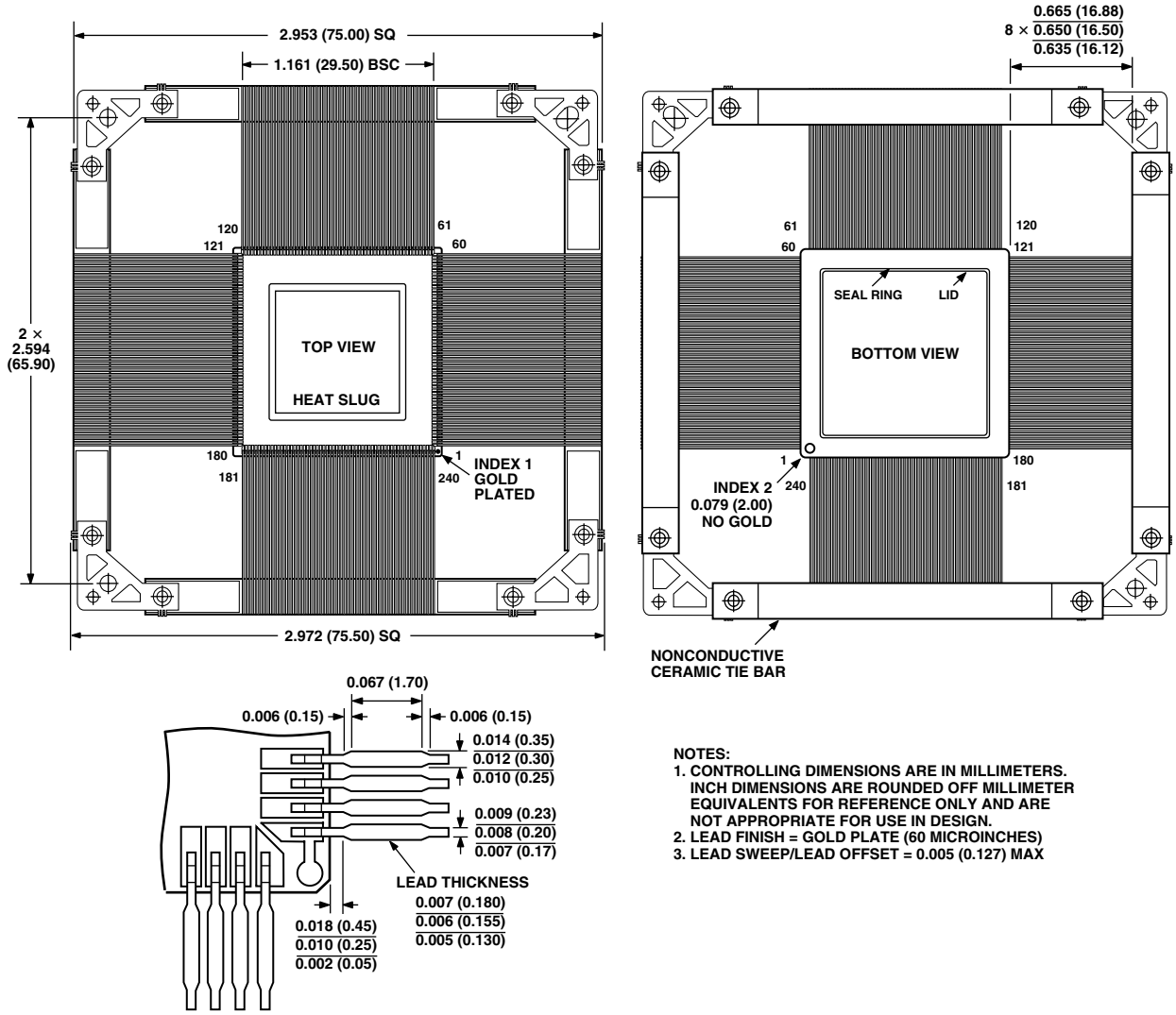


NOTES:
1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS. INCH DIMENSIONS ARE ROUNDED OFF MILLIMETER EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.
2. LEAD FINISH = GOLD PLATE (60 MICROINCHES)
3. LEAD SWEEP/LEAD OFFSET = 0.005 (0.127) MAX

OUTLINE DIMENSIONS

Dimensions shown in inches and (millimeters within parentheses).

240-Lead Metric CQFP with Heat Slug Up and Unformed Leads (QS-240)



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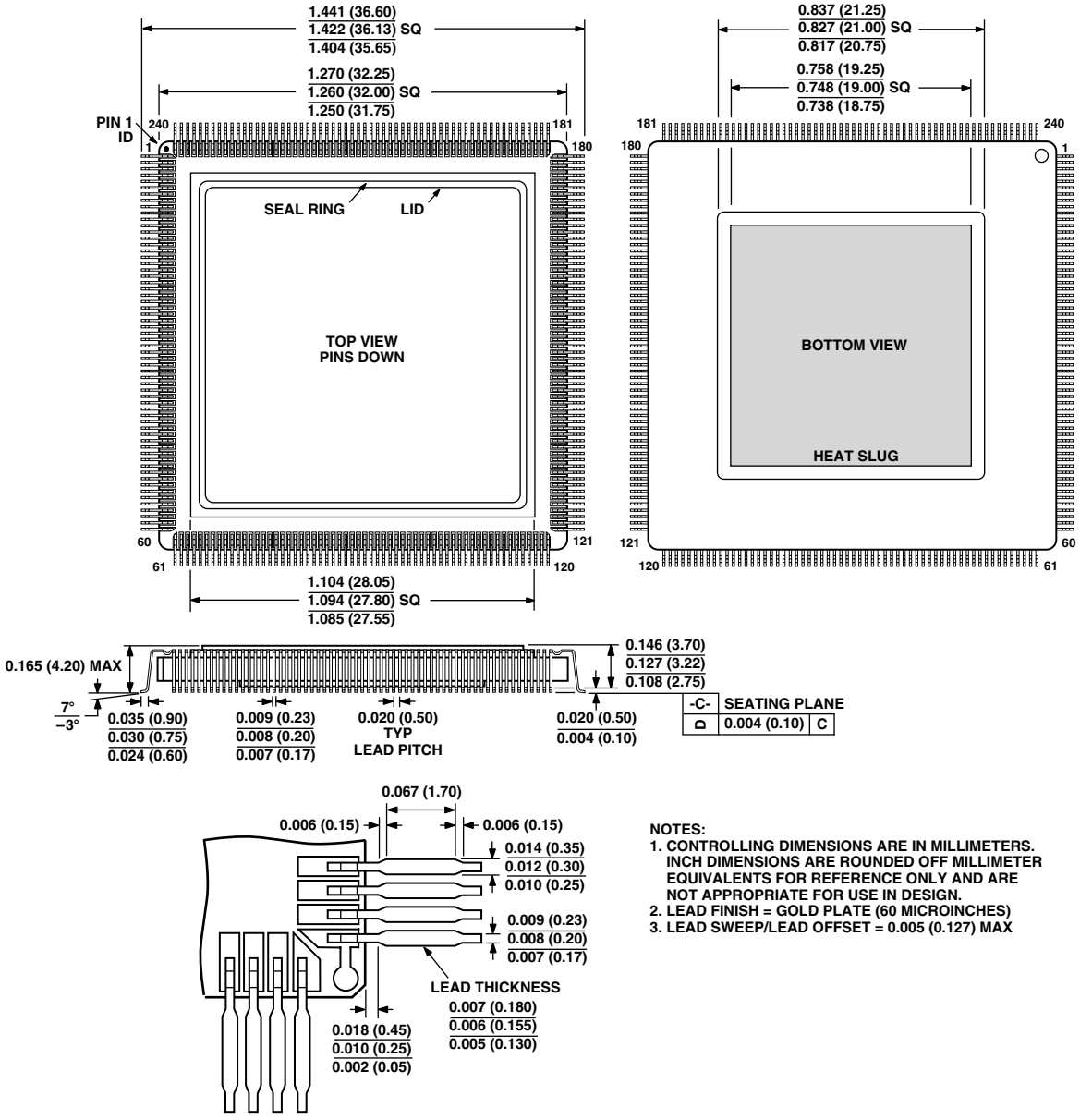
OUTLINE DIMENSIONS

Dimensions shown in inches and (millimeters within parentheses).

240-Lead Metric CQFP with Heat Slug Down and Formed Leads (QS-240A)



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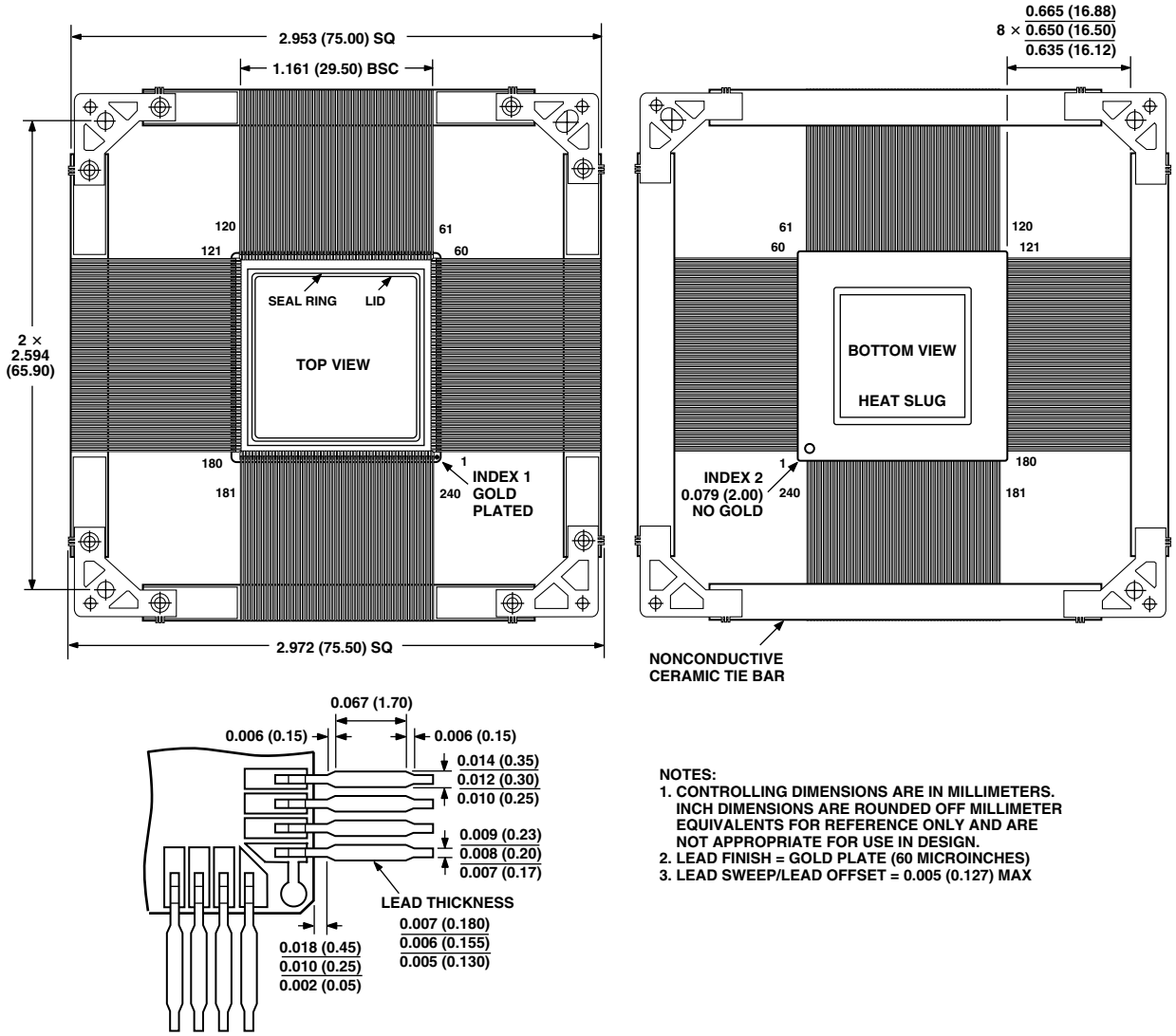
OUTLINE DIMENSIONS

Dimensions shown in inches and (millimeters within parentheses).

240-Lead Metric CQFP with Heat Slug Down and Unformed Leads (QS-240A)



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3. LEAD SWEEP/LEAD OFFSET = 0.005 (0.127) MAX

ORDERING GUIDE

Part Number	Case Temperature Range	Heat Slug Orientation	Instruction Rate	Operating Voltage
ADSP-21060CZ-133	–40°C to +100°C	Heat Slug Up	33 MHz	5 V
ADSP-21060CZ-160	–40°C to +100°C	Heat Slug Up	40 MHz	5 V
ADSP-21060CW-133	–40°C to +100°C	Heat Slug Down	33 MHz	5 V
ADSP-21060CW-160	–40°C to +100°C	Heat Slug Down	40 MHz	5 V
ADSP-21060LCW-133	–40°C to +100°C	Heat Slug Down	33 MHz	3.3 V
ADSP-21060LCW-160	–40°C to +100°C	Heat Slug Down	40 MHz	3.3 V

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