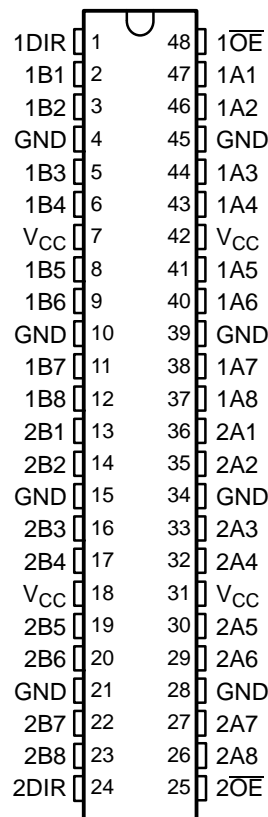


FEATURES

- Member of the Texas Instruments Widebus™ Family
- Operates From 1.65 V to 3.6 V
- Inputs Accept Voltages to 5.5 V
- Max t_{pd} of 4.8 ns at 3.3 V
- Typical V_{OLP} (Output Ground Bounce) <0.8 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$
- Typical V_{OHV} (Output V_{OH} Undershoot) >2 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$
- Supports Mixed-Mode Signal Operation on All Ports (5-V Input/Output Voltage With 3.3-V V_{CC})
- Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors
- All Outputs Have Equivalent 26- Ω Series Resistors, So No External Resistors Are Required
- I_{off} Supports Partial-Power-Down Mode Operation
- Latch-Up Performance Exceeds 250 mA Per JESD 17
- ESD Protection Exceeds JESD 22
 - 2000-V Human-Body Model (A114-A)
 - 200-V Machine Model (A115-A)

DGG, DGV, OR DL PACKAGE
(TOP VIEW)



DESCRIPTION/ORDERING INFORMATION

This 16-bit (dual-octal) noninverting bus transceiver is designed for 1.65-V to 3.6-V V_{CC} operation.

The SN74LVCHR16245A is designed for asynchronous communication between data buses. The control-function implementation minimizes external-timing requirements.

ORDERING INFORMATION

T_A	PACKAGE ⁽¹⁾		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	FBGA – GRD	Tape and reel	74LVCHR16245AGRDR	LR245A
	FBGA – ZRD (Pb-free)		74LVCHR16245AZRDR	
	SSOP – DL	Tape and reel	SN74LVCHR16245ALR	LVCHR16245A
			74LVCHR16245ALRG4	
	TSSOP – DGG	Tape and reel	SN74LVCHR16245AGR	LVCHR16245A
			74LVCHR16245AGRG4	
	TVSOP – DGV	Tape and reel	SN74LVCHR16245AVR	LDR245A
			74LVCHR16245AVRE4	
	VFBGA – GQL	Tape and reel	SN74LVCHR16245AKR	LR245A
	VFBGA – ZQL (Pb-free)		74LVCHR16245AZQLR	

(1) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

Widebus is a trademark of Texas Instruments.

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





































Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level. Use of pullup or pulldown resistors with the bus-hold circuitry is not recommended. The bus-hold circuitry is part of the input circuit and is not disabled by \overline{OE} or DIR.

	1	2	3	4	5	6
A	()	()	()	()	()	()
B	()	()	()	()	()	()
C	()	()	()	()	()	()
D	()	()	()	()	()	()
E	()	()			()	()
F	()	()			()	()
G	()	()	()	()	()	()
H	()	()	()	()	()	()
J	()	()	()	()	()	()
K	()	()	()	()	()	()

	1	2	3	4	5	6
A	1DIR	NC	NC	NC	NC	1OE
B	1B2	1B1	GND	GND	1A1	1A2
C	1B4	1B3	V _{CC}	V _{CC}	1A3	1A4
D	1B6	1B5	GND	GND	1A5	1A6
E	1B8	1B7			1A7	1A8
F	2B1	2B2			2A2	2A1
	G2B3	2B4	GND	GND	2A4	2A3
H	2B5	2B6	V _{CC}	V _{CC}	2A6	2A5
J	2B7	2B8	GND	GND	2A8	2A7
K	2DIR	NC	NC	NC	NC	2OE

(1) NC – No internal connection

	1	2	3	4	5	6
A						
B						
C						
D						
E						
F						
G						
H						
J						

	1	2	3	4	5	6
A	1B1	NC	1DIR	1OE	NC	1A1
B	1B3	1B2	NC	NC	1A2	1A3
C	1B5	1B4	V _{CC}	V _{CC}	1A4	1A5
D	1B7	1B6	GND	GND	1A6	1A7
E	2B1	1B8	GND	GND	1A8	2A1
F	2B3	2B2	GND	GND	2A2	2A3
G	2B5	2B4	V _{CC}	V _{CC}	2A4	2A5
H	2B7	2B6	NC	NC	2A6	2A7
J	2B8	NC	2DIR	2OE	NC	2A8

(1) NC – No internal connection

SN74LVCHR16245A

16-BIT BUS TRANSCEIVER

WITH 3-STATE OUTPUTS

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Absolute Maximum Ratings⁽¹⁾

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_{CC}	Supply voltage range	−0.5	6.5	V
V_I	Input voltage range ⁽²⁾	−0.5	6.5	V
V_O	Voltage range applied to any output in the high-impedance or power-off state ⁽²⁾	−0.5	6.5	V
V_O	Voltage range applied to any output in the high or low state ⁽²⁾⁽³⁾	−0.5	$V_{CC} + 0.5$	V
I_{IK}	Input clamp current	$V_I < 0$		−50 mA
I_{OK}	Output clamp current	$V_O < 0$		−50 mA
I_O	Continuous output current		±50	mA
	Continuous current through each V_{CC} or GND		±100	mA
θ_{JA}	Package thermal impedance ⁽⁴⁾	DGG package	70	°C/W
		DGV package	58	
		DL package	63	
		GQL/ZQL package	42	
		GRD/ZRD package	36	
T_{stg}	Storage temperature range	−65	150	°C

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
- (3) The value of V_{CC} is provided in the recommended operating conditions table.
- (4) The package thermal impedance is calculated in accordance with JESD 51-7.

Recommended Operating Conditions⁽¹⁾

			MIN	MAX	UNIT
V_{CC}	Supply voltage	Operating	1.65	3.6	V
		Data retention only	1.5		
V_{IH}	High-level input voltage	$V_{CC} = 1.65 \text{ V to } 1.95 \text{ V}$	$0.65 \times V_{CC}$		V
		$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$	1.7		
		$V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$	2		
V_{IL}	Low-level input voltage	$V_{CC} = 1.65 \text{ V to } 1.95 \text{ V}$		$0.35 \times V_{CC}$	V
		$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$		0.7	
		$V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$		0.8	
V_I	Input voltage		0	5.5	V
V_O	Output voltage	High or low state	0	V_{CC}	V
		3-state	0	5.5	
I_{OH}	High-level output current	$V_{CC} = 1.65 \text{ V}$		−2	mA
		$V_{CC} = 2.3 \text{ V}$		−4	
		$V_{CC} = 2.7 \text{ V}$		−8	
		$V_{CC} = 3 \text{ V}$		−12	
I_{OL}	Low-level output current	$V_{CC} = 1.65 \text{ V}$		2	mA
		$V_{CC} = 2.3 \text{ V}$		4	
		$V_{CC} = 2.7 \text{ V}$		8	
		$V_{CC} = 3 \text{ V}$		12	
$\Delta t/\Delta v$	Input transition rise or fall rate			10	ns/V
T_A	Operating free-air temperature		−40	85	°C

- (1) All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V _{CC}	MIN	TYP ⁽¹⁾	MAX	UNIT
V _{OH}		I _{OH} = –100 µA	1.65 V to 3.6 V	V _{CC} – 0.2			V
		I _{OH} = –2 mA	1.65 V	1.2			
		I _{OH} = –4 mA	2.3 V	1.7			
			2.7 V	2.2			
		I _{OH} = –6 mA	3 V	2.4			
		I _{OH} = –8 mA	2.7 V	2			
		I _{OH} = –12 mA	3 V	2			
V _{OL}		I _{OL} = 100 µA	1.65 V to 3.6 V			0.2	V
		I _{OL} = 2 mA	1.65 V			0.45	
		I _{OL} = 4 mA	2.3 V			0.7	
			2.7 V			0.4	
		I _{OL} = 6 mA	3 V			0.55	
		I _{OL} = 8 mA	2.7 V			0.6	
		I _{OL} = 12 mA	3 V			0.8	
I _I	Control inputs	V _I = 0 to 5.5 V	3.6 V			±5	µA
I _{I(hold)}	A or B port	V _I = 0.58 V	1.65 V	(2)			µA
		V _I = 1.07 V		(2)			
		V _I = 0.7 V	2.3 V	45			
		V _I = 1.7 V		–45			
		V _I = 0.8 V	3 V	75			
		V _I = 2 V		–75			
		V _I = 0 to 3.6 V ⁽³⁾	3.6 V			±500	
I _{off}		V _I or V _O = 5.5 V	0			±10	µA
I _{OZ} ⁽⁴⁾		V _O = 0 V or (V _{CC} to 5.5 V)	2.3 V to 3.6 V			±5	µA
I _{CC}		V _I = V _{CC} or GND	3.6 V			20	µA
		3.6 V ≤ V _I ≤ 5.5 V ⁽⁵⁾				20	
ΔI _{CC}		One input at V _{CC} – 0.6 V, Other inputs at V _{CC} or GND	2.7 V to 3.6 V			500	µA
C _i	Control inputs	V _I = V _{CC} or GND	3.3 V		3		pF
C _{io}	A or B port	V _O = V _{CC} or GND	3.3 V		12		pF

(1) All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

(2) This information was not available at the time of publication.

(3) This is the bus-hold maximum dynamic current. It is the minimum overdrive current required to switch the input from one state to another.

(4) For the total leakage current in an I/O port, please consult the I_{I(hold)} specification for the input voltage condition 0 V < V_I < V_{CC}, and the I_{OZ} specification for the input voltage conditions V_I = 0 V or V_I = V_{CC} to 5.5 V. The bus-hold current, at input voltages greater than V_{CC}, is negligible.

(5) This applies in the disabled state only.

SN74LVCHR16245A

16-BIT BUS TRANSCEIVER

WITH 3-STATE OUTPUTS

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Switching Characteristics

over recommended operating free-air temperature range (unless otherwise noted) (see [Figure 1](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 1.8\text{ V}$ $\pm 0.15\text{ V}$		$V_{CC} = 2.5\text{ V}$ $\pm 0.2\text{ V}$		$V_{CC} = 2.7\text{ V}$		$V_{CC} = 3.3\text{ V}$ $\pm 0.3\text{ V}$		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A or B	B or A	1	12.5	1	9.5	1	5.7	1.5	4.8	ns
t_{en}	\overline{OE}	A or B	1	15.8	1	12.2	1	7.9	1.5	6.3	ns
t_{dis}	\overline{OE}	A or B	1	19.2	1	11.9	1	8.3	2.2	7.4	ns

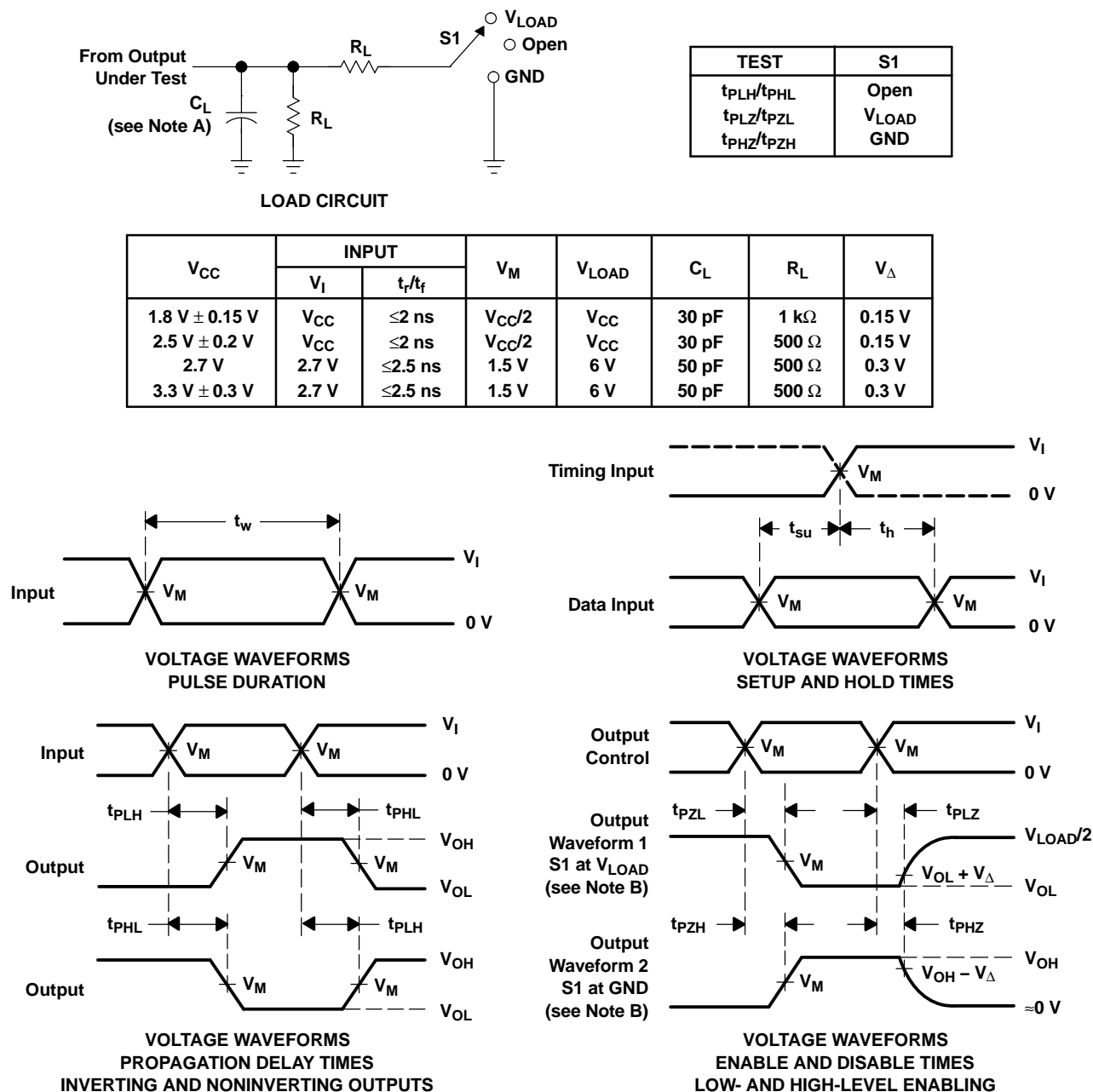
Operating Characteristics

$T_A = 25^\circ\text{C}$

PARAMETER			TEST CONDITIONS	$V_{CC} = 1.8\text{ V}$	$V_{CC} = 2.5\text{ V}$	$V_{CC} = 3.3\text{ V}$	UNIT
				TYP	TYP	TYP	
C_{pd}	Power dissipation capacitance per transceiver	Outputs enabled	$f = 10\text{ MHz}$	(1)	(1)	39	pF
		Outputs disabled		(1)	(1)	4	

(1) This information was not available at the time of publication.

PARAMETER MEASUREMENT INFORMATION



- NOTES:
- C_L includes probe and jig capacitance.
 - Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
 - All input pulses are supplied by generators having the following characteristics: $PRR \leq 10\text{ MHz}$, $Z_O = 50\text{ }\Omega$.
 - The outputs are measured one at a time, with one transition per measurement.
 - t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - t_{PZL} and t_{PZH} are the same as t_{en} .
 - t_{PLH} and t_{PHL} are the same as t_{pd} .
 - All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
74LVCHR16245AGRDR	ACTIVE	BGA MI CROSTAR JUNIOR	GRD	54	1000	TBD	SNPB	Level-1-240C-UNLIM
74LVCHR16245AGRG4	ACTIVE	TSSOP	DGG	48	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
74LVCHR16245ALRG4	ACTIVE	SSOP	DL	48	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
74LVCHR16245AVRE4	ACTIVE	TVSOP	DGV	48	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
74LVCHR16245AVRG4	ACTIVE	TVSOP	DGV	48	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
74LVCHR16245AZQLR	ACTIVE	BGA MI CROSTAR JUNIOR	ZQL	56	1000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM
74LVCHR16245AZRDR	ACTIVE	BGA MI CROSTAR JUNIOR	ZRD	54	1000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM
SN74LVCHR16245AGR	ACTIVE	TSSOP	DGG	48	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVCHR16245AKR	ACTIVE	BGA MI CROSTAR JUNIOR	GQL	56	1000	TBD	SNPB	Level-1-240C-UNLIM
SN74LVCHR16245ALR	ACTIVE	SSOP	DL	48	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVCHR16245AVR	ACTIVE	TVSOP	DGV	48	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

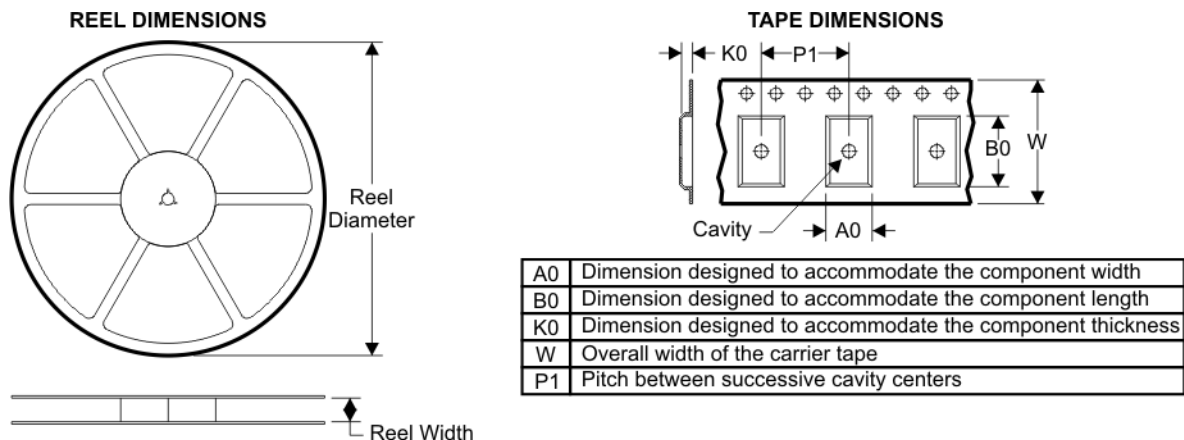
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

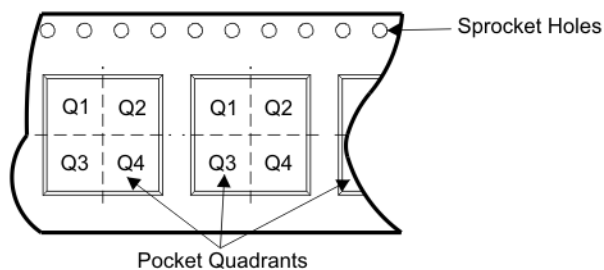
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TAPE AND REEL BOX INFORMATION



QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



Device	Package	Pins	Site	Reel Diameter (mm)	Reel Width (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
74LVCHR16245AGRDR	GRD	54	SITE 32	330	16	5.8	8.3	1.55	8	16	Q1
74LVCHR16245AZQLR	ZQL	56	SITE 32	330	16	4.8	7.3	1.45	8	16	Q1
74LVCHR16245AZQLR	ZQL	56	SITE 60	330	16	4.8	7.3	1.5	8	16	Q1
74LVCHR16245AZRDR	ZRD	54	SITE 32	330	16	5.8	8.3	1.55	8	16	Q1
SN74LVCHR16245AGR	DGG	48	SITE 41	330	24	8.6	15.8	1.8	12	24	Q1
SN74LVCHR16245AKR	GQL	56	SITE 32	330	16	4.8	7.3	1.45	8	16	Q1
SN74LVCHR16245AKR	GQL	56	SITE 60	330	16	4.8	7.3	1.5	8	16	Q1
SN74LVCHR16245ALR	DL	48	SITE 41	330	32	11.35	16.2	3.1	16	32	Q1
SN74LVCHR16245AVR	DGV	48	SITE 41	330	24	6.8	10.1	1.6	12	24	Q1

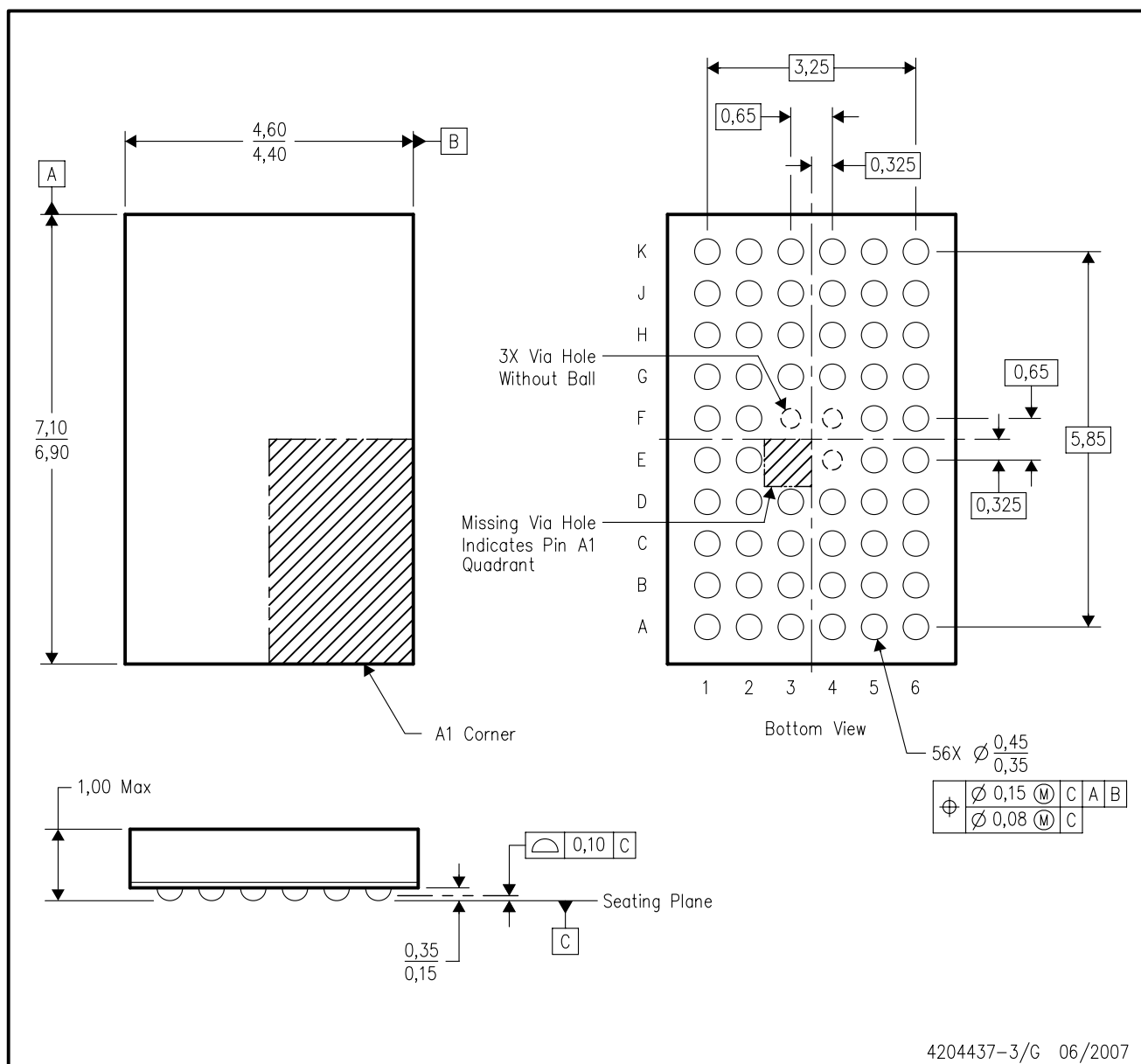
TAPE AND REEL BOX DIMENSIONS



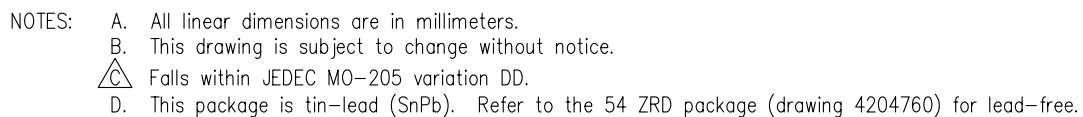
Device	Package	Pins	Site	Length (mm)	Width (mm)	Height (mm)
74LVCHR16245AGRDR	GRD	54	SITE 32	346.0	346.0	33.0
74LVCHR16245AZQLR	ZQL	56	SITE 32	346.0	346.0	33.0
74LVCHR16245AZQLR	ZQL	56	SITE 60	342.9	336.6	28.58
74LVCHR16245AZRDR	ZRD	54	SITE 32	346.0	346.0	33.0
SN74LVCHR16245AGR	DGG	48	SITE 41	346.0	346.0	41.0
SN74LVCHR16245AKR	GQL	56	SITE 32	346.0	346.0	33.0
SN74LVCHR16245AKR	GQL	56	SITE 60	342.9	336.6	28.58
SN74LVCHR16245ALR	DL	48	SITE 41	346.0	346.0	49.0
SN74LVCHR16245AVR	DGV	48	SITE 41	346.0	346.0	41.0

ZQL (R-PBGA-N56)

PLASTIC BALL GRID ARRAY

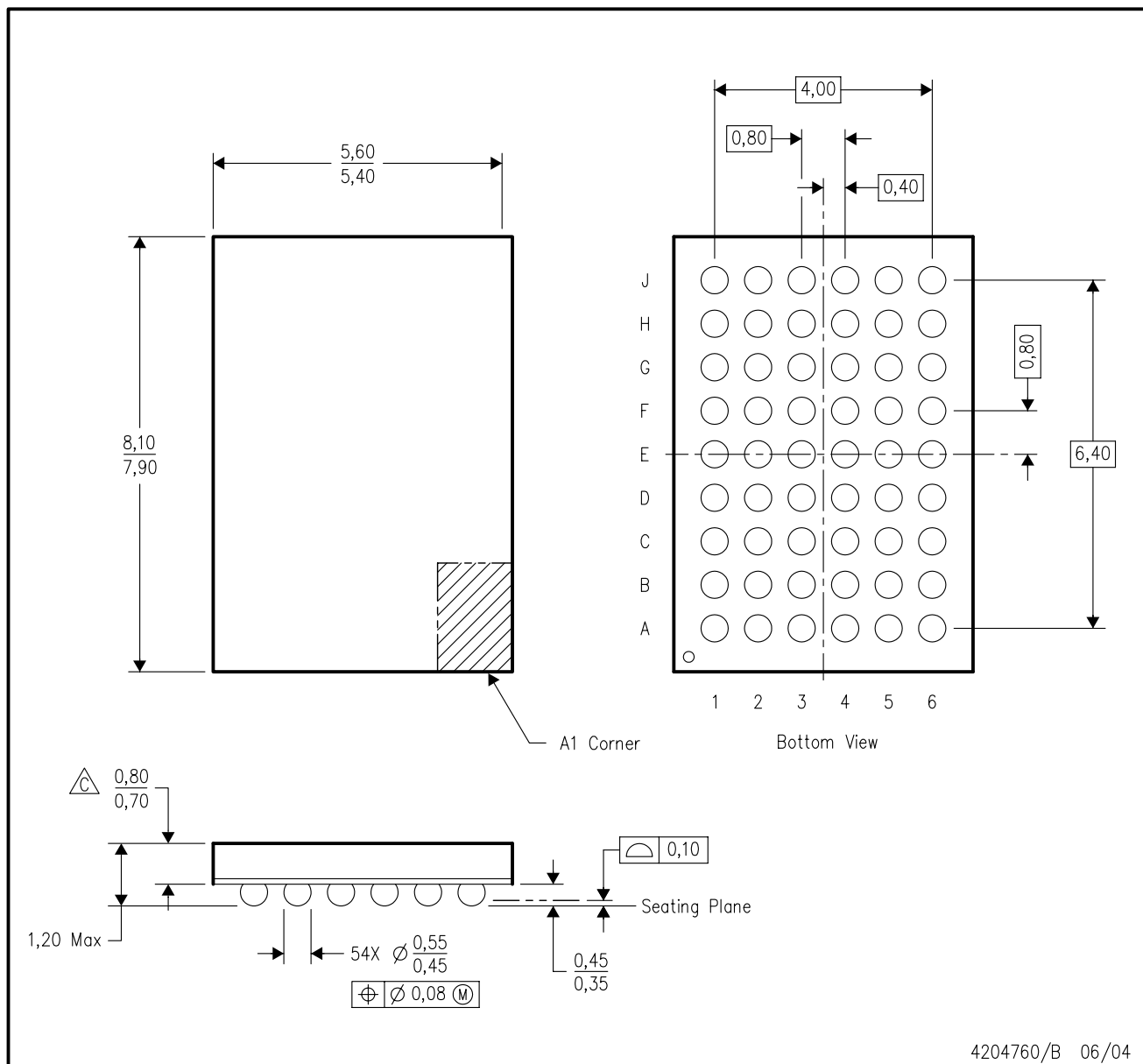


- NOTES:
- All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - This drawing is subject to change without notice.
 - Falls within JEDEC MO-285 variation BA-2.
 - This package is lead-free. Refer to the 56 GQL package (drawing 4200583) for tin-lead (SnPb).



ZRD (R-PBGA-N54)

PLASTIC BALL GRID ARRAY



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Falls within JEDEC MO-205 variation DD.
 - D. This package is lead-free. Refer to the 54 GRD package (drawing 4204759) for tin-lead (SnPb).

DGV (R-PDSO-G**)

PLASTIC SMALL-OUTLINE

24 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.
 D. Falls within JEDEC: 24/48 Pins – MO-153
 14/16/20/56 Pins – MO-194

GQL (R-PBGA-N56)

PLASTIC BALL GRID ARRAY



4200583-3/K 06/2007

- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. Falls within JEDEC MO-285 variation BA-2.
 - D. This package is tin-lead (SnPb). Refer to the 56 ZQL package (drawing 4204437) for lead-free.

DL (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

48 PINS SHOWN



- NOTES: A. All linear dimensions are in inches (millimeters).
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
 D. Falls within JEDEC MO-118

DGG (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

48 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-153

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