

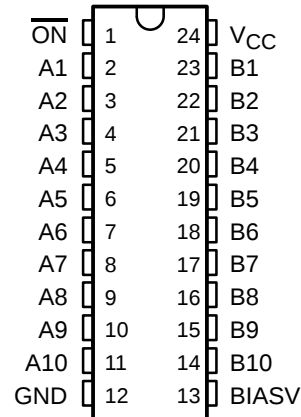
- 5-Ω Switch Connection Between Two Ports
- TTL-Compatible Input Levels
- Outputs Are Precharged by Bias Voltage to Minimize Signal Distortion During Live Insertion

## description

The SN74CBT6800A provides ten bits of high-speed TTL-compatible bus switching. The low on-state resistance of the switch allows bidirectional connections to be made while adding near-zero propagation delay. The device also precharges the B port to a user-selectable bias voltage (BIASV) to minimize live-insertion noise.

The SN74CBT6800A is organized as one 10-bit switch with a single enable ( $\overline{\text{ON}}$ ) input. When  $\overline{\text{ON}}$  is low, the switch is on, and port A is connected to port B. When  $\overline{\text{ON}}$  is high, the switch between port A and port B is open. When  $\overline{\text{ON}}$  is high or  $V_{CC}$  is 0 V, B port is precharged to BIASV through the equivalent of a 10-kΩ resistor.

DB, DBQ, DGV, DW, OR PW PACKAGE  
(TOP VIEW)



## ORDERING INFORMATION

| $T_A$         | PACKAGE†          |               | ORDERABLE PART NUMBER | TOP-SIDE MARKING |
|---------------|-------------------|---------------|-----------------------|------------------|
| –40°C to 85°C | SOIC – DW         | Tube          | SN74CBT6800ADW        | CBT6800A         |
|               |                   | Tape and reel | SN74CBT6800ADWR       |                  |
|               | SSOP – DB         | Tape and reel | SN74CBT6800ADBR       | CT6800A          |
|               | SSOP (QSOP) – DBQ | Tape and reel | SN74CBT6800ADBQR      | CBT6800A         |
|               | TSSOP – PW        | Tape and reel | SN74CBT6800APWR       | CT6800A          |
|               | TVSOP – DGV       | Tape and reel | SN74CBT6800ADGVR      | CT6800A          |

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at [www.ti.com/sc/package](http://www.ti.com/sc/package).

## FUNCTION TABLE

| INPUT $\overline{\text{ON}}$ | FUNCTION                     |
|------------------------------|------------------------------|
| L                            | A port = B port              |
| H                            | A port = Z<br>B port = BIASV |



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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

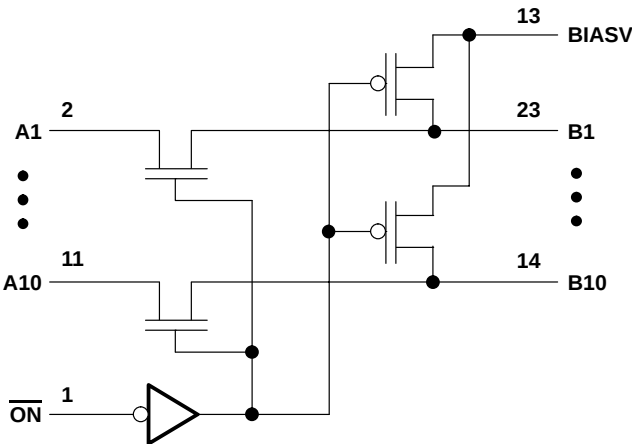
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SN74CBT6800A  
10-BIT FET BUS SWITCH  
WITH PRECHARGED OUTPUTS  
SCDS005N – MARCH 1993 – REVISED MARCH 2001

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)<sup>†</sup>

|                                                        |                |
|--------------------------------------------------------|----------------|
| Supply voltage range, $V_{CC}$                         | −0.5 V to 7 V  |
| Bias voltage range, BIASV                              | −0.5 V to 7 V  |
| Input voltage range, $V_I$ (see Note 1)                | −0.5 V to 7 V  |
| Continuous channel current                             | 128 mA         |
| Input clamp current, $I_{IK}$ ( $V_I < 0$ )            | −50 mA         |
| Package thermal impedance, $\theta_{JA}$ (see Note 2): |                |
| DB package                                             | 63°C/W         |
| DBQ package                                            | 61°C/W         |
| DGV package                                            | 86°C/W         |
| DW package                                             | 46°C/W         |
| PW package                                             | 88°C/W         |
| Storage temperature range, $T_{stg}$                   | −65°C to 150°C |

<sup>†</sup> Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.  
2. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Note 3)

|                                           | MIN | MAX      | UNIT |
|-------------------------------------------|-----|----------|------|
| $V_{CC}$ Supply voltage                   | 4   | 5.5      | V    |
| BIASV Supply voltage                      | 1.3 | $V_{CC}$ | V    |
| $V_{IH}$ High-level control input voltage | 2   |          | V    |
| $V_{IL}$ Low-level control input voltage  |     | 0.8      | V    |
| $T_A$ Operating free-air temperature      | −40 | 85       | °C   |

NOTE 3: All unused control inputs of the device must be held at  $V_{CC}$  or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

**electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)**

| PARAMETER                |                | TEST CONDITIONS                                         |                                                     | MIN  | TYP <sup>†</sup> | MAX     | UNIT          |
|--------------------------|----------------|---------------------------------------------------------|-----------------------------------------------------|------|------------------|---------|---------------|
| $V_{IK}$                 |                | $V_{CC} = 4.5\text{ V}$ ,                               | $I_I = -18\text{ mA}$                               |      |                  | -1.2    | V             |
| $I_I$                    |                | $V_{CC} = 5.5\text{ V}$ ,                               | $V_I = 5.5\text{ V}$ or GND                         |      |                  | $\pm 5$ | $\mu\text{A}$ |
| $I_O$                    |                | $V_{CC} = 4.5\text{ V}$ ,                               | $\text{BIASV} = 2.4\text{ V}$ , $V_O = 0$           | 0.25 |                  |         | mA            |
| $I_{CC}$                 |                | $V_{CC} = 5.5\text{ V}$ ,                               | $I_O = 0$ , $V_I = V_{CC}$ or GND                   |      |                  | 50      | $\mu\text{A}$ |
| $\Delta I_{CC}^\ddagger$ | Control inputs | $V_{CC} = 5.5\text{ V}$ ,                               | One input at 3.4 V, Other inputs at $V_{CC}$ or GND |      |                  | 2.5     | mA            |
| $C_i$                    | Control inputs | $V_I = 3\text{ V}$ or 0                                 |                                                     |      | 3.5              |         | pF            |
| $C_{O(\text{OFF})}$      |                | $V_O = 3\text{ V}$ or 0, Switch off                     |                                                     |      | 4.5              |         | pF            |
| $r_{on}^\S$              |                | $V_{CC} = 4\text{ V}$ ,<br>TYP at $V_{CC} = 4\text{ V}$ | $V_I = 2.4\text{ V}$ , $I_I = 15\text{ mA}$         |      | 11               | 20      | $\Omega$      |
|                          |                | $V_{CC} = 4.5\text{ V}$                                 | $V_I = 0$ , $I_I = 64\text{ mA}$                    |      | 3                | 7       |               |
|                          |                |                                                         | $I_I = 30\text{ mA}$                                |      | 3                | 7       |               |
|                          |                |                                                         | $V_I = 2.4\text{ V}$ , $I_I = 15\text{ mA}$         |      | 6                | 15      |               |

<sup>†</sup> All typical values are at  $V_{CC} = 5\text{ V}$  (unless otherwise noted),  $T_A = 25^\circ\text{C}$ .

<sup>‡</sup> This is the increase in supply current for each input that is at the specified TTL voltage level rather than  $V_{CC}$  or GND.

<sup>§</sup> Measured by the voltage drop between the A and B terminals at the indicated current through the switch. On-state resistance is determined by the lower of the voltages of the two (A or B) terminals.

**switching characteristics over recommended operating free-air temperature range,  $C_L = 50\text{ pF}$  (unless otherwise noted) (see Figure 1)**

| PARAMETER          | TEST CONDITIONS             | FROM (INPUT)           | TO (OUTPUT) | $V_{CC} = 4\text{ V}$ |      | $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$ |      | UNIT |
|--------------------|-----------------------------|------------------------|-------------|-----------------------|------|----------------------------------------|------|------|
|                    |                             |                        |             | MIN                   | MAX  | MIN                                    | MAX  |      |
| $t_{pd}^\parallel$ |                             | A or B                 | B or A      |                       | 0.35 |                                        | 0.25 | ns   |
| $t_{PZH}$          | $\text{BIASV} = \text{GND}$ | $\overline{\text{ON}}$ | A or B      |                       | 6    | 2                                      | 5.1  | ns   |
| $t_{PZL}$          | $\text{BIASV} = 3\text{ V}$ |                        |             |                       | 6    | 2                                      | 5.6  |      |
| $t_{PHZ}$          | $\text{BIASV} = \text{GND}$ | $\overline{\text{ON}}$ | A or B      |                       | 5.5  | 1                                      | 5    | ns   |
| $t_{PLZ}$          | $\text{BIASV} = 3\text{ V}$ |                        |             |                       | 5.5  | 2                                      | 5.9  |      |

<sup>||</sup> The propagation delay is the calculated RC time constant of the typical on-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).

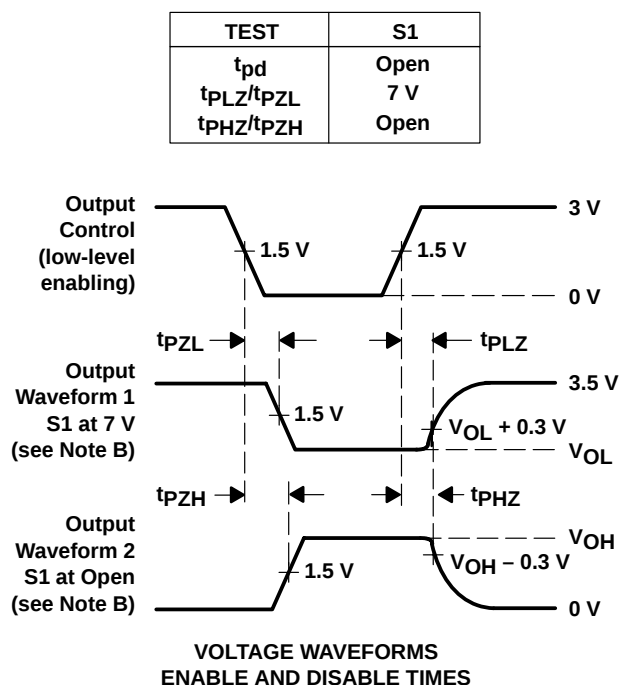
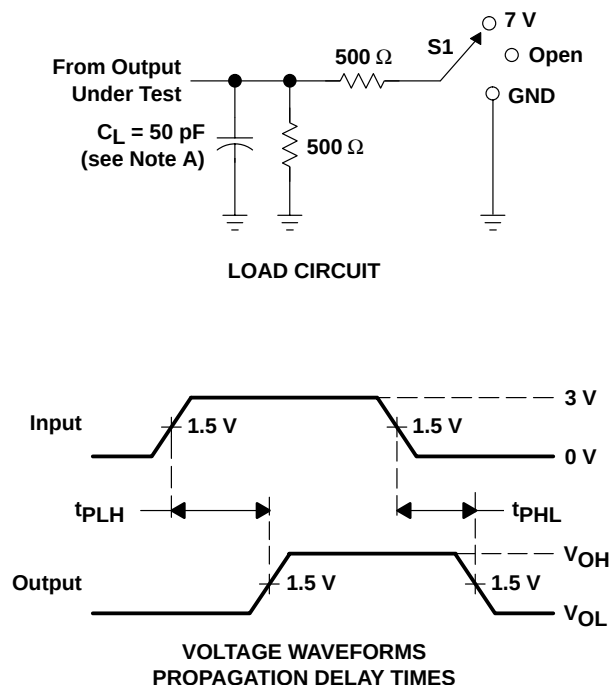
# SN74CBT6800A

## 10-BIT FET BUS SWITCH

### WITH PRECHARGED OUTPUTS

SCDS005N – MARCH 1993 – REVISED MARCH 2001

#### PARAMETER MEASUREMENT INFORMATION



- NOTES:
- A.  $C_L$  includes probe and jig capacitance.
  - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
  - C. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10 \text{ MHz}$ ,  $Z_O = 50 \Omega$ ,  $t_r \leq 2.5 \text{ ns}$ ,  $t_f \leq 2.5 \text{ ns}$ .
  - D. The outputs are measured one at a time with one transition per measurement.
  - E.  $t_{PLZ}$  and  $t_{PHZ}$  are the same as  $t_{dis}$ .
  - F.  $t_{PZL}$  and  $t_{PZH}$  are the same as  $t_{en}$ .
  - G.  $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{pd}$ .

Figure 1. Load Circuit and Voltage Waveforms

**PACKAGING INFORMATION**

| Orderable Device   | Status <sup>(1)</sup> | Package Type | Package Drawing | Pins | Package Qty | Eco Plan <sup>(2)</sup> | Lead/Ball Finish | MSL Peak Temp <sup>(3)</sup> |
|--------------------|-----------------------|--------------|-----------------|------|-------------|-------------------------|------------------|------------------------------|
| SN74CBT6800ADBQR   | ACTIVE                | SSOP/QSOP    | DBQ             | 24   | 2500        | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-2-260C-1 YEAR          |
| SN74CBT6800ADBQRE4 | ACTIVE                | SSOP/QSOP    | DBQ             | 24   | 2500        | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-2-260C-1 YEAR          |
| SN74CBT6800ADBQRG4 | ACTIVE                | SSOP/QSOP    | DBQ             | 24   | 2500        | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-2-260C-1 YEAR          |
| SN74CBT6800ADBR    | ACTIVE                | SSOP         | DB              | 24   | 2000        | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM           |
| SN74CBT6800ADBRE4  | ACTIVE                | SSOP         | DB              | 24   | 2000        | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM           |
| SN74CBT6800ADBRG4  | ACTIVE                | SSOP         | DB              | 24   | 2000        | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM           |
| SN74CBT6800ADGVR   | ACTIVE                | TVSOP        | DGV             | 24   | 2000        | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM           |
| SN74CBT6800ADGVRE4 | ACTIVE                | TVSOP        | DGV             | 24   | 2000        | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM           |
| SN74CBT6800ADGVRG4 | ACTIVE                | TVSOP        | DGV             | 24   | 2000        | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM           |
| SN74CBT6800ADW     | ACTIVE                | SOIC         | DW              | 24   | 25          | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM           |
| SN74CBT6800ADWE4   | ACTIVE                | SOIC         | DW              | 24   | 25          | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM           |
| SN74CBT6800ADWG4   | ACTIVE                | SOIC         | DW              | 24   | 25          | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM           |
| SN74CBT6800ADWR    | ACTIVE                | SOIC         | DW              | 24   | 2000        | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM           |
| SN74CBT6800ADWRE4  | ACTIVE                | SOIC         | DW              | 24   | 2000        | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM           |
| SN74CBT6800ADWRG4  | ACTIVE                | SOIC         | DW              | 24   | 2000        | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM           |
| SN74CBT6800APWR    | ACTIVE                | TSSOP        | PW              | 24   | 2000        | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM           |
| SN74CBT6800APWRE4  | ACTIVE                | TSSOP        | PW              | 24   | 2000        | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM           |
| SN74CBT6800APWRG4  | ACTIVE                | TSSOP        | PW              | 24   | 2000        | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM           |

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and

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package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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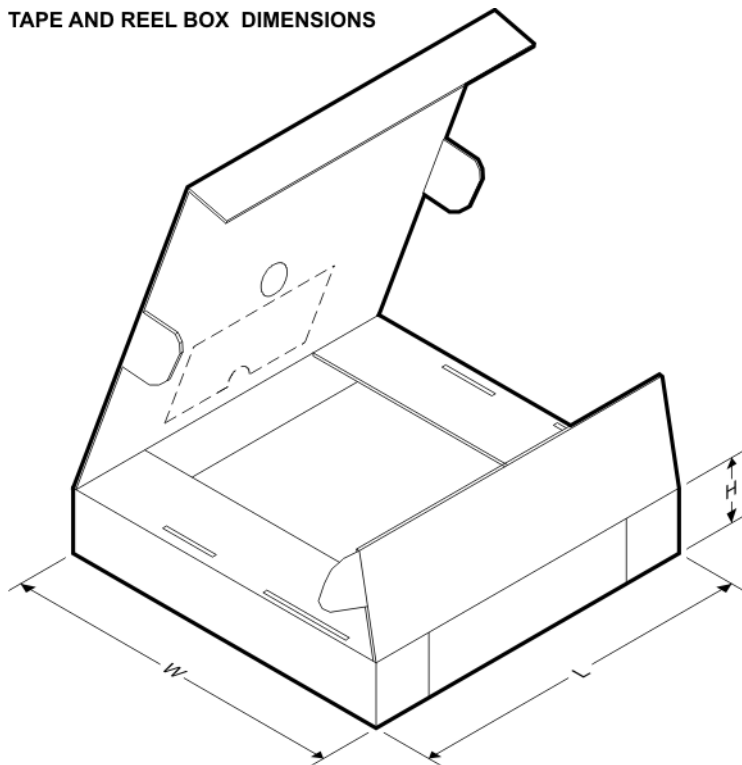
**TAPE AND REEL INFORMATION**



\*All dimensions are nominal

| Device           | Package Type | Package Drawing | Pins | SPQ  | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|------------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| SN74CBT6800ADBQR | SSOP/ QSOP   | DBQ             | 24   | 2500 | 330.0              | 16.4               | 6.5     | 9.0     | 2.1     | 8.0     | 16.0   | Q1            |
| SN74CBT6800ADBR  | SSOP         | DB              | 24   | 2000 | 330.0              | 16.4               | 8.2     | 8.8     | 2.5     | 12.0    | 16.0   | Q1            |
| SN74CBT6800ADGVR | TVSOP        | DGV             | 24   | 2000 | 330.0              | 12.4               | 7.0     | 5.6     | 1.6     | 8.0     | 12.0   | Q1            |
| SN74CBT6800ADWR  | SOIC         | DW              | 24   | 2000 | 330.0              | 24.4               | 10.75   | 15.7    | 2.7     | 12.0    | 24.0   | Q1            |
| SN74CBT6800APWR  | TSSOP        | PW              | 24   | 2000 | 330.0              | 16.4               | 6.95    | 8.3     | 1.6     | 8.0     | 16.0   | Q1            |

## TAPE AND REEL BOX DIMENSIONS



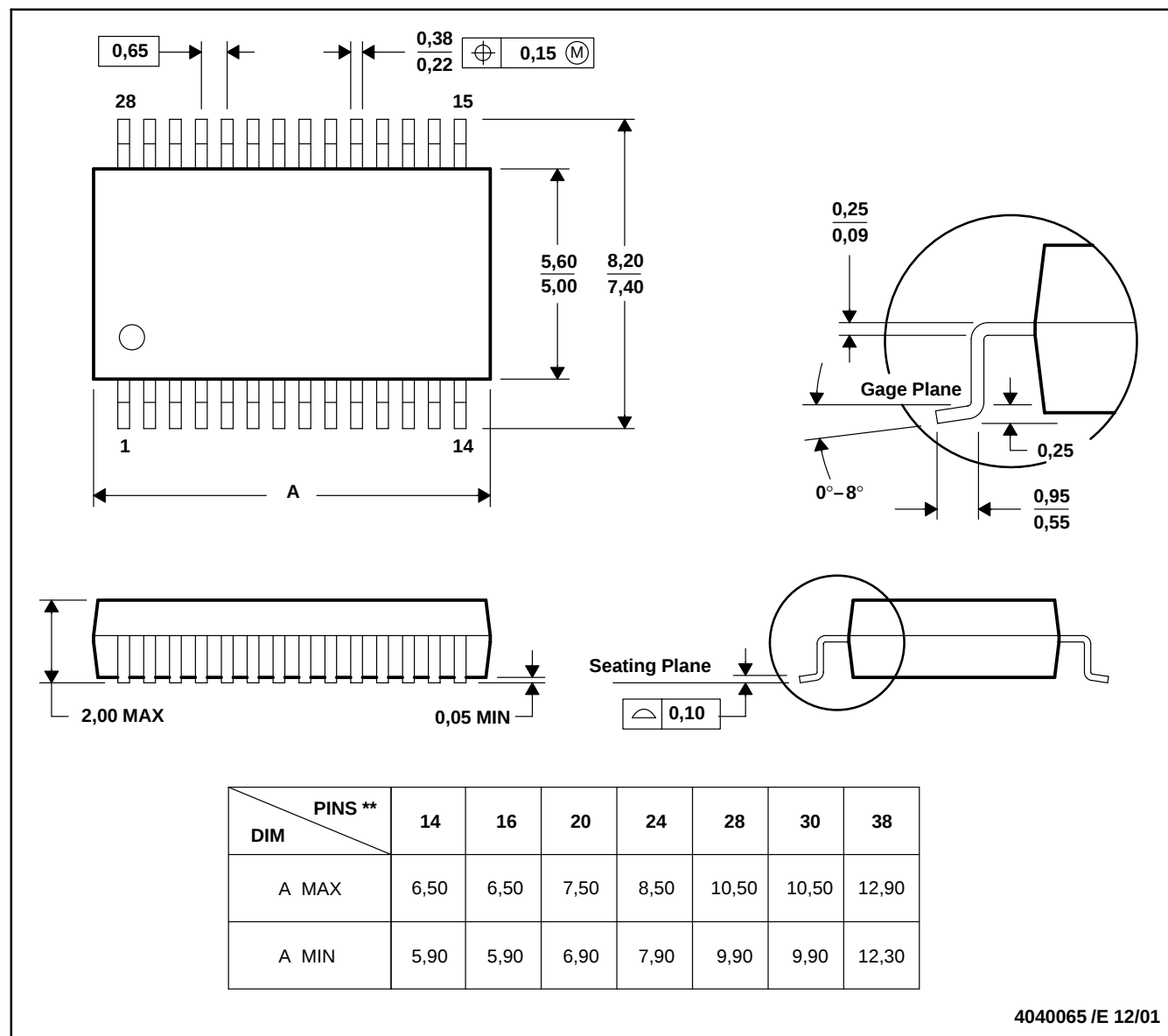
\*All dimensions are nominal

| Device           | Package Type | Package Drawing | Pins | SPQ  | Length (mm) | Width (mm) | Height (mm) |
|------------------|--------------|-----------------|------|------|-------------|------------|-------------|
| SN74CBT6800ADBQR | SSOP/QSOP    | DBQ             | 24   | 2500 | 346.0       | 346.0      | 33.0        |
| SN74CBT6800ADBR  | SSOP         | DB              | 24   | 2000 | 346.0       | 346.0      | 33.0        |
| SN74CBT6800ADGVR | TVSOP        | DGV             | 24   | 2000 | 346.0       | 346.0      | 29.0        |
| SN74CBT6800ADWR  | SOIC         | DW              | 24   | 2000 | 346.0       | 346.0      | 41.0        |
| SN74CBT6800APWR  | TSSOP        | PW              | 24   | 2000 | 346.0       | 346.0      | 33.0        |

## DB (R-PDSO-G\*\*)

## PLASTIC SMALL-OUTLINE

28 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.  
 D. Falls within JEDEC MO-150

## PW (R-PDSO-G\*\*)

## PLASTIC SMALL-OUTLINE PACKAGE

14 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.  
 D. Falls within JEDEC MO-153

## DGV (R-PDSO-G\*\*)

## PLASTIC SMALL-OUTLINE

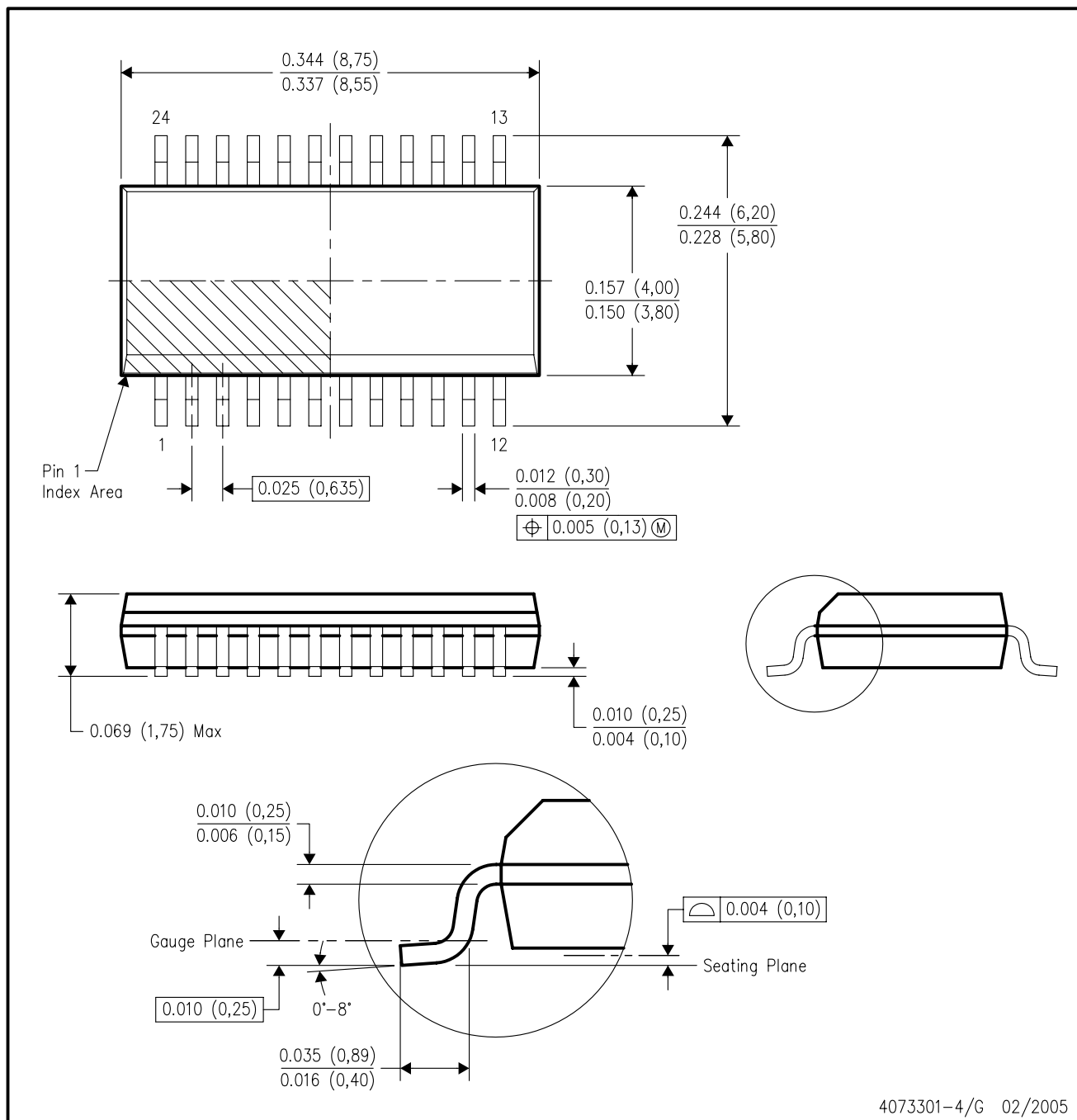
24 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.  
 D. Falls within JEDEC: 24/48 Pins – MO-153  
 14/16/20/56 Pins – MO-194

## DBQ (R-PDSO-G24)

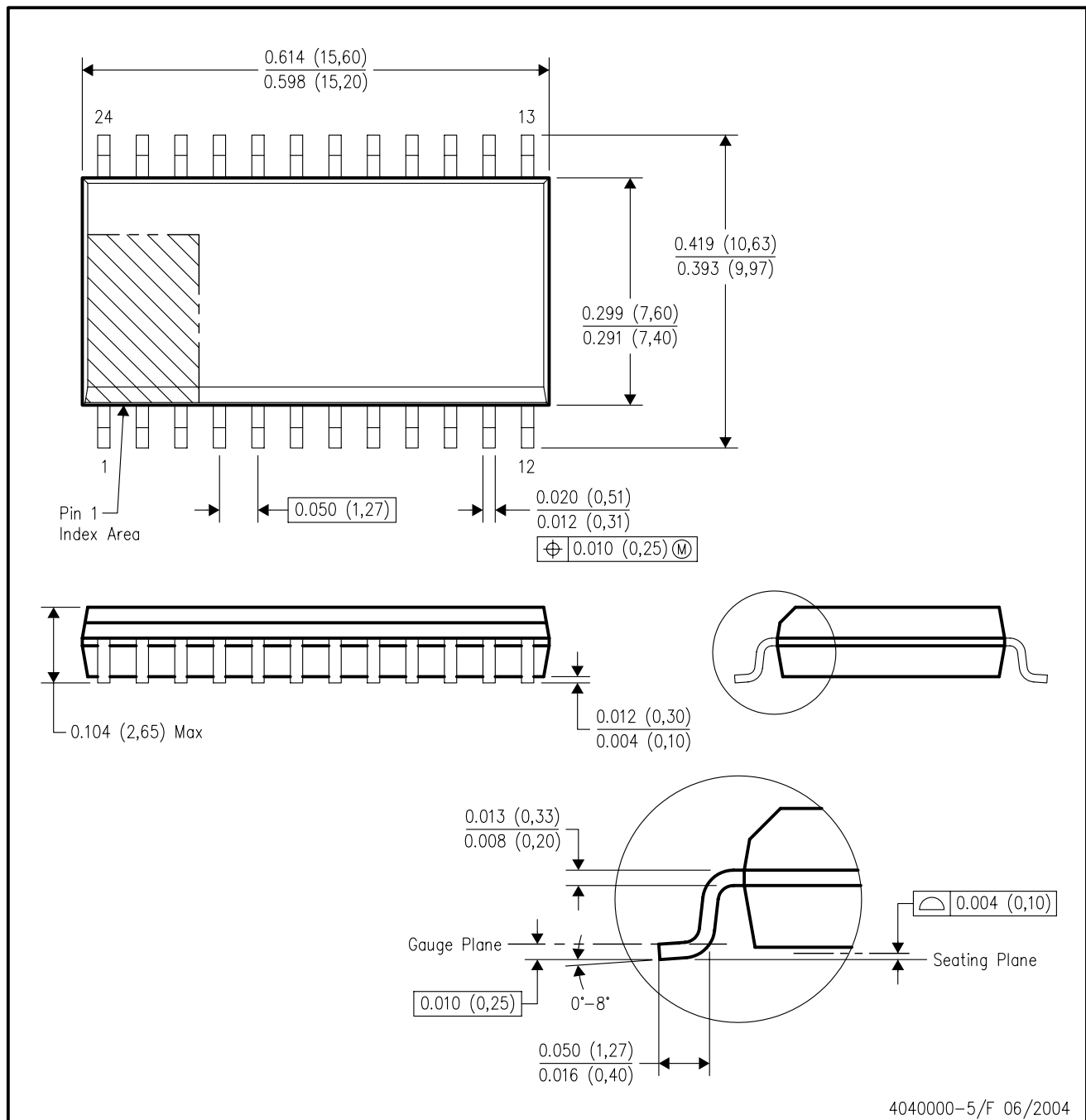
## PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- All linear dimensions are in inches (millimeters).
  - This drawing is subject to change without notice.
  - Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15) per side.
  - Falls within JEDEC MO-137 variation AE.

## DW (R-PDSO-G24)

## PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
  - D. Falls within JEDEC MS-013 variation AD.

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| Clocks and Timers           | <a href="http://www.ti.com/clocks">www.ti.com/clocks</a>           |
| Interface                   | <a href="http://interface.ti.com">interface.ti.com</a>             |
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| RF/IF and ZigBee® Solutions | <a href="http://www.ti.com/lprf">www.ti.com/lprf</a>               |

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