#### SN54BCT760, SN74BCT760 OCTAL BUFFERS/DRIVERS WITH OPEN-COLLECTOR OUTPUTS SCBS034B – JULY 1989 – REVISED NOVEMBER 1993

- Open-Collector Version of 'BCT244
- Open-Collector Outputs Drive Bus Lines or Buffer Memory Address Registers
- ESD Protection Exceeds 2000 V Per MIL-STD-883C Method 3015
- Packages Options Include Plastic Small-Outline (DW) Packages, Ceramic Chip Carriers (FK) and Flatpacks (W), and Standard Plastic and Ceramic 300-mil DIPs (J, N)

#### description

These octal buffers and line drivers are designed specifically to improve both the performance and density of 3-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters.

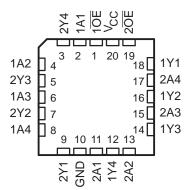
The 'BCT760 is organized as two 4-bit buffers/line drivers with separate output-enable ( $\overline{OE}$ ) inputs. When  $\overline{OE}$  is low, the device passes data from the A inputs to the Y outputs. When  $\overline{OE}$  is high, the outputs are in the high-impedance state.

The SN54BCT760 is characterized for operation over the full military temperature range of  $-55^{\circ}$ C to 125°C. The SN74BCT760 is characterized for operation from 0°C to 70°C.

SN54BCT760 J OR W PACKAGE						
SN74BCT760 DW OR N PACKAGE						

1OE 1 20 V <sub>CC</sub> 1A1 2 19 2OE   2Y4 3 18 1Y1   1A2 4 17 2A4   2Y3 5 16 1Y2   1A3 6 15 2A3   2Y2 7 14 1Y3   1A4 8 13 2A2   2Y1 9 12 1Y4   GND 10 11 2A1											
GND [10 11] 2A1	1A1 [ 2Y4 [ 1A2 [ 2Y3 [ 1A3 [ 2Y2 [ 1A4 ]	1 2 3 4 5 6 7 8	20 19 18 17 16 15 14 13	] 2 <del>0E</del> ] 1Y1 ] 2A4 ] 1Y2 ] 2A3 ] 1Y3 ] 2A2							
	-	1	11								

#### SN54BCT760 . . . FK PACKAGE (TOP VIEW)



#### FUNCTION TABLE (each buffer)

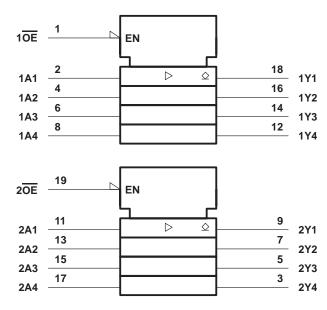
(each baller)									
INP	UTS	OUTPUT							
OE	Α	Y							
L	Н	Н							
L	L	L							
н	Х	н							

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

### SN54BCT760, SN74BCT760 **OCTAL BUFFERS/DRIVERS** WITH OPEN-COLLECTOR OUTPUTS

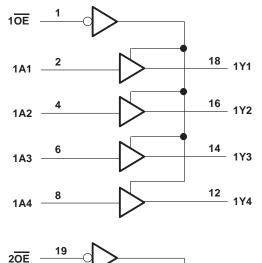
SCBS034B - JULY 1989 - REVISED NOVEMBER 1993

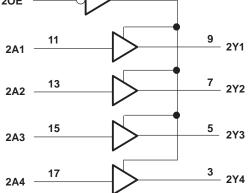
#### logic symbol<sup>†</sup>



<sup>†</sup> This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

#### logic diagram (positive logic)





#### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)<sup>‡</sup>

Supply voltage range, V <sub>CC</sub> Input voltage range, V <sub>I</sub> (see Note 1)	$-$ 0.5 V to 7 V
Input current range, I <sub>1</sub>	30 mA to 5 mA
Voltage range applied to any output in the disabled or power-off state, VO	$-$ 0.5 V to 5.5 V
Voltage range applied to any output in the high state, Vo	$\ldots$ – 0.5 V to V <sub>CC</sub>
Current into any output in the low state: SN54BCT760	96 mÅ
SN74BCT760	128 mA
Operating free-air temperature range: SN54BCT760	– 55°C to 125°C
SN74BCT760	0°C to 70°C
Storage temperature range	– 65°C to 150°C

<sup>‡</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The negative input voltage rating may be exceeded if the input clamp current rating is observed.



## SN54BCT760, SN74BCT760 OCTAL BUFFERS/DRIVERS WITH OPEN-COLLECTOR OUTPUTS

SCBS034B - JULY 1989 - REVISED NOVEMBER 1993

#### recommended operating conditions

		SN54BCT760			SN	UNIT		
		MIN	NOM	MAX	MIN	NOM	MAX	UNIT
VCC	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
VIH	High-level input voltage	2			2			V
VIL	Low-level input voltage			0.8			0.8	V
VOH	High-level output voltage			5.5			5.5	V
IIК	Input clamp current			-18			-18	mA
IOL	Low-level output current			48			64	mA
ТА	Operating free-air temperature	-55		125	0		70	°C

# electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

	SN	I54BCT7	60	SN	UNIT				
	MIN	TYP†	MAX	MIN	TYP†	MAX	UNIT		
V <sub>CC</sub> = 4.5 V,	lı = -18 mA				-1.2			-1.2	V
	I <sub>OL</sub> = 48 mA			0.38	0.55				V
VCC = 4.5 V	I <sub>OL</sub> = 64 mA						0.42	0.55	v
$V_{CC} = 5.5 V,$	VI = 7 V			0.1			0.1	mA	
V <sub>CC</sub> = 5.5 V,	V <sub>I</sub> = 2.7 V			20			20	μA	
$V_{CC} = 5.5 V,$	$V_{  } = 0.5 V$	V <sub>I</sub> = 0.5 V			-1			-1	mA
$V_{CC} = 4.5 V,$	V <sub>OH</sub> = 5.5 V				0.1			0.1	mA
		Outputs high		21	33		21	33	
V <sub>CC</sub> = 5.5 V,	Outputs open	Outputs low		48	76		48	76	mA
		OE disabled		6	10		6	10	
V <sub>CC</sub> = 5 V,	V <sub>I</sub> = 2.5 V or 0.5		6			6		pF	
V <sub>CC</sub> = 5 V,	V <sub>I</sub> = 2.5 V or 0.5		10			10		pF	
	$V_{CC} = 4.5 V$ $V_{CC} = 5.5 V,$ $V_{CC} = 5.5 V,$ $V_{CC} = 5.5 V,$ $V_{CC} = 4.5 V,$ $V_{CC} = 5.5 V,$ $V_{CC} = 5.5 V,$ $V_{CC} = 5.5 V,$	$\label{eq:VCC} \begin{array}{c} V_{CC} = 4.5 \ V, & I_{I} = -18 \ \text{mA} \\ \\ V_{CC} = 4.5 \ V & \hline I_{OL} = 48 \ \text{mA} \\ \hline I_{OL} = 64 \ \text{mA} \\ \\ V_{CC} = 5.5 \ V, & V_{I} = 7 \ V \\ \\ V_{CC} = 5.5 \ V, & V_{I} = 2.7 \ V \\ \\ V_{CC} = 5.5 \ V, & V_{I} = 0.5 \ V \\ \\ V_{CC} = 4.5 \ V, & V_{OH} = 5.5 \ V \\ \\ \\ V_{CC} = 5.5 \ V, & Outputs \ open \\ \\ \\ V_{CC} = 5 \ V, & V_{I} = 2.5 \ V \ or \ 0. \end{array}$	$\begin{array}{c} V_{CC} = 4.5 \ V & \hline I_{OL} = 48 \ \text{mA} \\ \hline I_{OL} = 64 \ \text{mA} \\ \hline V_{CC} = 5.5 \ \text{V}, & V_{I} = 7 \ \text{V} \\ \hline V_{CC} = 5.5 \ \text{V}, & V_{I} = 2.7 \ \text{V} \\ \hline V_{CC} = 5.5 \ \text{V}, & V_{I} = 0.5 \ \text{V} \\ \hline V_{CC} = 4.5 \ \text{V}, & V_{OH} = 5.5 \ \text{V} \\ \hline V_{CC} = 5.5 \ \text{V}, & Outputs \ \text{open} \\ \hline \hline \begin{array}{c} Outputs \ \text{high} \\ \hline Outputs \ \text{low} \\ \hline \hline \overline{\text{OE}} \ \text{disabled} \\ \hline \end{array} \\ \hline V_{CC} = 5 \ \text{V}, & V_{I} = 2.5 \ \text{V} \ \text{or} \ 0.5 \ \text{V} \\ \hline \end{array}$	TEST CONDITIONS     MIN $V_{CC} = 4.5 \text{ V}$ I <sub>I</sub> = -18 mA $V_{CC} = 4.5 \text{ V}$ IOL = 48 mA $I_{OL} = 64 \text{ mA}$ IOL = 64 mA $V_{CC} = 5.5 \text{ V}$ , $V_I = 7 \text{ V}$ V $V_{CC} = 5.5 \text{ V}$ , $V_I = 2.7 \text{ V}$ V $V_{CC} = 5.5 \text{ V}$ , $V_I = 0.5 \text{ V}$ V $V_{CC} = 4.5 \text{ V}$ , $V_{OH} = 5.5 \text{ V}$ Outputs high $V_{CC} = 5.5 \text{ V}$ , Outputs open   Outputs high $V_{CC} = 5.5 \text{ V}$ , $V_I = 2.5 \text{ V}$ or $0.5 \text{ V}$ V	$\begin{tabular}{ c c c c } \hline TEST CONDITIONS & \hline MIN TYPT \\ \hline V_{CC} = 4.5 \ V, & I_I = -18 \ mA & & & & & & & & & & & & & & & & & & $	$\begin{tabular}{ c c c c c c c } \hline \mbox{MIN TYPT MAX} \\ \hline \mbox{V}_{CC} = 4.5 \ \mbox{V} & I_I = -18 \ \mbox{mA} & -1.2 \\ \hline \mbox{V}_{CC} = 4.5 \ \mbox{V} & I_{OL} = 48 \ \mbox{mA} & 0.38 & 0.55 \\ \hline \mbox{I}_{OL} = 64 \ \mbox{mA} & 0.38 & 0.55 \\ \hline \mbox{I}_{OL} = 64 \ \mbox{mA} & 0.38 & 0.55 \\ \hline \mbox{V}_{CC} = 5.5 \ \mbox{V} & \mbox{V}_I = 7 \ \mbox{V} & 0.1 \\ \hline \mbox{V}_{CC} = 5.5 \ \mbox{V} & \mbox{V}_I = 2.7 \ \mbox{V} & 0.1 \\ \hline \mbox{V}_{CC} = 5.5 \ \mbox{V} & \mbox{V}_I = 2.7 \ \mbox{V} & 0.1 \\ \hline \mbox{V}_{CC} = 5.5 \ \mbox{V} & \mbox{V}_I = 0.5 \ \mbox{V} & -11 \\ \hline \mbox{V}_{CC} = 5.5 \ \mbox{V} & \mbox{V}_I = 0.5 \ \mbox{V} & 0.1 \\ \hline \mbox{V}_{CC} = 5.5 \ \mbox{V} & \mbox{Outputs open} & \hline \end{tabular} & \box{Outputs high} & 21 \ \mbox{33} \\ \hline \mbox{Outputs low} & \mbox{48} \ \ \mbox{76} \\ \hline \mbox{OE disabled} & \box{6} \ \ \mbox{10} \\ \hline \mbox{V}_{CC} = 5 \ \mbox{V} & \mbox{V}_I = 2.5 \ \mbox{V or } 0.5 \ \mbox{V} & \box{6} \\ \hline \end{tabular}$	$\begin{tabular}{ c c c c c c } \hline TEST CONDITIONS & \hline MIN $$TYP$^{\dagger}$ $$MAX $$MIN$ \\ \hline VCC = 4.5 V, $$I_I = -18 $mA$ $$-1.2$ \\ \hline U_{CC} = 4.5 V, $$I_{I} = -18 $mA$ $$0.38$ $$0.55$ \\ \hline U_{OL} = 64 $mA$ $$0.38$ $$0.55$ \\ \hline U_{OL} = 64 $mA$ $$0.38$ $$0.55$ \\ \hline U_{CC} = 5.5 V, $$V_I = 7 V$ $$0.1$ \\ \hline V_{CC} = 5.5 V, $$V_I = 2.7 V$ $$0.1$ \\ \hline V_{CC} = 5.5 V, $$V_I = 0.5 V$ $$0.1$ \\ \hline V_{CC} = 4.5 V, $$V_{OH} = 5.5 V$ $$0.1$ \\ \hline V_{CC} = 5.5 V, $$V_{I} = 0.5 V$ $$0.1$ \\ \hline V_{CC} = 5.5 V, $$V_{OH} = 5.5 V$ $$0.1$ \\ \hline V_{CC} = 5.5 V, $$Outputs open $$ $$0tputs high $$21$ $$33$ \\ \hline Outputs high $$21$ $$33$ \\ \hline Outputs low $$48$ $$76$ \\ \hline \hline \overline{OE}$ $ $disabled $$6$ $$10$ \\ \hline V_{CC} = 5 V, $$V_I = 2.5 V $$or 0.5 V$ $$ $$6$ \\ \hline \end{tabular}$	$\begin{tabular}{ c c c c c c } \hline TEST CONDITIONS & \hline MIN $$TYPT$ $$MAX$ $$MIN $$TYPT$ $$MIN $$TYPT$ $$MAX$ $$MIN $$TYPT$ $$MIN $$TYPT$ $$MAX$ $$MIN $$TYPT$ $$\\ \hline V_{CC} = 4.5 V, $$I_1 = -18 $mA$ $$-1.2$ $$\\ \hline U_{CC} = 4.5 V, $$I_0 = 64 $mA$ $$0.38$ $$0.55$ $$\\ \hline I_{0L} = 64 $mA$ $$0.38$ $$0.55$ $$\\ \hline U_{CC} = 5.5 V, $$V_1 = 7 V$ $$0.1$ $$\\ \hline V_{CC} = 5.5 V, $$V_1 = 2.7 V$ $$0.1$ $$\\ \hline V_{CC} = 5.5 V, $$V_1 = 0.5 V$ $$$0.1$ $$\\ \hline V_{CC} = 5.5 V, $$V_1 = 0.5 V$ $$$0.1$ $$\\ \hline V_{CC} = 5.5 V, $$V_1 = 0.5 V$ $$$0.1$ $$\\ \hline V_{CC} = 5.5 V, $$Outputs open $$ $$Outputs high $$21$ $$33$ $$21$ $$\\ \hline Outputs high $$21$ $$33$ $$21$ $$\\ \hline Outputs low $$48$ $$76$ $$48$ $$\\ \hline OE $$ $disabled $$6$ $$10$ $$6$ $$\\ \hline V_{CC} = 5 V, $$V_1 = 2.5 V $$or 0.5 V$ $$\\ \hline \end{tabular}$	$\begin{tabular}{ c c c c c c } \hline \mbox{TEST CONDITIONS} & \begin{tabular}{ c c c c c c c } \hline \mbox{MIN TYPT MAX} & \begin{tabular}{ c c c c c c c } \hline \mbox{MIN TYPT MAX} & \begin{tabular}{ c c c c c c c } \hline \mbox{MIN TYPT MAX} & \begin{tabular}{ c c c c c c c } \hline \mbox{MIN TYPT MAX} & \begin{tabular}{ c c c c c c c } \hline \mbox{MIN TYPT MAX} & \begin{tabular}{ c c c c c c c } \hline \mbox{MIN TYPT MAX} & \begin{tabular}{ c c c c c c c } \hline \mbox{MIN TYPT MAX} & \begin{tabular}{ c c c c c c c c } \hline \mbox{MIN TYPT MAX} & \begin{tabular}{ c c c c c c c c } \hline \mbox{MIN TYPT MAX} & \begin{tabular}{ c c c c c c c c c c c c c c c c c c c$

<sup>†</sup> All typical values are at V<sub>CC</sub> = 5 V,  $T_A = 25^{\circ}C$ .

#### switching characteristics (see Note 2)

PARAMETER	FROM (INPUT)	ТО (OUTPUT)	CL RL	C = 5 V, = 50 pF = 500 Ω = 25°C	; 2,	CL RL	= 50 pl = 500 Ω		V,	UNIT
			1	<b>3CT760</b>		SN54B	CT760	SN74B	CT760	
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
<sup>t</sup> PLH	Any A	v	6.3	8	9.5	6.3	11.1	6.3	10	
<sup>t</sup> PHL		ř	2.1	4.3	6.5	2.1	7.7	2.1	7.2	ns
<sup>t</sup> PLH	OE	V	8.6	13	15.2	8.6	18.7	8.6	17.5	-
<sup>t</sup> PHL		r	3.2	6.2	8.9	3.2	10.4	3.2	9.9	ns

<sup>‡</sup> For conditions shown as MIN or MAX, use the appropriate values specified under recommended operating conditions. NOTE 2: Load circuits and voltage waveforms are shown in Section 1.



9-Oct-2007

#### **PACKAGING INFORMATION**

JMENTS

www ti com

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	e Eco Plan <sup>(2)</sup>	Lead/Ball Finish	MSL Peak Temp <sup>(3)</sup>
5962-9093801M2A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type
5962-9093801MRA	ACTIVE	CDIP	J	20	1	TBD	A42 SNPB	N / A for Pkg Type
5962-9093801MSA	ACTIVE	CFP	W	20	1	TBD	A42	N / A for Pkg Type
SN54BCT760J	ACTIVE	CDIP	J	20	1	TBD	A42 SNPB	N / A for Pkg Type
SN74BCT760DW	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74BCT760DWE4	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74BCT760DWG4	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74BCT760DWR	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74BCT760DWRE4	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74BCT760DWRG4	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74BCT760N	ACTIVE	PDIP	Ν	20	20	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN74BCT760NE4	ACTIVE	PDIP	Ν	20	20	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN74BCT760NSR	ACTIVE	SO	NS	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74BCT760NSRE4	ACTIVE	SO	NS	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74BCT760NSRG4	ACTIVE	SO	NS	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SNJ54BCT760FK	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type
SNJ54BCT760J	ACTIVE	CDIP	J	20	1	TBD	A42 SNPB	N / A for Pkg Type
SNJ54BCT760W	ACTIVE	CFP	W	20	1	TBD	A42	N / A for Pkg Type

<sup>(1)</sup> The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

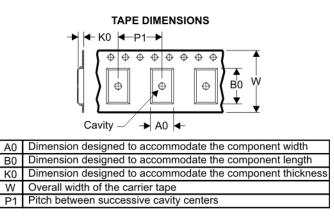


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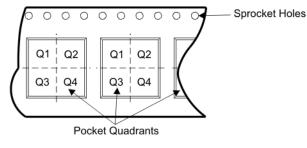
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#### TAPE AND REEL BOX INFORMATION





#### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

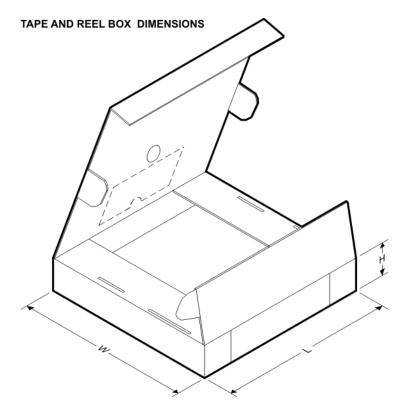


Device	Package	Pins	Site	Reel Diameter (mm)	Reel Width (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74BCT760DWR	DW	20	SITE 41	330	24	10.8	13.0	2.7	12	24	Q1



## PACKAGE MATERIALS INFORMATION

12-Feb-2008



Device	Package	Pins	Site	Length (mm)	Width (mm)	Height (mm)
SN74BCT760DWR	DW	20	SITE 41	346.0	346.0	41.0

J (R-GDIP-T\*\*) 14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



NOTES: A. All linear dimensions are in inches (millimeters).

- B. This drawing is subject to change without notice.
- C. This package is hermetically sealed with a ceramic lid using glass frit.
- D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
- E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

W (R-GDFP-F20)

CERAMIC DUAL FLATPACK



- NOTES: A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. This package can be hermetically sealed with a ceramic lid using glass frit.
  - D. Index point is provided on cap for terminal identification only.
  - E. Falls within Mil-Std 1835 GDFP2-F20



MLCC006B - OCTOBER 1996

#### FK (S-CQCC-N\*\*)

#### LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



NOTES: A. All linear dimensions are in inches (millimeters).

- B. This drawing is subject to change without notice.
- C. This package can be hermetically sealed with a metal lid.
- D. The terminals are gold plated.
- E. Falls within JEDEC MS-004



## N (R-PDIP-T\*\*)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



NOTES:

- A. All linear dimensions are in inches (millimeters).B. This drawing is subject to change without notice.
- Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
- $\triangle$  The 20 pin end lead shoulder width is a vendor option, either half or full width.



DW (R-PDSO-G20)

PLASTIC SMALL-OUTLINE PACKAGE



NOTES: A. All linear dimensions are in inches (millimeters).

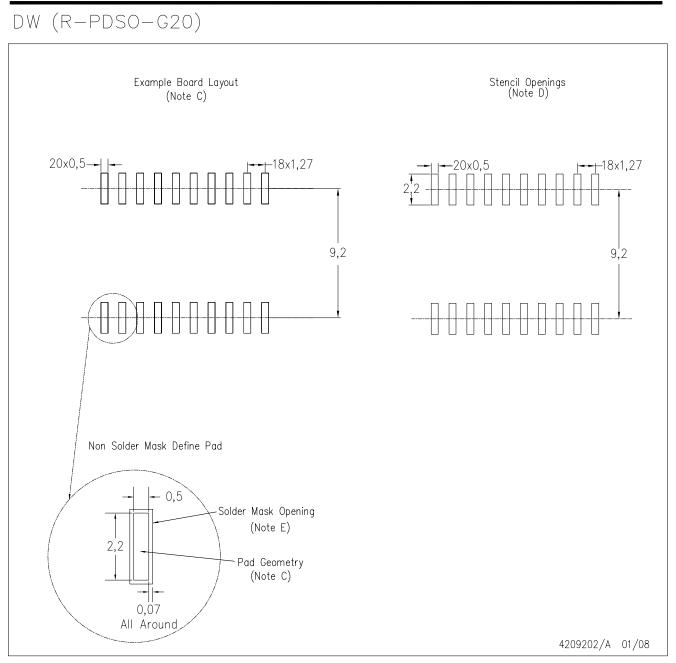
B. This drawing is subject to change without notice.

C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).

D. Falls within JEDEC MS-013 variation AC.



## LAND PATTERN



NOTES:

- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.



#### MECHANICAL DATA

#### PLASTIC SMALL-OUTLINE PACKAGE

#### 0,51 0,35 ⊕0,25⊛ 1,27 8 14 0,15 NOM 5,60 8,20 5,00 7,40 $\bigcirc$ Gage Plane ₽ 0,25 7 1 1,05 0,55 0°-10° Δ 0,15 0,05 Seating Plane — 2,00 MAX 0,10PINS \*\* 14 16 20 24 DIM 10,50 10,50 12,90 15,30 A MAX A MIN 9,90 9,90 12,30 14,70 4040062/C 03/03

NOTES: A. All linear dimensions are in millimeters.

NS (R-PDSO-G\*\*)

**14-PINS SHOWN** 

- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.



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