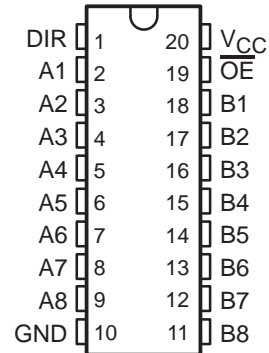


# SN54BCT640, SN74BCT640 OCTAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

SCBS025C – SEPTEMBER 1988 – REVISED APRIL 1994

- State-of-the-Art BiCMOS Design Substantially Reduces Standby Current
- Outputs Have Undershoot-Protection Circuitry
- Power-Up High-Impedance State
- Buffered Control Inputs to Reduce DC Loading Effects
- ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015
- Package Options Include Plastic Small-Outline (DW) Packages, Ceramic Chip Carriers (FK) and Flatpacks (W), and Plastic and Ceramic 300-mil DIPs (J, N)

SN54BCT640 . . . J OR W PACKAGE  
SN74BCT640 . . . DW OR N PACKAGE  
(TOP VIEW)

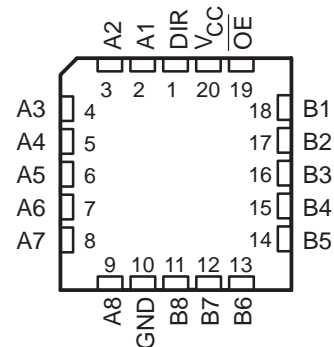


## description

The 'BCT640 bus transceiver is designed for asynchronous communication between data buses. These devices transmit data from the A bus to the B bus or from the B bus to the A bus depending upon the level at the direction-control (DIR) input. The output-enable ( $\overline{OE}$ ) input can be used to disable the device so that the buses are effectively isolated.

The SN54BCT640 is characterized for operation over the full military temperature range of  $-55^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ . The SN74BCT640 is characterized for operation from  $0^{\circ}\text{C}$  to  $70^{\circ}\text{C}$ .

SN54BCT640 . . . FK PACKAGE  
(TOP VIEW)

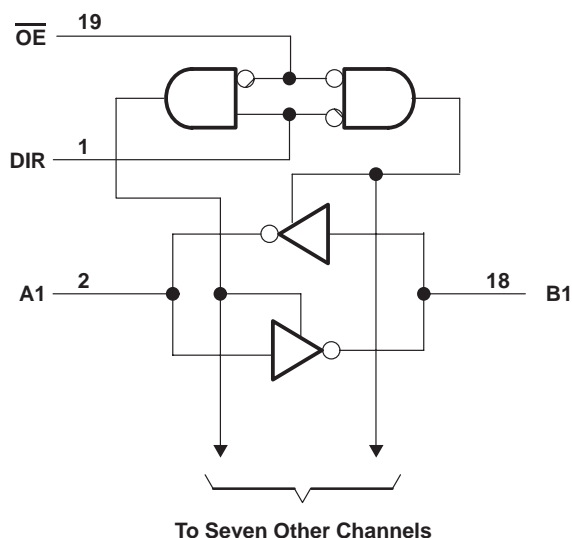
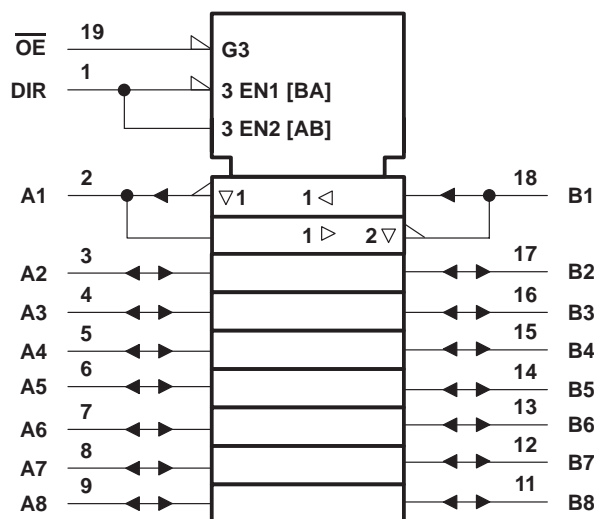


FUNCTION TABLE

INPUTS		OPERATION
$\overline{OE}$	DIR	
L	L	$\overline{B}$ data to A bus
L	H	$\overline{A}$ data to B bus
H	X	Isolation

## SCBS025C – SEPTEMBER 1988 – REVISED APRIL 1994

**logic diagram (positive logic)**



**absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡**

Supply voltage range, V <sub>CC</sub>	.....	- 0.5 V to 7 V
Input voltage range: Control inputs (see Note 1)	.....	- 0.5 V to 7 V
I/O ports (see Note 1)	.....	- 0.5 V to 5.5 V
Voltage range applied to any output in the disabled or power-off state, V <sub>O</sub>	.....	- 0.5 V to 5.5 V
Voltage range applied to any output in the high state, V <sub>O</sub>	.....	- 0.5 V to V <sub>CC</sub>
Input clamp current, I <sub>IK</sub>	.....	-30 mA
Current into any output in the low state: SN54BCT640	.....	96 mA
SN74BCT640	.....	128 mA
Operating free-air temperature range: SN54BCT640	.....	- 55°C to 125°C
SN74BCT640	.....	0°C to 70°C
Storage temperature range	.....	- 65°C to 150°C

NOTE 1: The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

# SN54BCT640, SN74BCT640 OCTAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

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## recommended operating conditions

			SN54BCT640			SN74BCT640			UNIT	
			MIN	NOM	MAX	MIN	NOM	MAX		
V <sub>CC</sub>	Supply voltage		4.5	5	5.5	4.5	5	5.5	V	
V <sub>IH</sub>	High-level input voltage		2			2			V	
V <sub>IL</sub>	Low-level input voltage		0.8			0.8			V	
I <sub>IK</sub>	Input clamp current		−18			−18			mA	
I <sub>OH</sub>	High-level output current		A port		−3		−3		mA	
			B port		−12		−15			
I <sub>OL</sub>	Low-level output current		A port		20		24		mA	
			B port		48		64			
T <sub>A</sub>	Operating free-air temperature		−55		125		0		70	°C

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54BCT640		SN74BCT640		UNIT
				MIN	TYP†	MAX	MIN	
$V_{IK}$		$V_{CC} = 4.5\text{ V}$ , $I_I = -18\text{ mA}$				–1.2		V
$V_{OH}$	A port	$V_{CC} = 4.5\text{ V}$	$I_{OH} = -1\text{ mA}$	2.5	3.4	2.5	3.4	V
			$I_{OH} = -3\text{ mA}$	2.4	3.3	2.4	3.3	
	B port	$V_{CC} = 4.5\text{ V}$	$I_{OH} = -3\text{ mA}$	2.4	3.3	2.4	3.3	
			$I_{OH} = -12\text{ mA}$	2	3.2			
$V_{OL}$	A port	$V_{CC} = 4.5\text{ V}$	$I_{OL} = 20\text{ mA}$		0.3	0.5		V
			$I_{OL} = 24\text{ mA}$				0.35	
	B port	$V_{CC} = 4.5\text{ V}$	$I_{OL} = 48\text{ mA}$		0.38	0.55		
			$I_{OL} = 64\text{ mA}$				0.42	
$I_I$	A or B port	$V_{CC} = 5.5\text{ V}$ , $V_I = 5.5\text{ V}$			1		1	mA
	Control inputs				0.1		0.1	
$I_{IH}^\ddagger$	A or B port	$V_{CC} = 5.5\text{ V}$ , $V_I = 2.7\text{ V}$			70		70	$\mu\text{A}$
	Control inputs				20		20	
$I_{IL}^\ddagger$	A or B port	$V_{CC} = 5.5\text{ V}$ , $V_I = 0.5\text{ V}$			–0.6		–0.6	mA
	Control inputs				–0.65		–0.65	
$I_{OS}^\S$	A port	$V_{CC} = 5.5\text{ V}$ , $V_O = 0$		–60		–150	–60	mA
	B port			–100		–225	–100	
$I_{CCL}$	A to B	$V_{CC} = 5.5\text{ V}$			53	84		mA
$I_{CCH}$	A to B	$V_{CC} = 5.5\text{ V}$			23	37		mA
$I_{CCZ}$		$V_{CC} = 5.5\text{ V}$			4	10		mA

† All typical values are at  $V_{CC} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$ .

‡ For I/O ports, the parameters  $I_{IH}$  and  $I_{IL}$  include the off-state output current.

§ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

# SN54BCT640, SN74BCT640

## OCTAL BUS TRANSCEIVERS

### WITH 3-STATE OUTPUTS

SCBS025C – SEPTEMBER 1988 – REVISED APRIL 1994

#### switching characteristics (see Note 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V <sub>CC</sub> = 5 V, C <sub>L</sub> = 50 pF, R <sub>1</sub> = 500 Ω, R <sub>2</sub> = 500 Ω, T <sub>A</sub> = 25°C			V <sub>CC</sub> = 4.5 V to 5.5 V, C <sub>L</sub> = 50 pF, R <sub>1</sub> = 500 Ω, R <sub>2</sub> = 500 Ω, T <sub>A</sub> = MIN to MAX†				UNIT
			'BCT640			SN54BCT640		SN74BCT640		
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t <sub>PLH</sub>	A or B	B or A	0.5	3.6	5.6	0.5	7	0.5	6.5	ns
t <sub>PHL</sub>			0.5	1.9	3.4	0.5	3.8	0.5	3.7	
t <sub>PZH</sub>	$\overline{\text{OE}}$	A or B	3.1	6.4	8.9	2.6	10.5	2.6	10.2	ns
t <sub>PZL</sub>			4.1	6.9	9.5	3.5	12.3	3.5	10.7	
t <sub>PHZ</sub>	$\overline{\text{OE}}$	A or B	1.9	5	7.9	1.4	12.2	1.4	10.2	ns
t <sub>PLZ</sub>			1.8	4.3	6.8	1.5	8.3	1.5	7.8	

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

NOTE 2: Load circuits and voltage waveforms are shown in Section 1.

**PACKAGING INFORMATION**

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/Ball Finish	MSL Peak Temp <sup>(3)</sup>
5962-9075201M2A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type
5962-9075201MRA	ACTIVE	CDIP	J	20	1	TBD	A42 SNPB	N / A for Pkg Type
5962-9075201MSA	ACTIVE	CFP	W	20	1	TBD	A42	N / A for Pkg Type
SN74BCT640DW	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74BCT640DWE4	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74BCT640DWG4	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74BCT640DWR	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74BCT640DWRE4	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74BCT640DWRG4	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74BCT640N	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN74BCT640NE4	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN74BCT640NSR	ACTIVE	SO	NS	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74BCT640NSRE4	ACTIVE	SO	NS	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74BCT640NSRG4	ACTIVE	SO	NS	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SNJ54BCT640FK	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type
SNJ54BCT640J	ACTIVE	CDIP	J	20	1	TBD	A42 SNPB	N / A for Pkg Type
SNJ54BCT640W	ACTIVE	CFP	W	20	1	TBD	A42	N / A for Pkg Type

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

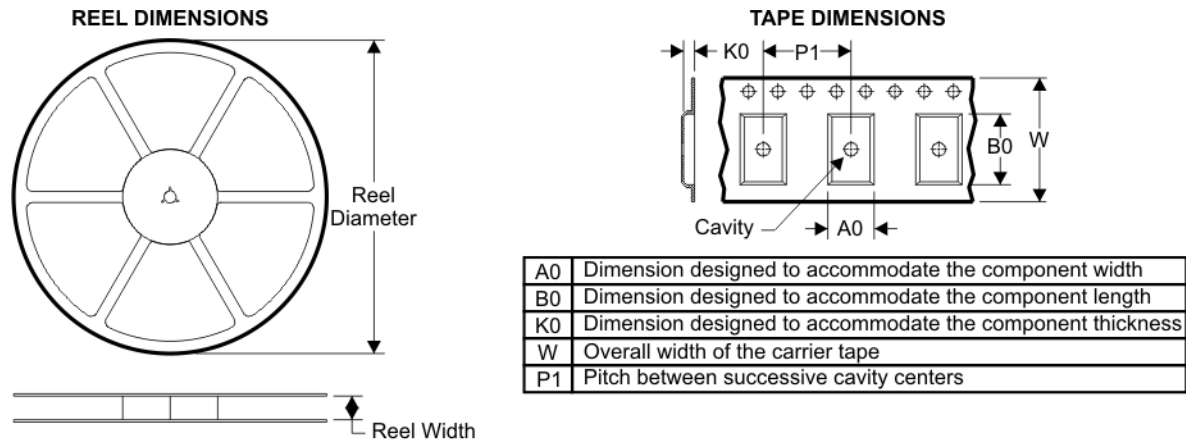
**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

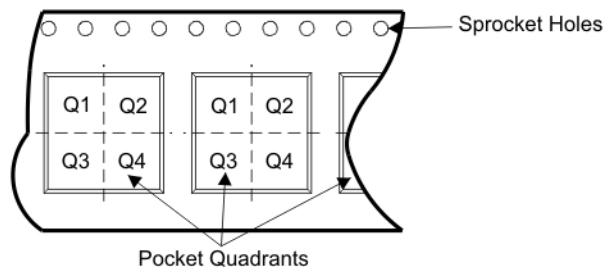
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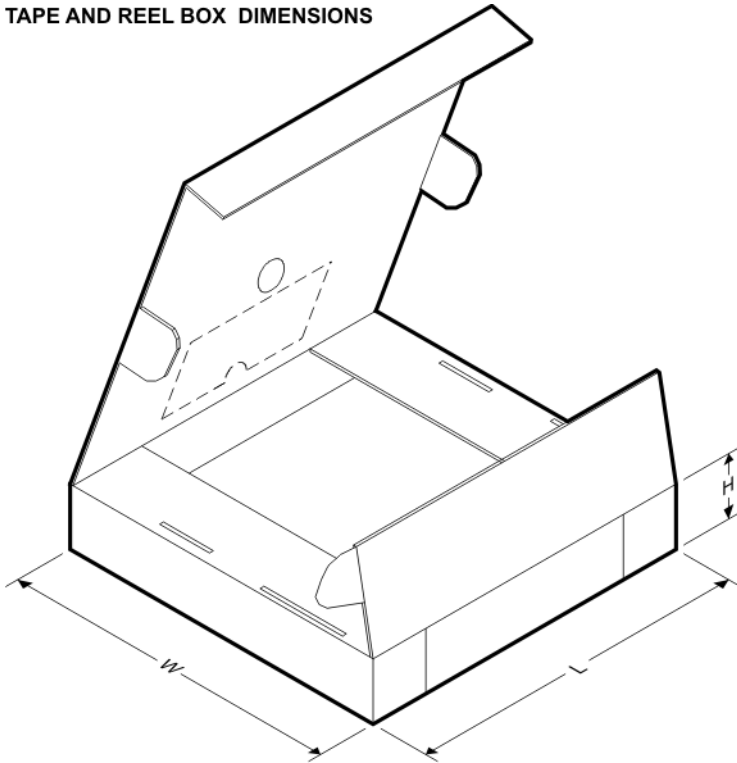


**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**



Device	Package	Pins	Site	Reel Diameter (mm)	Reel Width (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74BCT640DWR	DW	20	SITE 41	330	24	10.8	13.0	2.7	12	24	Q1
SN74BCT640NSR	NS	20	SITE 41	330	24	8.2	13.0	2.5	12	24	Q1

## TAPE AND REEL BOX DIMENSIONS



Device	Package	Pins	Site	Length (mm)	Width (mm)	Height (mm)
SN74BCT640DWR	DW	20	SITE 41	346.0	346.0	41.0
SN74BCT640NSR	NS	20	SITE 41	346.0	346.0	41.0



J (R-GDIP-T\*\*)

14 LEADS SHOWN

# CERAMIC DUAL IN-LINE PACKAGE



PINS ** DIM	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



4040083/F 03/03

- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. This package is hermetically sealed with a ceramic lid using glass frit.
  - D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
  - E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

W (R-GDFP-F20)

CERAMIC DUAL FLATPACK



- NOTES:
- All linear dimensions are in inches (millimeters).
  - This drawing is subject to change without notice.
  - This package can be hermetically sealed with a ceramic lid using glass frit.
  - Index point is provided on cap for terminal identification only.
  - Falls within Mil-Std 1835 GDFP2-F20

## FK (S-CQCC-N\*\*)

## LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. This package can be hermetically sealed with a metal lid.
  - D. The terminals are gold plated.
  - E. Falls within JEDEC MS-004

N (R-PDIP-T\*\*)

16 PINS SHOWN

## PLASTIC DUAL-IN-LINE PACKAGE



PINS ** DIM	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS-001 VARIATION	AA	BB	AC	AD



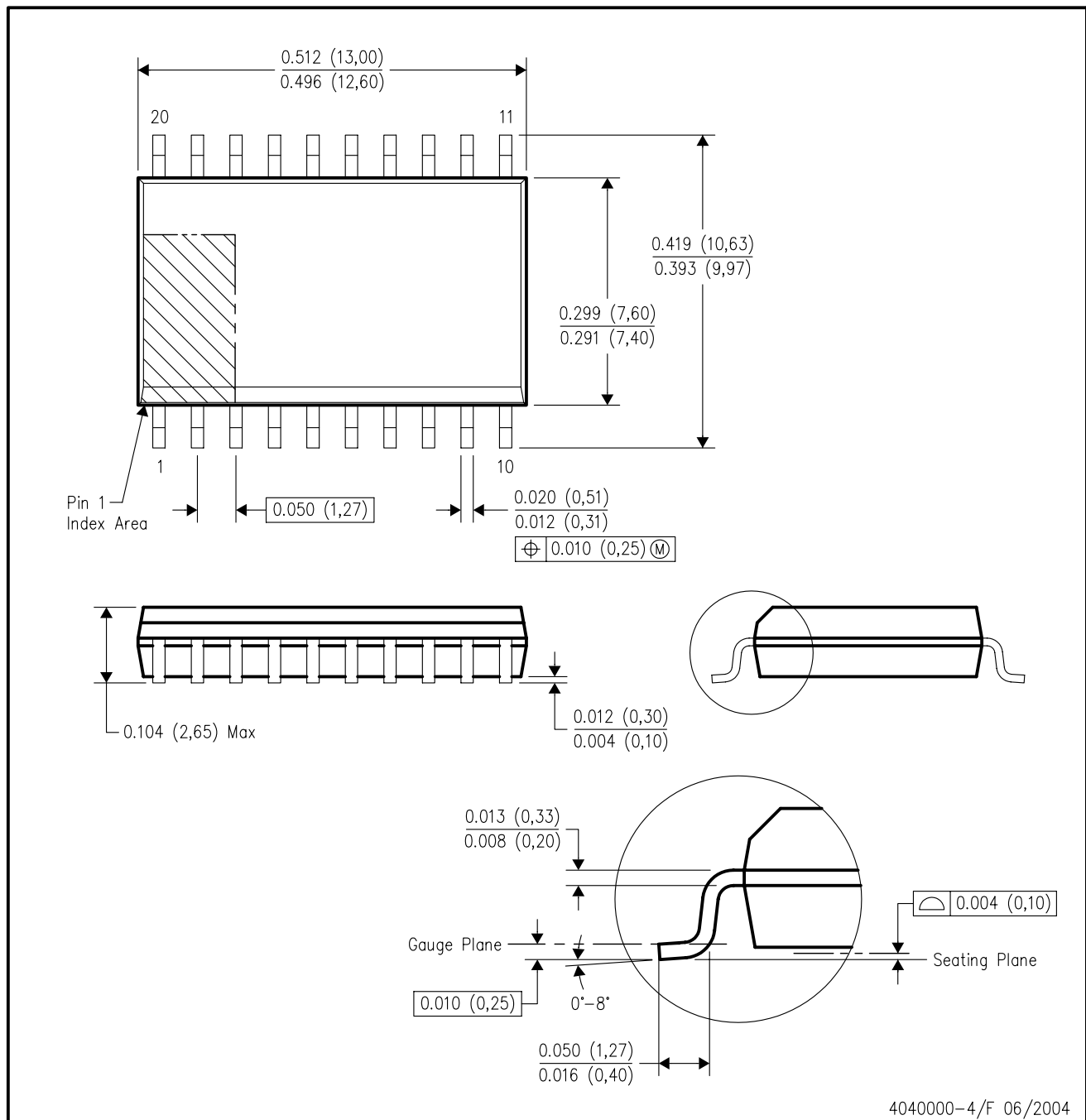
4040049/E 12/2002

NOTES:

- A. All linear dimensions are in inches (millimeters).  
B. This drawing is subject to change without notice.
-  Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).  
 The 20 pin end lead shoulder width is a vendor option, either half or full width.

DW (R-PDSO-G20)

PLASTIC SMALL-OUTLINE PACKAGE



# MECHANICAL DATA

NS (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

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