

## FEATURES

- Control Inputs  $V_{IH}/V_{IL}$  Levels Are Referenced to  $V_{CCA}$  Voltage
- $V_{CC}$  Isolation Feature – If Either  $V_{CC}$  Input Is at GND, Both Ports Are in the High-Impedance State
- Overvoltage-Tolerant Inputs/Outputs Allow Mixed-Voltage-Mode Data Communications
- Fully Configurable Dual-Rail Design Allows Each Port to Operate Over the Full 1.2-V to 3.6-V Power-Supply Range
- $I_{off}$  Supports Partial-Power-Down Mode Operation
- I/Os Are 4.6-V Tolerant
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Protection Exceeds JESD 22
  - 8000-V Human-Body Model (A114-A)
  - 200-V Machine Model (A115-A)
  - 1000-V Charged-Device Model (C101)

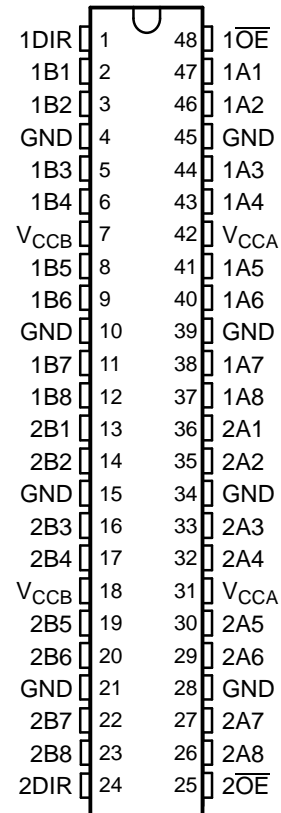
## DESCRIPTION/ORDERING INFORMATION

This 16-bit noninverting bus transceiver uses two separate configurable power-supply rails. The SN74AVC16T245 is optimized to operate with  $V_{CCA}/V_{CCB}$  set at 1.4 V to 3.6 V. It is operational with  $V_{CCA}/V_{CCB}$  as low as 1.2 V. The A port is designed to track  $V_{CCA}$ .  $V_{CCA}$  accepts any supply voltage from 1.2 V to 3.6 V. The B port is designed to track  $V_{CCB}$ .  $V_{CCB}$  accepts any supply voltage from 1.2 V to 3.6 V. This allows for universal low-voltage bidirectional translation between any of the 1.2-V, 1.5-V, 1.8-V, 2.5-V, and 3.3-V voltage nodes.

The SN74AVC16T245 is designed for asynchronous communication between data buses. The device transmits data from the A bus to the B bus or from the B bus to the A bus, depending on the logic level at the direction-control (DIR) input. The output-enable ( $\overline{OE}$ ) input can be used to disable the outputs so the buses effectively are isolated.

The SN74AVC16T245 is designed so that the control pins (1DIR, 2DIR,  $1\overline{OE}$ , and  $2\overline{OE}$ ) are supplied by  $V_{CCA}$ .

DGG OR DGV PACKAGE  
(TOP VIEW)



## ORDERING INFORMATION

$T_A$	PACKAGE <sup>(1)</sup>		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	TSSOP – DGG	Tape and reel	SN74AVC16T245DGGR	AVC16T245
	TVSOP – DGV	Tape and reel	SN74AVC16T245DGV	WF245
	VFBGA – GQL	Tape and reel	SN74AVC16T245GQLR	WF245
	VFBGA – ZQL (Pb-free)		SN74AVC16T245ZQLR	

(1) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at [www.ti.com/sc/package](http://www.ti.com/sc/package).



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

# SN74AVC16T245

## 16-BIT DUAL-SUPPLY BUS TRANSCEIVER

### WITH CONFIGURABLE VOLTAGE TRANSLATION AND 3-STATE OUTPUTS

SCES551C—FEBRUARY 2004—REVISED AUGUST 2005

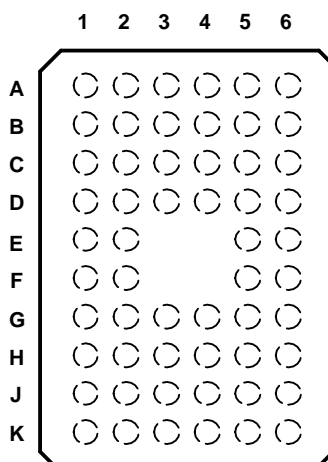
## DESCRIPTION/ORDERING INFORMATION (CONTINUED)

This device is fully specified for partial-power-down applications using  $I_{off}$ . The  $I_{off}$  circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

The  $V_{CC}$  isolation feature ensures that if either  $V_{CC}$  input is at GND, both ports are in the high-impedance state.

To ensure the high-impedance state during power up or power down,  $\overline{OE}$  should be tied to  $V_{CC}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

**GQL OR ZQL PACKAGE  
(TOP VIEW)**



## TERMINAL ASSIGNMENTS<sup>(2)</sup>

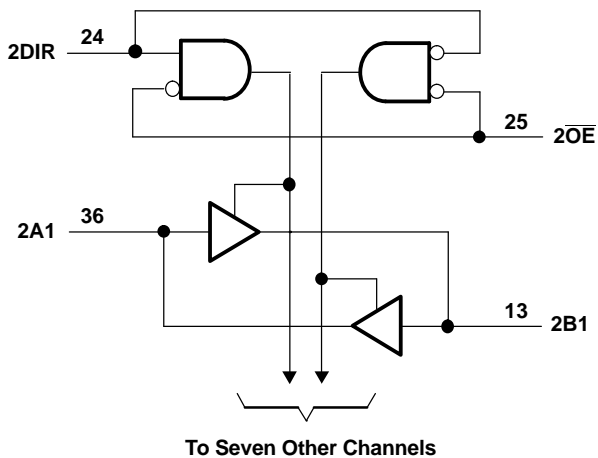
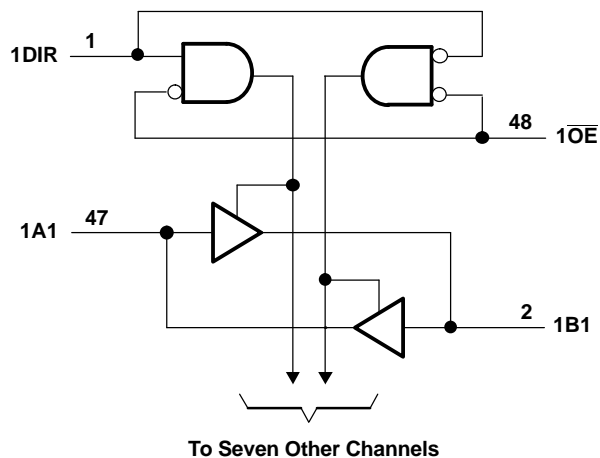
	1	2	3	4	5	6
<b>A</b>	1DIR	NC	NC	NC	NC	1 $\overline{OE}$
<b>B</b>	1B2	1B1	GND	GND	1A1	1A2
<b>C</b>	1B4	1B3	$V_{CCB}$	$V_{CCA}$	1A3	1A4
<b>D</b>	1B6	1B5	GND	GND	1A5	1A6
<b>E</b>	1B8	1B7			1A7	1A8
<b>F</b>	2B1	2B2			2A2	2A1
<b>G</b>	2B3	2B4	GND	GND	2A4	2A3
<b>H</b>	2B5	2B6	$V_{CCB}$	$V_{CCA}$	2A6	2A5
<b>J</b>	2B7	2B8	GND	GND	2A8	2A7
<b>K</b>	2DIR	NC	NC	NC	NC	2 $\overline{OE}$

(2) NC – No internal connection

## FUNCTION TABLE (EACH 8-BIT SECTION)

INPUTS		OPERATION
$\overline{OE}$	DIR	
L	L	B data to A bus
L	H	A data to B bus
H	X	Isolation

### LOGIC DIAGRAM (POSITIVE LOGIC)



### Absolute Maximum Ratings<sup>(1)</sup>

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
$V_{CCA}$ $V_{CCB}$	Supply voltage range		-0.5	4.6	V
$V_I$	Input voltage range <sup>(2)</sup>	I/O ports (A port)	-0.5	4.6	V
		I/O ports (B port)	-0.5	4.6	
		Control inputs	-0.5	4.6	
$V_O$	Voltage range applied to any output in the high-impedance or power-off state <sup>(2)</sup>	A port	-0.5	4.6	V
		B port	-0.5	4.6	
$V_O$	Voltage range applied to any output in the high or low state <sup>(2)(3)</sup>	A port	-0.5	$V_{CCA} + 0.5$	V
		B port	-0.5	$V_{CCB} + 0.5$	
$I_{IK}$	Input clamp current	$V_I < 0$		-50	mA
$I_{OK}$	Output clamp current	$V_O < 0$		-50	mA
$I_O$	Continuous output current			±50	mA
	Continuous current through each $V_{CCA}$ , $V_{CCB}$ , and GND			±100	mA
$\theta_{JA}$	Package thermal impedance <sup>(4)</sup>	DGG package		70	°C/W
		DGV package		58	
		GQL/ZQL package		42	
$T_{stg}$	Storage temperature range		-65	150	°C

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input voltage and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.
- (3) The output positive-voltage rating may be exceeded up to 4.6 V maximum if the output current rating is observed.
- (4) The package thermal impedance is calculated in accordance with JESD 51-7.

**Recommended Operating Conditions**<sup>(1)(2)(3)</sup>

			V <sub>CCI</sub>	V <sub>CCO</sub>	MIN	MAX	UNIT
V <sub>CCA</sub>	Supply voltage				1.2	3.6	V
V <sub>CCB</sub>	Supply voltage				1.2	3.6	V
V <sub>IH</sub>	High-level input voltage	Data inputs <sup>(4)</sup>	1.2 V to 1.95 V		V <sub>CCI</sub> × 0.65		V
			1.95 V to 2.7 V		1.6		
			2.7 V to 3.6 V		2		
V <sub>IL</sub>	Low-level input voltage	Data inputs <sup>(4)</sup>	1.2 V to 1.95 V		V <sub>CCI</sub> × 0.35		V
			1.95 V to 2.7 V		0.7		
			2.7 V to 3.6 V		0.8		
V <sub>IH</sub>	High-level input voltage	DIR (referenced to V <sub>CCA</sub> ) <sup>(5)</sup>	1.2 V to 1.95 V		V <sub>CCA</sub> × 0.65		V
			1.95 V to 2.7 V		1.6		
			2.7 V to 3.6 V		2		
V <sub>IL</sub>	Low-level input voltage	DIR (referenced to V <sub>CCA</sub> ) <sup>(5)</sup>	1.2 V to 1.95 V		V <sub>CCA</sub> × 0.35		V
			1.95 V to 2.7 V		0.7		
			2.7 V to 3.6 V		0.8		
V <sub>I</sub>	Input voltage				0	3.6	V
V <sub>O</sub>	Output voltage	Active state			0	V <sub>CCO</sub>	V
		3-state			0	3.6	
I <sub>OH</sub>	High-level output current			1.2 V	−3		mA
				1.4 V to 1.6 V	−6		
				1.65 V to 1.95 V	−8		
				2.3 V to 2.7 V	−9		
				3 V to 3.6 V	−12		
I <sub>OL</sub>	Low-level output current			1.2 V	3		mA
				1.4 V to 1.6 V	6		
				1.65 V to 1.95 V	8		
				2.3 V to 2.7 V	9		
				3 V to 3.6 V	12		
Δt/Δv	Input transition rise or fall rate				5		ns/V
T <sub>A</sub>	Operating free-air temperature				−40	85	°C

(1)  $V_{CCI}$  is the  $V_{CC}$  associated with the data input port.(2)  $V_{CCO}$  is the  $V_{CC}$  associated with the output port.(3) All unused data inputs of the device must be held at  $V_{CCI}$  or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.(4) For  $V_{CCI}$  values not specified in the data sheet,  $V_{IH}$  min =  $V_{CCI} \times 0.7$  V,  $V_{IL}$  max =  $V_{CCI} \times 0.3$  V.(5) For  $V_{CCA}$  values not specified in the data sheet,  $V_{IH}$  min =  $V_{CCA} \times 0.7$  V,  $V_{IL}$  max =  $V_{CCA} \times 0.3$  V.

## Electrical Characteristics<sup>(1)(2)</sup>

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V <sub>CCA</sub>	V <sub>CCB</sub>	T <sub>A</sub> = 25°C			−40°C to 85°C		UNIT
					MIN	TYP	MAX	MIN	MAX	
V <sub>OH</sub>		I <sub>OH</sub> = −100 μA	V <sub>I</sub> = V <sub>IH</sub>	1.2 V to 3.6 V	1.2 V to 3.6 V			V <sub>CCO</sub> − 0.2	V	
		I <sub>OH</sub> = −3 mA		1.2 V	1.2 V	0.95				
		I <sub>OH</sub> = −6 mA		1.4 V	1.4 V			1.05		
		I <sub>OH</sub> = −8 mA		1.65 V	1.65 V			1.2		
		I <sub>OH</sub> = −9 mA		2.3 V	2.3 V			1.75		
		I <sub>OH</sub> = −12 mA		3 V	3 V			2.3		
V <sub>OL</sub>		I <sub>OL</sub> = 100 μA	V <sub>I</sub> = V <sub>IL</sub>	1.2 V to 3.6 V	1.2 V to 3.6 V			0.2	V	
		I <sub>OL</sub> = 3 mA		1.2 V	1.2 V	0.15				
		I <sub>OL</sub> = 6 mA		1.4 V	1.4 V			0.35		
		I <sub>OL</sub> = 8 mA		1.65 V	1.65 V			0.45		
		I <sub>OL</sub> = 9 mA		2.3 V	2.3 V			0.55		
		I <sub>OL</sub> = 12 mA		3 V	3 V			0.7		
I <sub>I</sub>	Control inputs	V <sub>I</sub> = V <sub>CCA</sub> or GND	1.2 V to 3.6 V	1.2 V to 3.6 V	±0.025	±0.25	±1		μA	
I <sub>off</sub>	A or B port	V <sub>I</sub> or V <sub>O</sub> = 0 to 3.6 V	0 V	0 to 3.6 V	±0.1	±2.5	±5		μA	
	A or B port		0 to 3.6 V	0 V	±0.5	±2.5	±5			
I <sub>OZ</sub> <sup>(3)</sup>	A or B port	V <sub>O</sub> = V <sub>CCO</sub> or GND, V <sub>I</sub> = V <sub>CCI</sub> or GND, OE =V <sub>IH</sub>	3.6 V	3.6 V	±0.5	±2.5	±5		μA	
I <sub>CCA</sub>		V <sub>I</sub> = V <sub>CCI</sub> or GND, I <sub>O</sub> = 0	1.2 V to 3.6 V	1.2 V to 3.6 V			25		μA	
			0 V	3.6 V			−5			
			3.6 V	0 V			25			
I <sub>CCB</sub>		V <sub>I</sub> = V <sub>CCI</sub> or GND, I <sub>O</sub> = 0	1.2 V to 3.6 V	1.2 V to 3.6 V			25		μA	
			0 V	3.6 V			25			
			3.6 V	0 V			−5			
I <sub>CCA</sub> + I <sub>CCB</sub>		V <sub>I</sub> = V <sub>CCI</sub> or GND, I <sub>O</sub> = 0	1.2 V to 3.6 V	1.2 V to 3.6 V			45		μA	
C <sub>i</sub>	Control inputs	V <sub>I</sub> = 3.3 V or GND	3.3 V	3.3 V	3.5				pF	
C <sub>io</sub>	A or B port	V <sub>O</sub> = 3.3 V or GND	3.3 V	3.3 V	7				pF	

(1)  $V_{CCO}$  is the  $V_{CC}$  associated with the output port.

(2)  $V_{CCI}$  is the  $V_{CC}$  associated with the input port.

(3) For I/O ports, the parameter  $I_{OZ}$  includes the input leakage current.

# SN74AVC16T245

## 16-BIT DUAL-SUPPLY BUS TRANSCEIVER

### WITH CONFIGURABLE VOLTAGE TRANSLATION AND 3-STATE OUTPUTS

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#### Switching Characteristics

over recommended operating free-air temperature range,  $V_{CCA} = 1.2 \text{ V}$  (see [Figure 11](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CCB} = 1.2 \text{ V}$	$V_{CCB} = 1.5 \text{ V}$	$V_{CCB} = 1.8 \text{ V}$	$V_{CCB} = 2.5 \text{ V}$	$V_{CCB} = 3.3 \text{ V}$	UNIT
			TYP	TYP	TYP	TYP	TYP	
$t_{PLH}$	A	B	4.1	3.3	3	2.8	3.2	ns
$t_{PHL}$			4.1	3.3	3	2.8	3.2	
$t_{PLH}$	B	A	4.4	4	3.8	3.6	3.5	ns
$t_{PHL}$			4.4	4	3.8	3.6	3.5	
$t_{PZH}$	$\overline{OE}$	A	6.4	6.4	6.4	6.4	6.4	ns
$t_{PZL}$			6.4	6.4	6.4	6.4	6.4	
$t_{PZH}$	$\overline{OE}$	B	6	4.6	4	3.4	3.2	ns
$t_{PZL}$			6	4.6	4	3.4	3.2	
$t_{PHZ}$	$\overline{OE}$	A	6.6	6.6	6.6	6.6	6.8	ns
$t_{PLZ}$			6.6	6.6	6.6	6.6	6.8	
$t_{PHZ}$	$\overline{OE}$	B	6	4.9	4.9	4.2	5.3	ns
$t_{PLZ}$			6	4.9	4.9	4.2	5.3	

#### Switching Characteristics

over recommended operating free-air temperature range,  $V_{CCA} = 1.5 \text{ V} \pm 0.1 \text{ V}$  (see [Figure 11](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CCB} = 1.2 \text{ V}$	$V_{CCB} = 1.5 \text{ V} \pm 0.1 \text{ V}$		$V_{CCB} = 1.8 \text{ V} \pm 0.15 \text{ V}$		$V_{CCB} = 2.5 \text{ V} \pm 0.2 \text{ V}$		$V_{CCB} = 3.3 \text{ V} \pm 0.3 \text{ V}$		UNIT
			TYP	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
$t_{PLH}$	A	B	3.6	0.5	6.2	0.5	5.2	0.5	4.1	0.5	3.7	ns
$t_{PHL}$			3.6	0.5	6.2	0.5	5.2	0.5	4.1	0.5	3.7	
$t_{PLH}$	B	A	3.3	0.5	6.2	0.5	5.9	0.5	5.6	0.5	5.5	ns
$t_{PHL}$			3.3	0.5	6.2	0.5	5.9	0.5	5.6	0.5	5.5	
$t_{PZH}$	$\overline{OE}$	A	4.3	1	10.1	1	10.1	1	10.1	1	10.1	ns
$t_{PZL}$			4.3	1	10.1	1	10.1	1	10.1	1	10.1	
$t_{PZH}$	$\overline{OE}$	B	5.6	1	10.1	0.5	8.1	0.5	5.9	0.5	5.2	ns
$t_{PZL}$			5.6	1	10.1	0.5	8.1	0.5	5.9	0.5	5.2	
$t_{PHZ}$	$\overline{OE}$	A	4.5	1.5	9.1	1.5	9.1	1.5	9.1	1.5	9.1	ns
$t_{PLZ}$			4.5	1.5	9.1	1.5	9.1	1.5	9.1	1.5	9.1	
$t_{PHZ}$	$\overline{OE}$	B	5.5	1.5	8.7	1.5	7.5	1	6.5	1	6.3	ns
$t_{PLZ}$			5.5	1.5	8.7	1.5	7.5	1	6.5	1	6.3	

## Switching Characteristics

over recommended operating free-air temperature range,  $V_{CCA} = 1.8 \text{ V} \pm 0.15 \text{ V}$  (see [Figure 11](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CCB} = 1.2 \text{ V}$	$V_{CCB} = 1.5 \text{ V} \pm 0.1 \text{ V}$		$V_{CCB} = 1.8 \text{ V} \pm 0.15 \text{ V}$		$V_{CCB} = 2.5 \text{ V} \pm 0.2 \text{ V}$		$V_{CCB} = 3.3 \text{ V} \pm 0.3 \text{ V}$		UNIT
			TYP	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
$t_{PLH}$	A	B	3.4	0.5	5.9	0.5	4.8	0.5	3.7	0.5	3.3	ns
$t_{PHL}$			3.4	0.5	5.9	0.5	4.8	0.5	3.7	0.5	3.3	
$t_{PLH}$	B	A	3	0.5	5.2	0.5	4.8	0.5	4.5	0.5	4.4	ns
$t_{PHL}$			3	0.5	5.2	0.5	4.8	0.5	4.5	0.5	4.4	
$t_{PZH}$	$\overline{OE}$	A	3.4	1	7.8	1	7.8	1	7.8	1	7.8	ns
$t_{PZL}$			3.4	1	7.8	1	7.8	1	7.8	1	7.8	
$t_{PZH}$	$\overline{OE}$	B	5.4	1	9.2	0.5	7.4	0.5	5.3	0.5	4.5	ns
$t_{PZL}$			5.4	1	9.2	0.5	7.4	0.5	5.3	0.5	4.5	
$t_{PHZ}$	$\overline{OE}$	A	4.2	1.5	7.7	1.5	7.7	1.5	7.7	1.5	7.7	ns
$t_{PLZ}$			4.2	1.5	7.7	1.5	7.7	1.5	7.7	1.5	7.7	
$t_{PHZ}$	$\overline{OE}$	B	5.2	1.5	8.4	1.5	7.1	1	5.9	1	5.7	ns
$t_{PLZ}$			5.2	1.5	8.4	1.5	7.1	1	5.9	1	5.7	

## Switching Characteristics

over recommended operating free-air temperature range,  $V_{CCA} = 2.5 \text{ V} \pm 0.2 \text{ V}$  (see [Figure 11](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CCB} = 1.2 \text{ V}$	$V_{CCB} = 1.5 \text{ V} \pm 0.1 \text{ V}$		$V_{CCB} = 1.8 \text{ V} \pm 0.15 \text{ V}$		$V_{CCB} = 2.5 \text{ V} \pm 0.2 \text{ V}$		$V_{CCB} = 3.3 \text{ V} \pm 0.3 \text{ V}$		UNIT
			TYP	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
$t_{PLH}$	A	B	3.2	0.5	5.6	0.5	4.5	0.5	3.3	0.5	2.8	ns
$t_{PHL}$			3.2	0.5	5.6	0.5	4.5	0.5	3.3	0.5	2.8	
$t_{PLH}$	B	A	2.6	0.5	4.1	0.5	3.7	0.5	3.3	0.5	3.2	ns
$t_{PHL}$			2.6	0.5	4.1	0.5	3.7	0.5	3.3	0.5	3.2	
$t_{PZH}$	$\overline{OE}$	A	2.5	0.5	5.3	0.5	5.3	0.5	5.3	0.5	5.3	ns
$t_{PZL}$			2.5	0.5	5.3	0.5	5.3	0.5	5.3	0.5	5.3	
$t_{PZH}$	$\overline{OE}$	B	5.2	0.5	9.4	0.5	7.3	0.5	5.1	0.5	4.5	ns
$t_{PZL}$			5.2	0.5	9.4	0.5	7.3	0.5	5.1	0.5	4.5	
$t_{PHZ}$	$\overline{OE}$	A	3	1	6.1	1	6.1	1	6.1	1	6.1	ns
$t_{PLZ}$			3	1	6.1	1	6.1	1	6.1	1	6.1	
$t_{PHZ}$	$\overline{OE}$	B	5	1	7.9	1	6.6	1	6.1	1	5.2	ns
$t_{PLZ}$			5	1	7.9	1	6.6	1	6.1	1	5.2	

# SN74AVC16T245

## 16-BIT DUAL-SUPPLY BUS TRANSCEIVER

### WITH CONFIGURABLE VOLTAGE TRANSLATION AND 3-STATE OUTPUTS

SCES551C—FEBRUARY 2004—REVISED AUGUST 2005

#### Switching Characteristics

over recommended operating free-air temperature range,  $V_{CCA} = 3.3 \text{ V} \pm 0.3 \text{ V}$  (see [Figure 11](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CCB} = 1.2 \text{ V}$	$V_{CCB} = 1.5 \text{ V} \pm 0.1 \text{ V}$		$V_{CCB} = 1.8 \text{ V} \pm 0.15 \text{ V}$		$V_{CCB} = 2.5 \text{ V} \pm 0.2 \text{ V}$		$V_{CCB} = 3.3 \text{ V} \pm 0.3 \text{ V}$		UNIT
			TYP	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
$t_{PLH}$	A	B	3.2	0.5	5.5	0.5	4.4	0.5	3.2	0.5	2.7	ns
$t_{PHL}$			3.2	0.5	5.5	0.5	4.4	0.5	3.2	0.5	2.7	
$t_{PLH}$	B	A	2.8	0.5	3.7	0.5	3.3	0.5	2.8	0.5	2.7	ns
$t_{PHL}$			2.8	0.5	3.7	0.5	3.3	0.5	2.8	0.5	2.7	
$t_{PZH}$	$\overline{OE}$	A	2.2	0.5	4.3	0.5	4.2	0.5	4.1	0.5	4	ns
$t_{PZL}$			2.2	0.5	4.3	0.5	4.2	0.5	4.1	0.5	4	
$t_{PZH}$	$\overline{OE}$	B	5.1	0.5	9.3	0.5	7.2	0.5	4.9	0.5	4	ns
$t_{PZL}$			5.1	0.5	9.3	0.5	7.2	0.5	4.9	0.5	4	
$t_{PHZ}$	$\overline{OE}$	A	3.4	0.5	5	0.5	5	0.5	5	0.5	5	ns
$t_{PLZ}$			3.4	0.5	5	0.5	5	0.5	5	0.5	5	
$t_{PHZ}$	$\overline{OE}$	B	4.9	1	7.7	1	6.5	1	5.2	0.5	5	ns
$t_{PLZ}$			4.9	1	7.7	1	6.5	1	5.2	0.5	5	

#### Operating Characteristics

$T_A = 25^\circ\text{C}$

PARAMETER			TEST CONDITIONS	$V_{CCA} =$ $V_{CCB} = 1.2 \text{ V}$	$V_{CCA} =$ $V_{CCB} = 1.5 \text{ V}$	$V_{CCA} =$ $V_{CCB} = 1.8 \text{ V}$	$V_{CCA} =$ $V_{CCB} = 2.5 \text{ V}$	$V_{CCA} =$ $V_{CCB} = 3.3 \text{ V}$	UNIT
				TYP	TYP	TYP	TYP	TYP	
$C_{pdA}^{(1)}$	A to B	Outputs enabled	$C_L = 0,$ $f = 10 \text{ MHz},$ $t_r = t_f = 1 \text{ ns}$	1	1	1	1	2	pF
		Outputs disabled		1	1	1	1	1	
	B to A	Outputs enabled		13	13	14	15	16	
		Outputs disabled		1	1	1	1	1	
$C_{pdB}^{(1)}$	A to B	Outputs enabled	$C_L = 0,$ $f = 10 \text{ MHz},$ $t_r = t_f = 1 \text{ ns}$	13	13	14	15	16	pF
		Outputs disabled		1	1	1	1	1	
	B to A	Outputs enabled		1	1	1	1	2	
		Outputs disabled		1	1	1	1	1	

(1) Power dissipation capacitance per transceiver



**Table 1. Typical Total Static Power Consumption ( $I_{CCA} + I_{CCB}$ )**

$V_{CCB}$	$V_{CCA}$						UNIT
	0 V	1.2 V	1.5 V	1.8 V	2.5 V	3.3 V	
0 V	0	<0.5	<0.5	<0.5	<0.5	<0.5	$\mu A$
1.2 V	<0.5	<1	<1	<1	<1	1	
1.5 V	<0.5	<1	<1	<1	<1	1	
1.8 V	<0.5	<1	<1	<1	<1	<1	
2.5 V	<0.5	1	<1	<1	<1	<1	
3.3 V	<0.5	1	<1	<1	<1	<1	

**SN74AVC16T245**  
**16-BIT DUAL-SUPPLY BUS TRANSCEIVER**  
**WITH CONFIGURABLE VOLTAGE TRANSLATION AND 3-STATE OUTPUTS**

SCES551C—FEBRUARY 2004—REVISED AUGUST 2005

**TYPICAL CHARACTERISTICS**

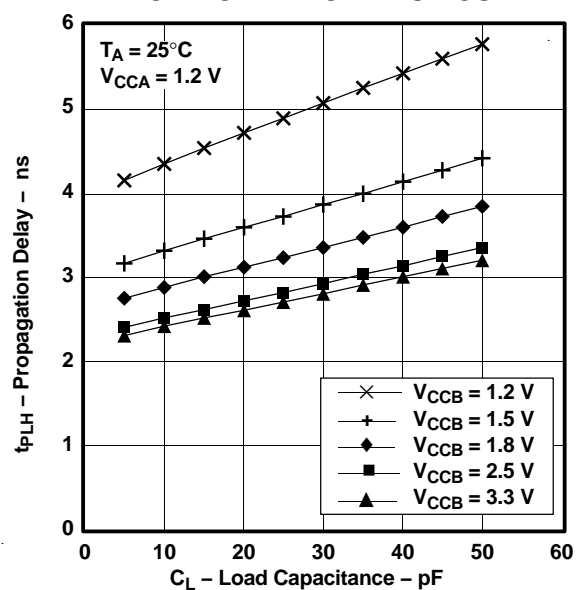


Figure 1.

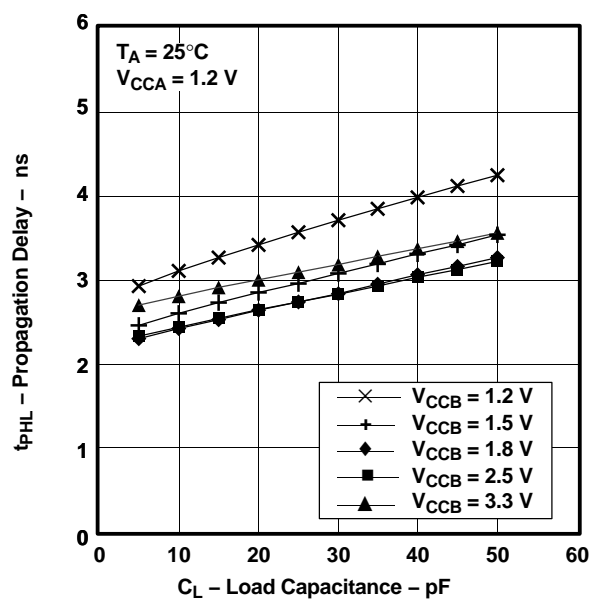


Figure 2.

### TYPICAL CHARACTERISTICS

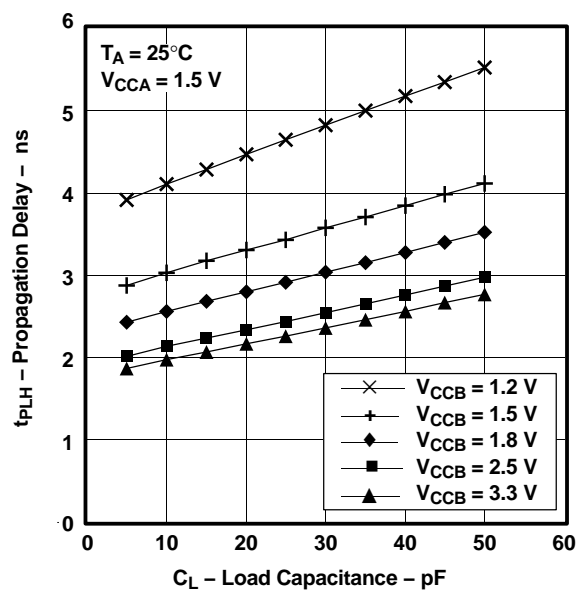


Figure 3.

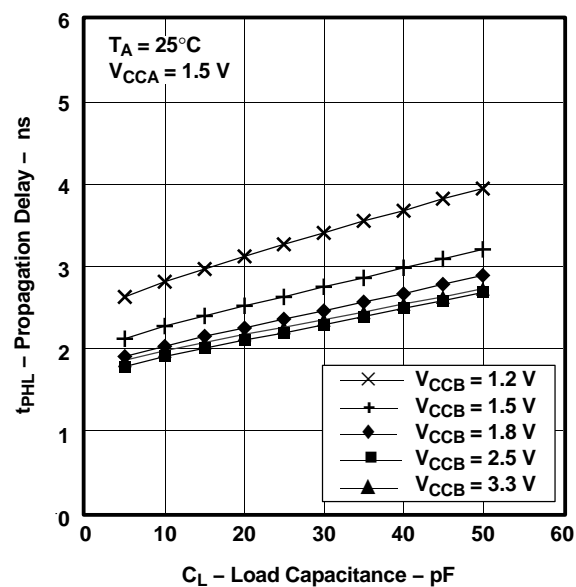


Figure 4.

## TYPICAL CHARACTERISTICS

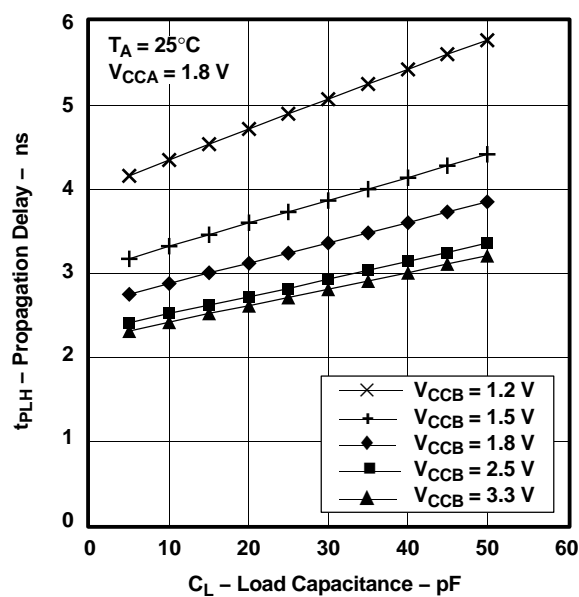


Figure 5.

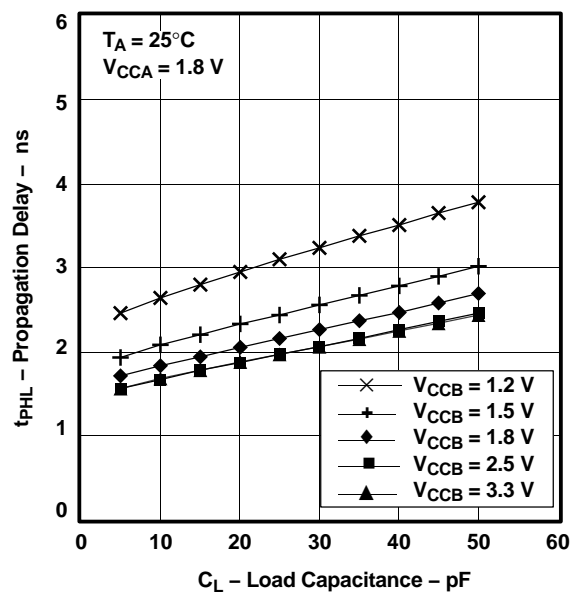


Figure 6.

# TYPICAL CHARACTERISTICS

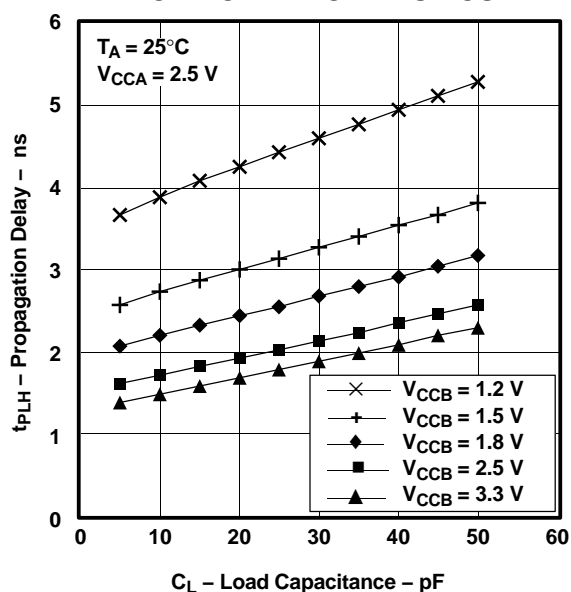


Figure 7.

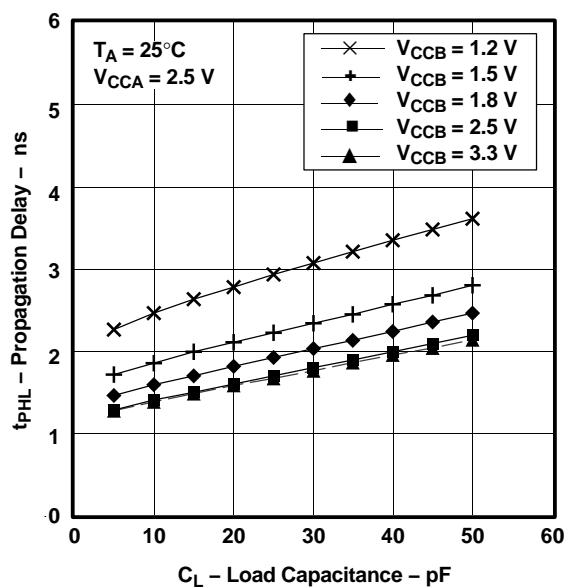


Figure 8.

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**WITH CONFIGURABLE VOLTAGE TRANSLATION AND 3-STATE OUTPUTS**

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**TYPICAL CHARACTERISTICS**

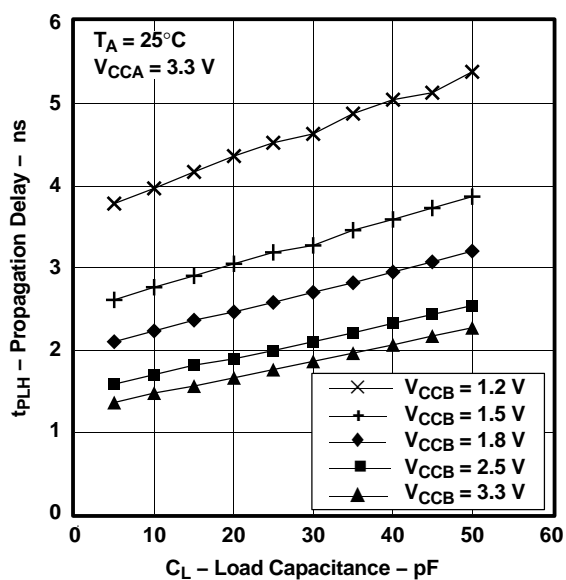


Figure 9.

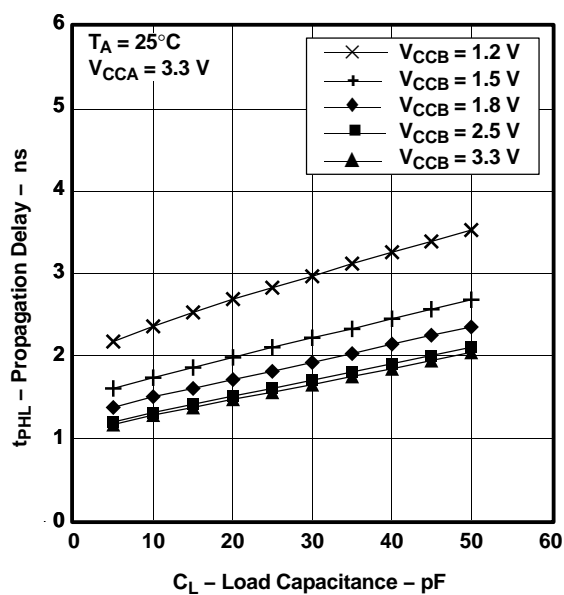
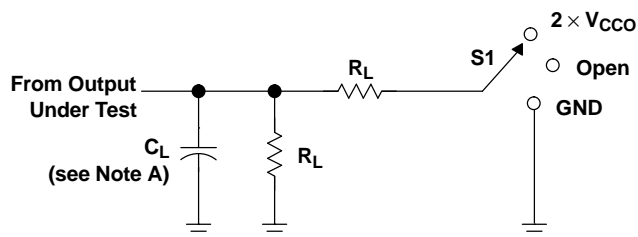


Figure 10.

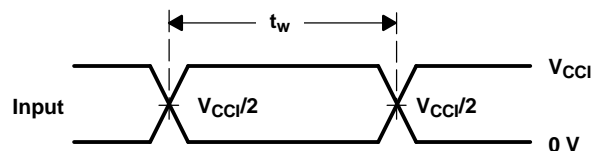
## PARAMETER MEASUREMENT INFORMATION



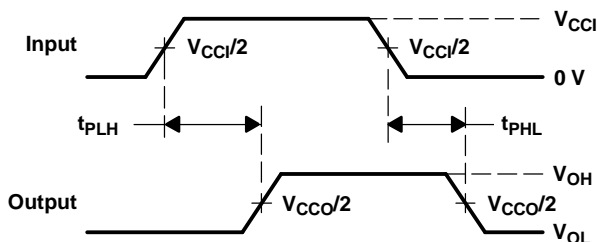
LOAD CIRCUIT

$V_{CCO}$	$C_L$	$R_L$	$V_{TP}$
1.2 V	15 pF	2 k $\Omega$	0.1 V
1.5 V $\pm$ 0.1 V	15 pF	2 k $\Omega$	0.1 V
1.8 V $\pm$ 0.15 V	15 pF	2 k $\Omega$	0.15 V
2.5 V $\pm$ 0.2 V	15 pF	2 k $\Omega$	0.15 V
3.3 V $\pm$ 0.3 V	15 pF	2 k $\Omega$	0.3 V

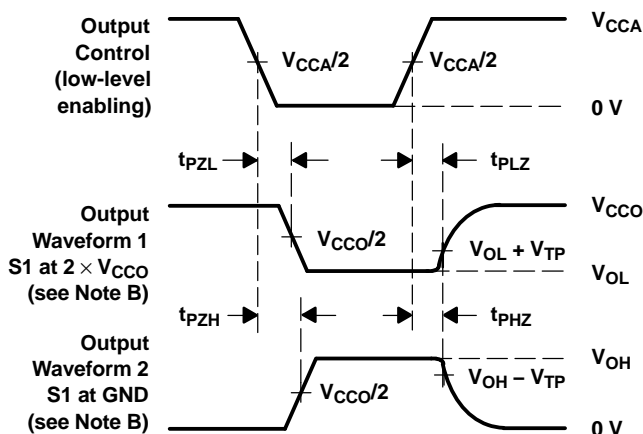
TEST	S1
$t_{pd}$	Open
$t_{PLZ}/t_{PZL}$	$2 \times V_{CCO}$
$t_{PHZ}/t_{PZH}$	GND



VOLTAGE WAVEFORMS  
PULSE DURATION



VOLTAGE WAVEFORMS  
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS  
ENABLE AND DISABLE TIMES

- NOTES:
- $C_L$  includes probe and jig capacitance.
  - Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
  - All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10$  MHz,  $Z_O = 50 \Omega$ ,  $dv/dt \geq 1$  V/ns.
  - The outputs are measured one at a time, with one transition per measurement.
  - $t_{PLZ}$  and  $t_{PHZ}$  are the same as  $t_{dis}$ .
  - $t_{PZL}$  and  $t_{PZH}$  are the same as  $t_{en}$ .
  - $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{pd}$ .
  - $V_{CCI}$  is the  $V_{CC}$  associated with the input port.
  - $V_{CCO}$  is the  $V_{CC}$  associated with the output port.

Figure 11. Load Circuit and Voltage Waveforms

**PACKAGING INFORMATION**

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/Ball Finish	MSL Peak Temp <sup>(3)</sup>
74AVC16T245DGGRE4	ACTIVE	TSSOP	DGG	48	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
74AVC16T245DGGRG4	ACTIVE	TSSOP	DGG	48	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
74AVC16T245DGVRE4	ACTIVE	TVSOP	DGV	48	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
74AVC16T245DGVRG4	ACTIVE	TVSOP	DGV	48	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AVC16T245DGGR	ACTIVE	TSSOP	DGG	48	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AVC16T245DGVR	ACTIVE	TVSOP	DGV	48	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AVC16T245GQLR	NRND	BGA MI CROSTA R JUNI OR	GQL	56	1000	TBD	SNPB	Level-1-240C-UNLIM
SN74AVC16T245ZQLR	ACTIVE	BGA MI CROSTA R JUNI OR	ZQL	56	1000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBsolete:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

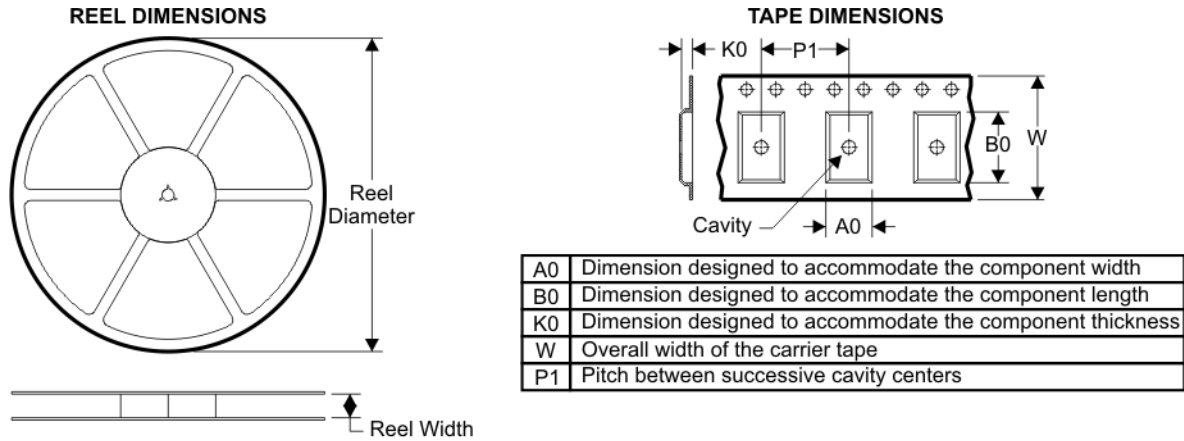
<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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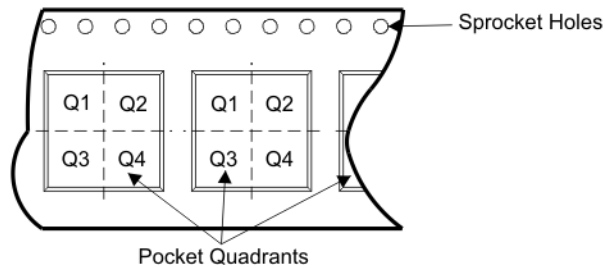
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**TAPE AND REEL BOX INFORMATION**



**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**



Device	Package	Pins	Site	Reel Diameter (mm)	Reel Width (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74AVC16T245DGGR	DGG	48	SITE 41	330	24	8.6	15.8	1.8	12	24	Q1
SN74AVC16T245DGVR	DGV	48	SITE 41	330	24	6.8	10.1	1.6	12	24	Q1
SN74AVC16T245GQLR	GQL	56	SITE 32	330	16	4.8	7.3	1.45	8	16	Q1
SN74AVC16T245GQLR	GQL	56	SITE 60	330	16	4.8	7.3	1.5	8	16	Q1
SN74AVC16T245ZQLR	ZQL	56	SITE 32	330	16	4.8	7.3	1.45	8	16	Q1
SN74AVC16T245ZQLR	ZQL	56	SITE 60	330	16	4.8	7.3	1.5	8	16	Q1

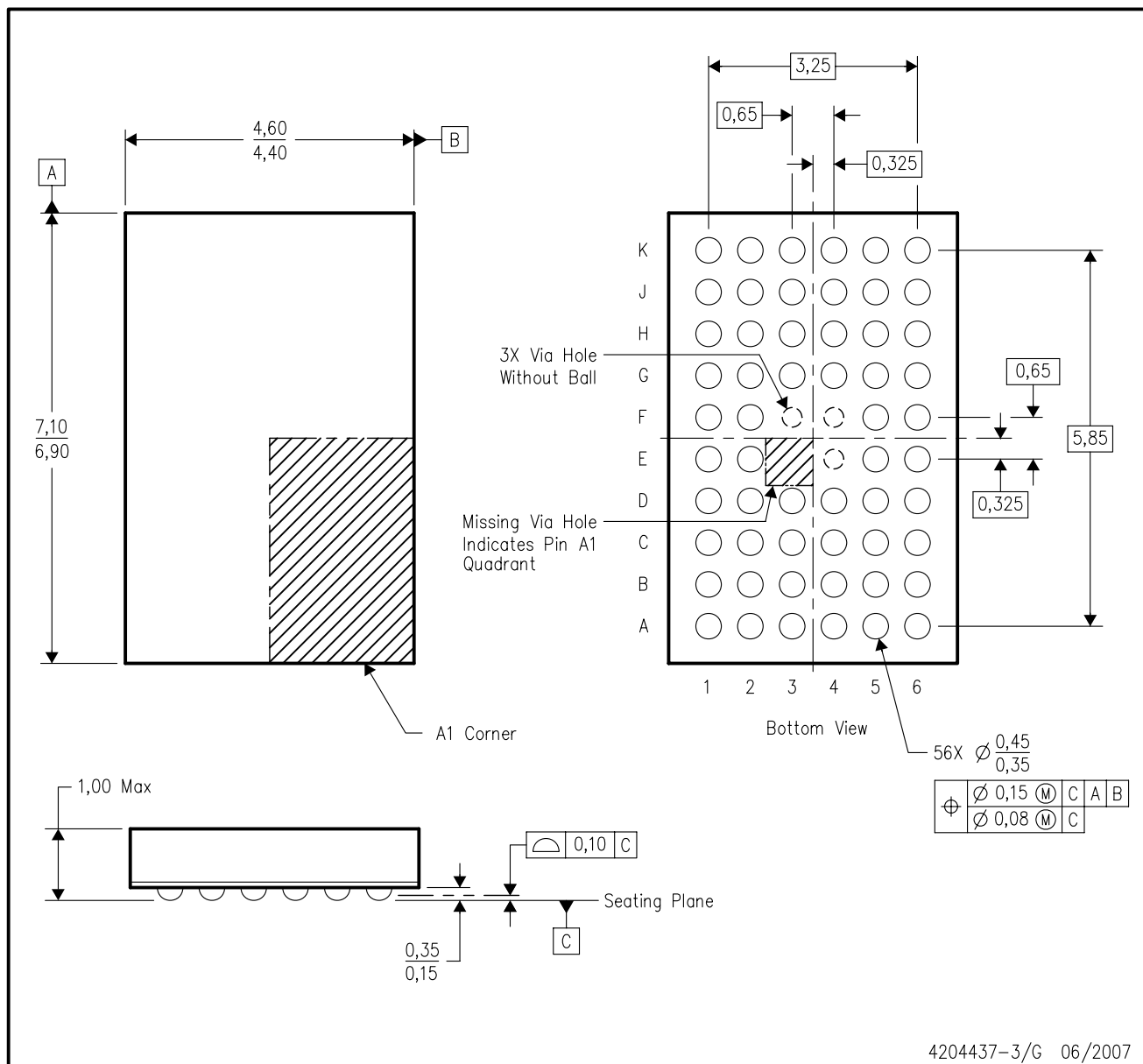
## TAPE AND REEL BOX DIMENSIONS



Device	Package	Pins	Site	Length (mm)	Width (mm)	Height (mm)
SN74AVC16T245DGGR	DGG	48	SITE 41	346.0	346.0	41.0
SN74AVC16T245DGVR	DGV	48	SITE 41	346.0	346.0	41.0
SN74AVC16T245GQLR	GQL	56	SITE 32	346.0	346.0	33.0
SN74AVC16T245GQLR	GQL	56	SITE 60	342.9	345.9	28.58
SN74AVC16T245ZQLR	ZQL	56	SITE 32	346.0	346.0	33.0
SN74AVC16T245ZQLR	ZQL	56	SITE 60	342.9	345.9	28.58

## ZQL (R-PBGA-N56)

## PLASTIC BALL GRID ARRAY

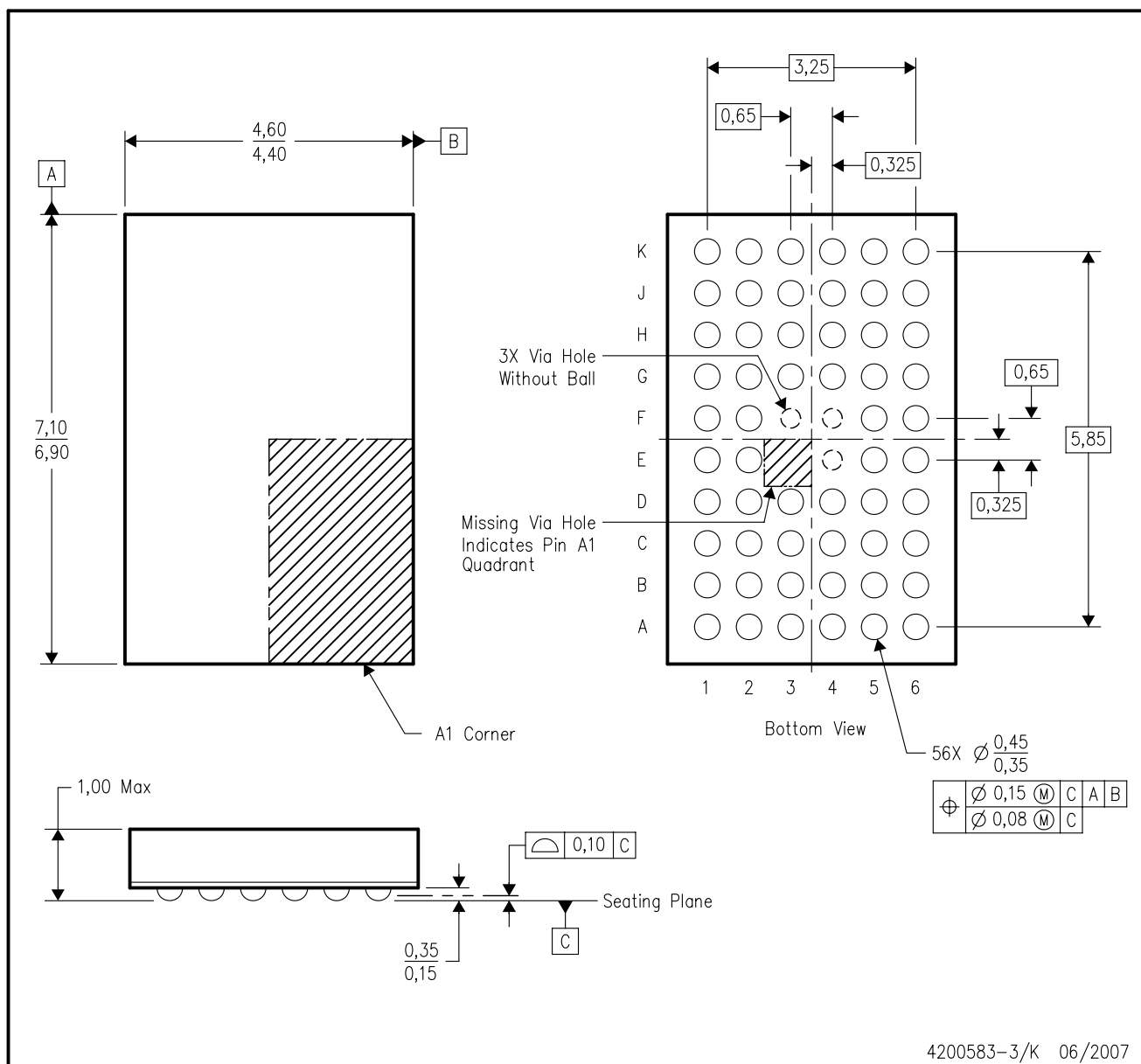


4204437-3/G 06/2007

- NOTES:
- All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
  - This drawing is subject to change without notice.
  - Falls within JEDEC MO-285 variation BA-2.
  - This package is lead-free. Refer to the 56 GQL package (drawing 4200583) for tin-lead (SnPb).

## GQL (R-PBGA-N56)

## PLASTIC BALL GRID ARRAY



4200583-3/K 06/2007

## DGG (R-PDSO-G\*\*)

## PLASTIC SMALL-OUTLINE PACKAGE

48 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold protrusion not to exceed 0,15.  
 D. Falls within JEDEC MO-153

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