- **3-State Bus Driving Inverting Outputs**
- **Buffered Control Inputs**
- **Package Options Include Plastic Small-Outline (DW), Ceramic Chip Carriers (FK), and Standard Plastic (N) and Ceramic (J) 300-mil DIPs**

description

These octal D-type edge-triggered flip-flops feature 3-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. They are particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.
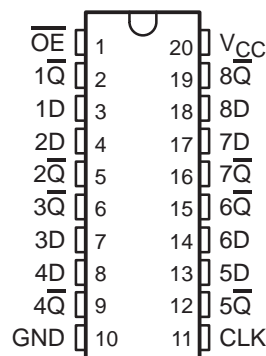
On the positive transition of the clock (CLK) input, the $\overline{Q}$ outputs are set to the complement of the logic states set up at the data (D) inputs. The 'ALS534A and SN74AS534 have inverted outputs, but otherwise are functionally equivalent to the 'ALS374A and SN74AS374.

A buffered output-enable ($\overline{OE}$) input places the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines without interface or pullup components.
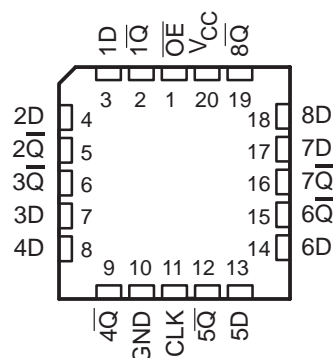
SN54ALS534A . . . J PACKAGE
SN74ALS534A, SN74AS534 . . . DW OR N PACKAGE
(TOP VIEW)

$\overline{OE}$	1	20	V_{CC}
$1\overline{Q}$	2	19	$8\overline{Q}$
1D	3	18	8D
2D	4	17	7D
$2\overline{Q}$	5	16	$7\overline{Q}$
$3\overline{Q}$	6	15	$6\overline{Q}$
3D	7	14	6D
4D	8	13	5D
$4\overline{Q}$	9	12	$5\overline{Q}$
GND	10	11	CLK

SN54ALS534A . . . FK PACKAGE
(TOP VIEW)

Top pins (left to right): 1D, $1\overline{Q}$, $\overline{OE}$, V_{CC}, $8\overline{Q}$ (pins 3, 2, 1, 20, 19)

2D	4	18	8D
$2\overline{Q}$	5	17	7D
$3\overline{Q}$	6	16	$7\overline{Q}$
3D	7	15	$6\overline{Q}$
4D	8	14	6D

Bottom pins (left to right): $4\overline{Q}$, GND, CLK, $5\overline{Q}$, 5D (pins 9, 10, 11, 12, 13)

$\overline{OE}$ does not affect the internal operations of the flip-flops. Old data can be retained or new data can be entered while the outputs are off.

The SN54ALS534A is characterized for operation over the full military temperature range of $-55°C$ to $125°C$. The SN74ALS534A and SN74AS534 are characterized for operation from $0°C$ to $70°C$.

FUNCTION TABLE
(each flip-flop)

INPUTS			OUTPUT
$\overline{OE}$	CLK	D	$\overline{Q}$
L	↑	H	L
L	↑	L	H
L	H or L	X	$\overline{Q}_0$
H	X	X	Z

Copyright © 1996, Texas Instruments Incorporated
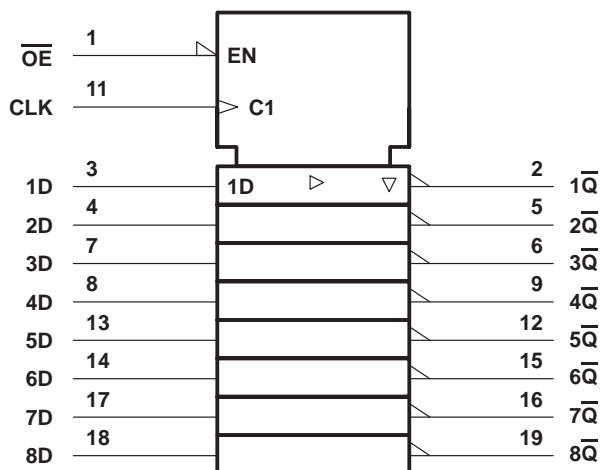
TEXAS INSTRUMENTS

SN54ALS534A, SN74ALS534A, SN74AS534
OCTAL D-TYPE EDGE-TRIGGERED FLIP-FLOPS
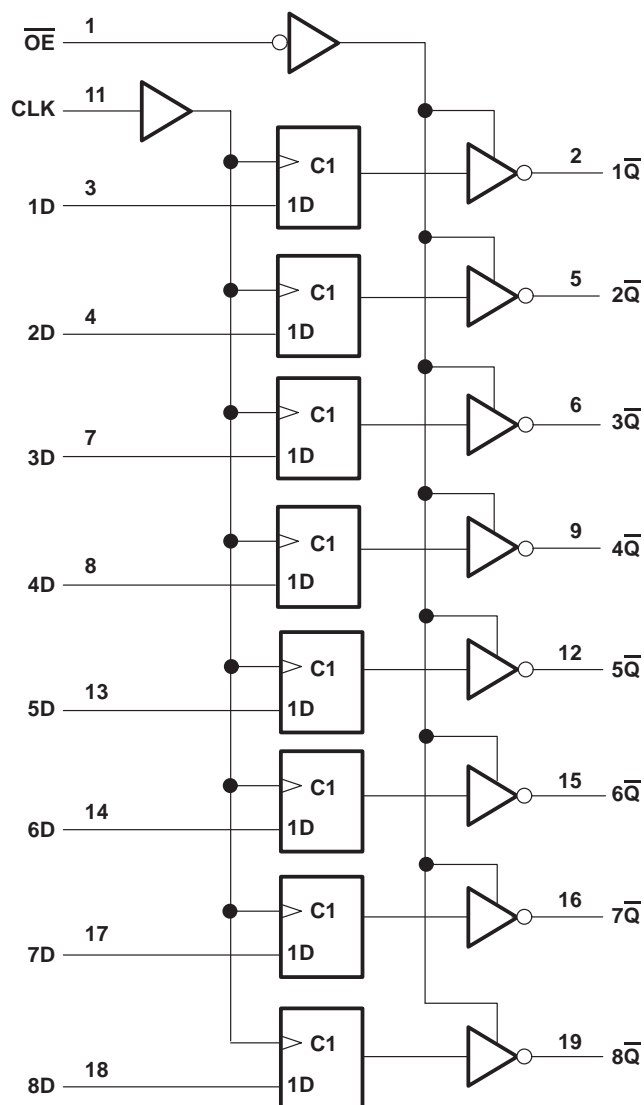## WITH 3-STATE OUTPUTS

SDAS168B – APRIL 1982 – REVISED JULY 1996

logic symbol†

† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC} .... 7 V
Input voltage, V_I .... 7 V
Voltage applied to a disabled 3-state output .... 5.5 V
Operating free-air temperature range, T_A: SN54ALS534A .... −55°C to 125°C
                                   SN74ALS534A .... 0°C to 70°C
Storage temperature range, T_{stg} .... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

		SN54ALS534A			SN74ALS534A			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.7			0.8	V
I_{OH}	High-level output current			−1			−2.6	mA
I_{OL}	Low-level output current			12			24	mA
f_{clock}	Clock frequency	0		30	0		35	MHz
t_w	Pulse duration, CLK high or low	16.5			14			ns
t_{su}	Setup time, data before CLK↑	10			10			ns
t_h	Hold time, data after CLK↑	0			0			ns
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54ALS534A			SN74ALS534A			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}		V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −0.4 mA	V_{CC} −2			V_{CC} −2			V
		V_{CC} = 4.5 V	I_{OH} = −1 mA	2.4	3.3					
			I_{OH} = −2.6 mA				2.4	3.2		
V_{OL}		V_{CC} = 4.5 V	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
			I_{OL} = 24 mA					0.35	0.5	
I_{OZH}		V_{CC} = 5.5 V,	V_O = 2.7 V			20			20	µA
I_{OZL}		V_{CC} = 5.5 V,	V_O = 0.4 V			−20			−20	µA
I_I		V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}		V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	µA
I_{IL}	CLK, $\overline{OE}$	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.1			−0.1	mA
	D					−0.2			−0.2	
I_O§		V_{CC} = 5.5 V,	V_O = 2.25 V	−20		−112	−30		−112	mA
I_{CC}		V_{CC} = 5.5 V	Outputs high		11	19		11	19	mA
			Outputs low		19	28		19	28	
			Outputs disabled		10	31		20	31	

‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.
§ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

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switching characteristics (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX[†]				UNIT
			SN54ALS534A		SN74ALS534A		
			MIN	MAX	MIN	MAX	
f_{max}			30		35		MHz
t_{PLH}	CLK	Any $\overline{Q}$	3	17	3	12	ns
t_{PHL}			4	18	4	16	
t_{PZH}	$\overline{OE}$	Any $\overline{Q}$	3	19	3	17	ns
t_{PZL}			4	20	4	18	
t_{PHZ}	$\overline{OE}$	Any $\overline{Q}$	1	12	1	10	ns
t_{PLZ}			1	25	2	14	

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage, V_{CC} . . . . 7 V
Input voltage, V_I . . . . 7 V
Voltage applied to a disabled 3-state output . . . . 5.5 V
Operating free-air temperature range, T_A: SN74AS534 . . . . 0°C to 70°C
Storage temperature rang, T_{stg} . . . . −65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

			SN74AS534			UNIT
			MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	V
V_{IH}	High-level input voltage		2			V
V_{IL}	Low-level input voltage				0.8	V
I_{OH}	High-level output current				−15	mA
I_{OL}	Low-level output current				48	mA
f_{clock}	Clock frequency		0		125	MHz
t_w	Pulse duration	CLK high	4			ns
		CLK low	3			
t_{su}	Setup time, data before CLK↑		2			ns
t_h	Hold time, data after CLK↑		2			ns
T_A	Operating free-air temperature		0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN74AS534 MIN	TYP†	MAX	UNIT
V_{IK}		$V_{CC} = 4.5$ V,	$I_I = -18$ mA			−1.2	V
V_{OH}		$V_{CC} = 4.5$ V to 5.5 V,	$I_{OH} = -2$ mA	$V_{CC} -2$			V
		$V_{CC} = 4.5$ V,	$I_{OH} = -15$ mA	2.4	3.3		
V_{OL}		$V_{CC} = 4.5$ V,	$I_{OL} = 48$ mA		0.34	0.5	V
I_{OZH}		$V_{CC} = 5.5$ V,	$V_O = 2.7$ V			50	µA
I_{OZL}		$V_{CC} = 5.5$ V,	$V_I = 0.4$ V			−50	µA
I_I		$V_{CC} = 5.5$ V,	$V_I = 7$ V			0.1	mA
I_{IH}		$V_{CC} = 5.5$ V,	$V_I = 2.7$ V			20	µA
I_{IL}	$\overline{OE}$, CLK	$V_{CC} = 5.5$ V,	$V_I = 0.4$ V			−0.5	mA
	D					−2	
I_O‡		$V_{CC} = 5.5$ V,	$V_O = 2.25$ V	−30		−112	mA
I_{CC}		$V_{CC} = 5.5$ V	Outputs high		77	120	mA
			Outputs low		84	128	
			Outputs disabled		84	128	

† All typical values are at $V_{CC} = 5$ V, $T_A = 25°$C.
‡ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.
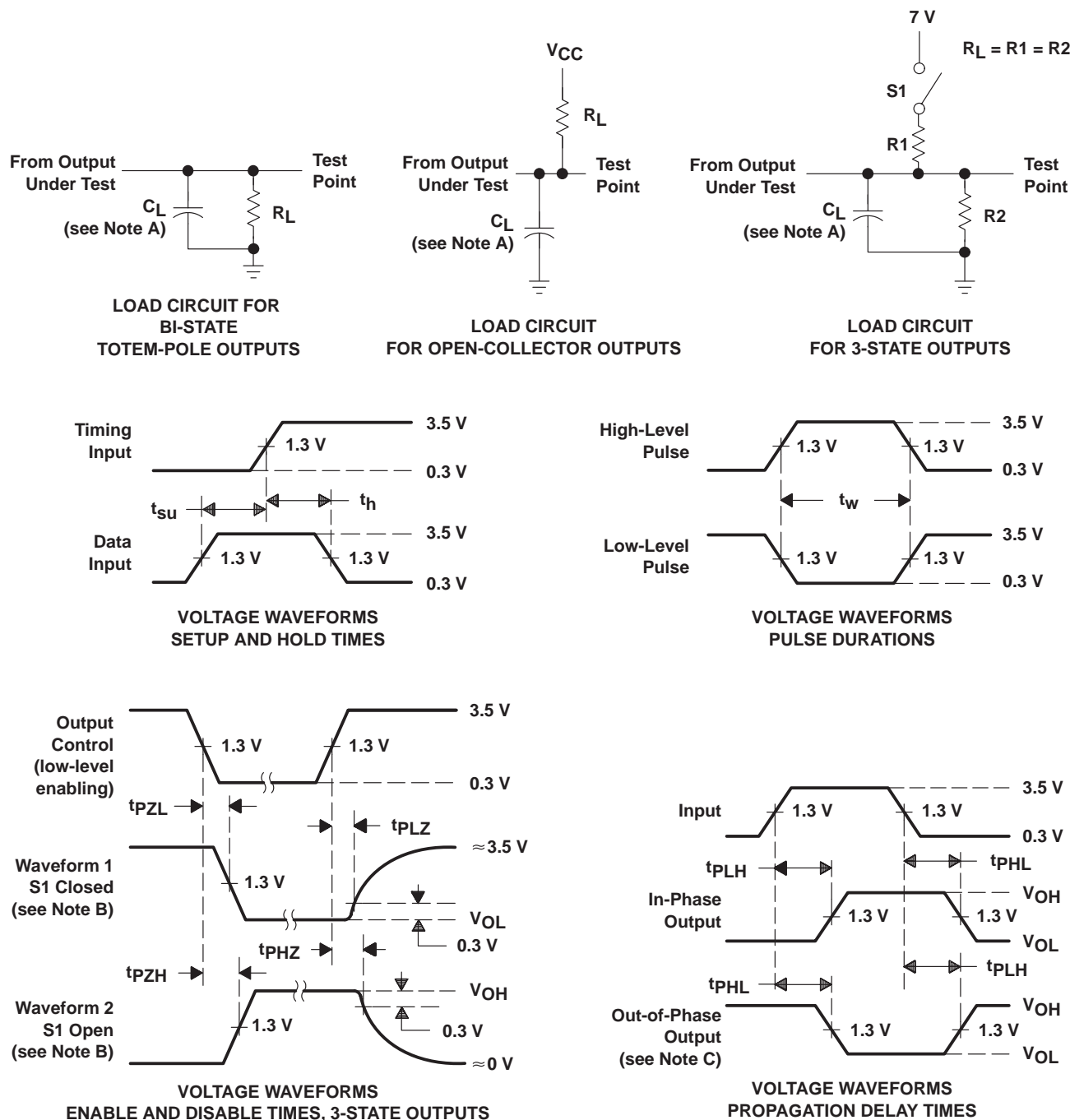
switching characteristics (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 4.5$ V to 5.5 V, $C_L = 50$ pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX§ SN74AS534 MIN	MAX	UNIT
f_{max}			125		MHz
t_{PLH}	CLK	Any $\overline{Q}$	3	8	ns
t_{PHL}			4	9	
t_{PZH}	$\overline{OE}$	Any $\overline{Q}$	2	6	ns
t_{PZL}			3	10	
t_{PHZ}	$\overline{OE}$	Any $\overline{Q}$	2	6	ns
t_{PLZ}			2	6	

§ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

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PARAMETER MEASUREMENT INFORMATION
SERIES 54ALS/74ALS AND 54AS/74AS DEVICES

LOAD CIRCUIT FOR
BI-STATE
TOTEM-POLE OUTPUTS

LOAD CIRCUIT
FOR OPEN-COLLECTOR OUTPUTS

LOAD CIRCUIT
FOR 3-STATE OUTPUTS

VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES

VOLTAGE WAVEFORMS
PULSE DURATIONS

VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES, 3-STATE OUTPUTS

VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES

NOTES: A. C_L includes probe and jig capacitance.
      B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
      C. When measuring propagation delay items of 3-state outputs, switch S1 is open.
      D. All input pulses have the following characteristics: PRR ≤ 1 MHz, $t_r = t_f = 2$ ns, duty cycle = 50%.
      E. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuits and Voltage Waveforms

PACKAGE OPTION ADDENDUM

PACKAGING INFORMATION

Orderable Device	Status [1]	Package Type	Package Drawing	Pins	Package Qty	Eco Plan [2]	Lead/Ball Finish	MSL Peak Temp [3]
SN54ALS534J	OBSOLETE	CDIP	J	20		TBD	Call TI	Call TI
SN74ALS534ADW	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ALS534ADWE4	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ALS534ADWR	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ALS534ADWRE4	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ALS534AN	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN74ALS534AN3	OBSOLETE	PDIP	N	20		TBD	Call TI	Call TI
SN74ALS534ANE4	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN74ALS534ANSR	ACTIVE	SO	NS	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ALS534ANSRE4	ACTIVE	SO	NS	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AS534DW	OBSOLETE	SOIC	DW	20		TBD	Call TI	Call TI
SN74AS534DWR	OBSOLETE	SOIC	DW	20		TBD	Call TI	Call TI
SN74AS534N	OBSOLETE	PDIP	N	20		TBD	Call TI	Call TI
SNJ54ALS534FK	OBSOLETE	LCCC	FK	20		TBD	Call TI	Call TI
SNJ54ALS534J	OBSOLETE	CDIP	J	20		TBD	Call TI	Call TI

[1] The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

[2] Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

[3] MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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J (R—GDIP—T**)   CERAMIC DUAL IN—LINE PACKAGE
14 LEADS SHOWN
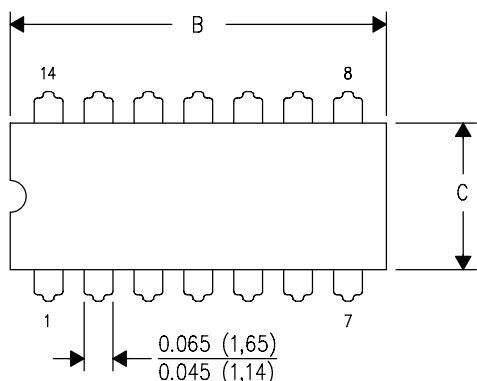
DIM / PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)

B

14   8

1   7

0.065 (1,65)
0.045 (1,14)

C

0.005 (0,13) MIN

0.060 (1,52)
0.015 (0,38)

0.200 (5,08) MAX

Seating Plane

0.130 (3,30) MIN

0.026 (0,66)
0.014 (0,36)

0.100 (2,54)
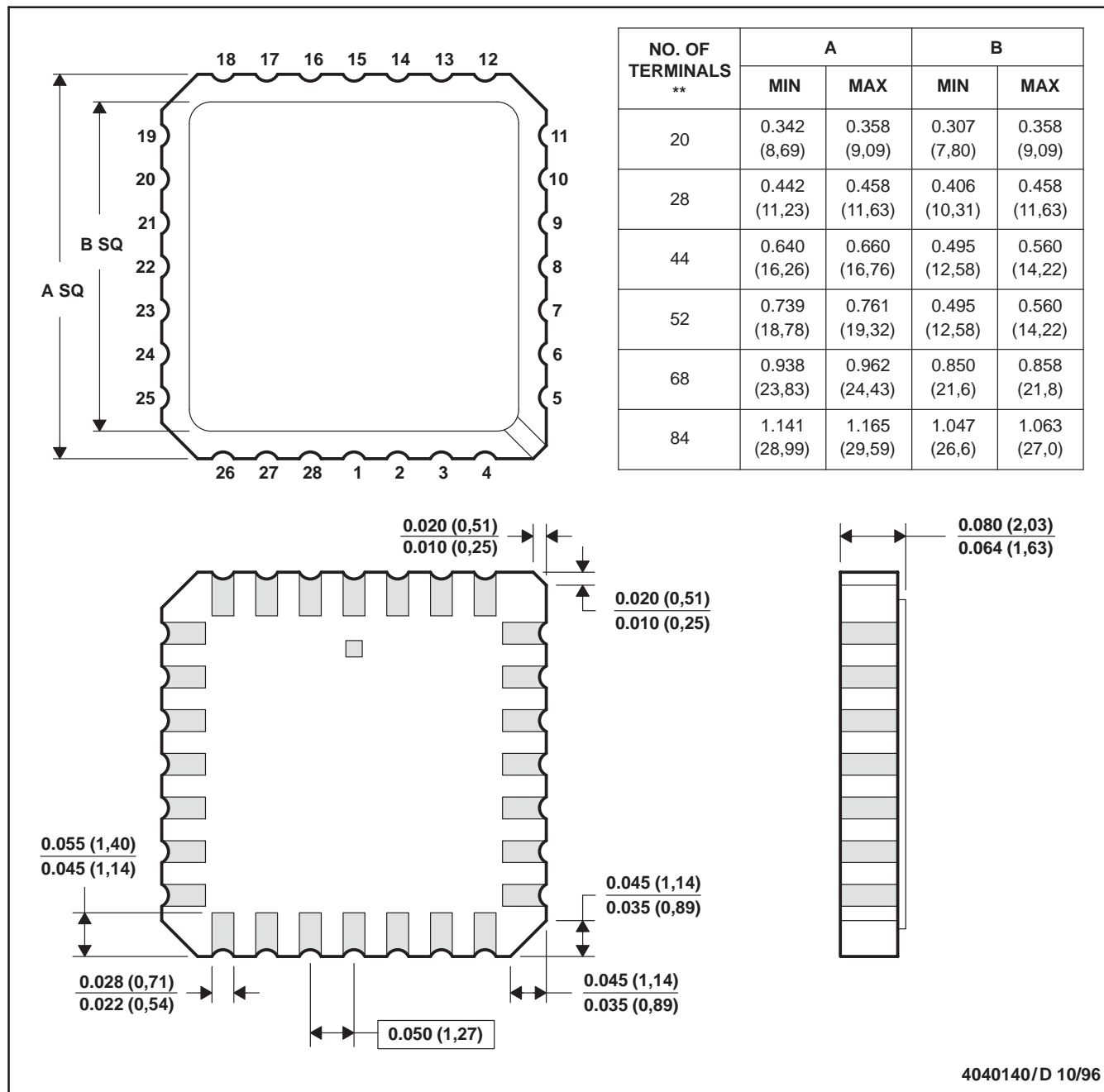
A

0°—15°

0.014 (0,36)
0.008 (0,20)

4040083/F 03/03

NOTES: A. All linear dimensions are in inches (millimeters).
          B. This drawing is subject to change without notice.
          C. This package is hermetically sealed with a ceramic lid using glass frit.
          D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
          E. Falls within MIL STD 1835 GDIP1—T14, GDIP1—T16, GDIP1—T18 and GDIP1—T20.

FK (S-CQCC-N**)

LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN

| NO. OF TERMINALS **	A		B	
	MIN	MAX	MIN	MAX
20	0.342 (8,69)	0.358 (9,09)	0.307 (7,80)	0.358 (9,09)
28	0.442 (11,23)	0.458 (11,63)	0.406 (10,31)	0.458 (11,63)
44	0.640 (16,26)	0.660 (16,76)	0.495 (12,58)	0.560 (14,22)
52	0.739 (18,78)	0.761 (19,32)	0.495 (12,58)	0.560 (14,22)
68	0.938 (23,83)	0.962 (24,43)	0.850 (21,6)	0.858 (21,8)
84	1.141 (28,99)	1.165 (29,59)	1.047 (26,6)	1.063 (27,0)

4040140/D 10/96

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a metal lid.
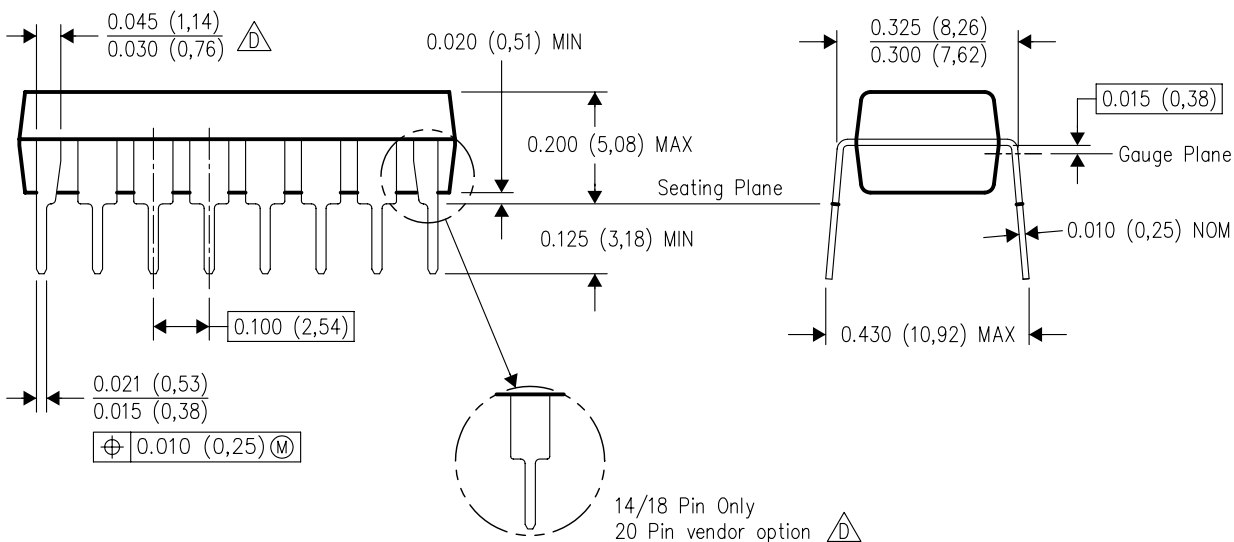D. The terminals are gold plated.
E. Falls within JEDEC MS-004

![Texas Instruments logo] **TEXAS INSTRUMENTS**

N (R–PDIP–T**)   PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN
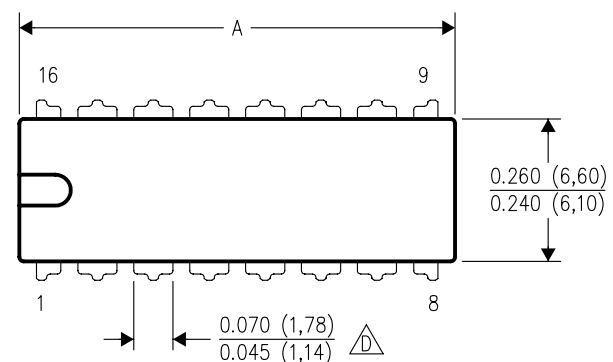
DIM / PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS–001 VARIATION	AA	BB	AC	AD

0.260 (6,60) / 0.240 (6,10)

0.070 (1,78) / 0.045 (1,14)

0.045 (1,14) / 0.030 (0,76)

0.020 (0,51) MIN

0.200 (5,08) MAX

Seating Plane

0.125 (3,18) MIN

0.100 (2,54)

0.021 (0,53) / 0.015 (0,38)

⊕ 0.010 (0,25) Ⓜ

14/18 Pin Only
20 Pin vendor option

0.325 (8,26) / 0.300 (7,62)

0.015 (0,38)

Gauge Plane

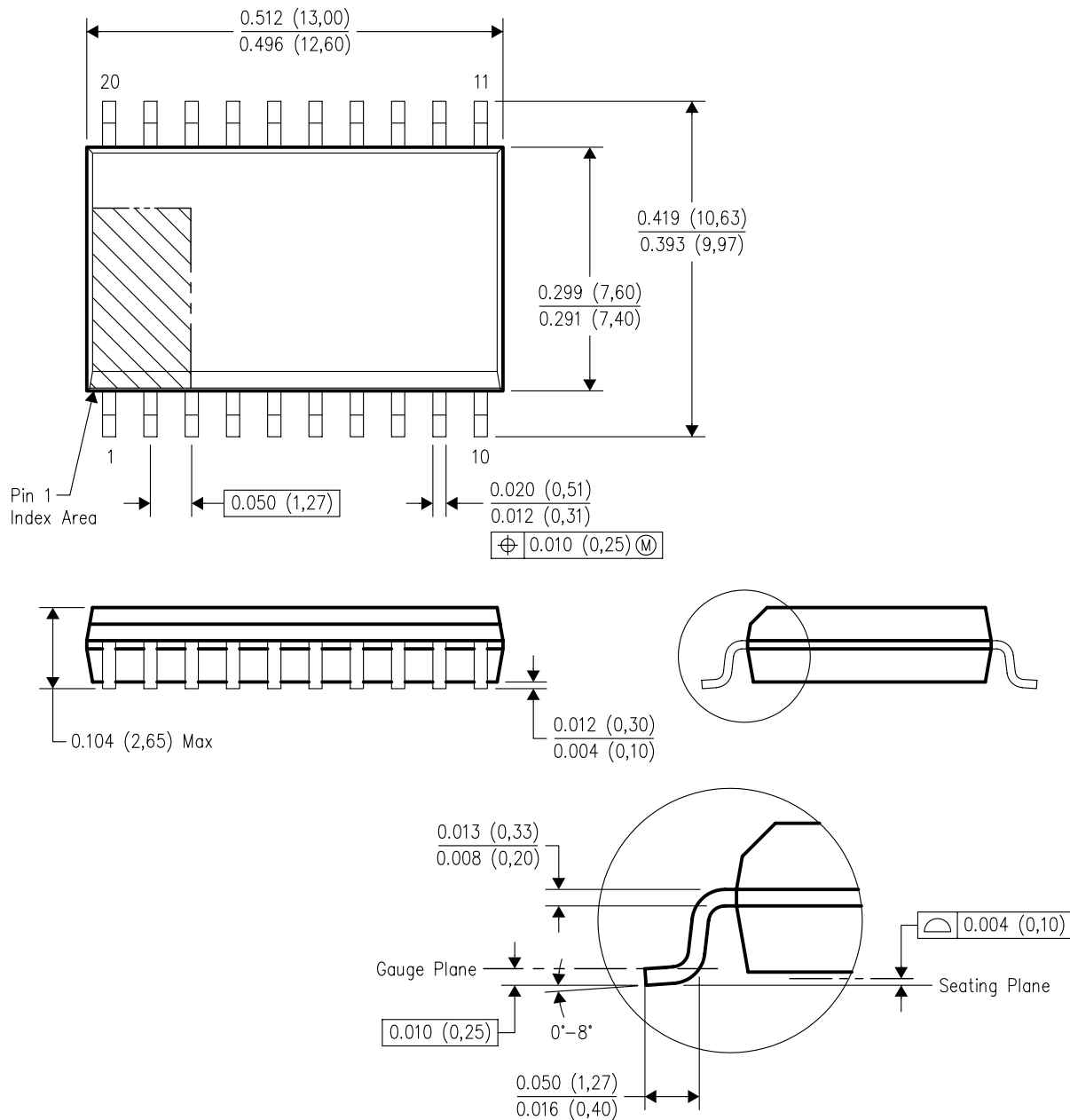0.010 (0,25) NOM

0.430 (10,92) MAX

4040049/E 12/2002

NOTES: A. All linear dimensions are in inches (millimeters).
          B. This drawing is subject to change without notice.
          C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
          D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

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DW (R−PDSO−G20) PLASTIC SMALL−OUTLINE PACKAGE

0.512 (13,00)
0.496 (12,60)

20   11

0.419 (10,63)
0.393 (9,97)

0.299 (7,60)
0.291 (7,40)

1   10

Pin 1
Index Area

0.050 (1,27)

0.020 (0,51)
0.012 (0,31)

⊕ 0.010 (0,25) Ⓜ

0.104 (2,65) Max

0.012 (0,30)
0.004 (0,10)

0.013 (0,33)
0.008 (0,20)

Gauge Plane

0.004 (0,10)

Seating Plane

0.010 (0,25)

0°−8°

0.050 (1,27)
0.016 (0,40)

4040000−4/F 06/2004

NOTES: A. All linear dimensions are in inches (millimeters).
         B. This drawing is subject to change without notice.
         C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
         D. Falls within JEDEC MS−013 variation AC.

NS (R-PDSO-G)**   PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN

PINS ** DIM	14	16	20	24
A MAX	10,50	10,50	12,90	15,30
A MIN	9,90	9,90	12,30	14,70

4040062/C 03/03

NOTES: A.   All linear dimensions are in millimeters.
         B.   This drawing is subject to change without notice.
         C.   Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

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