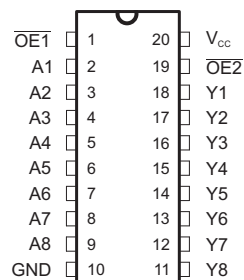


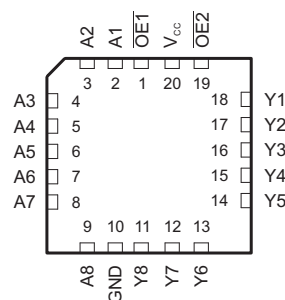
FEATURES

- State-of-the-Art *EPIC-IIB™* BiCMOS Design Significantly Reduces Power Dissipation
- Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17
- Typical V_{OLP} (Output Ground Bounce) < 1 V at $V_{CC} = 5$ V, $T_A = 25^\circ\text{C}$
- High-Impedance State During Power Up and Power Down
- High-Drive Outputs ($-32\text{-mA } I_{OH}$, $64\text{-mA } I_{OL}$)
- Package Options Include Plastic Small-Outline (DW), Shrink Small-Outline (DB), and Thin Shrink Small-Outline (PW) Packages, Ceramic Chip Carriers (FK), Ceramic Flat (W) Package, and Plastic (N) and Ceramic (J) DIPs

SN54ABT541...J OR W PACKAGE
SN74ABT541B...DB, DW, N, OR PW PACKAGE
(TOP VIEW)



SN54ABT541...FK PACKAGE
(TOP VIEW)



DESCRIPTION/ORDERING INFORMATION

The SN54ABT541 and SN74ABT541B octal buffers and line drivers are ideal for driving bus lines or buffering memory address registers. The devices feature inputs and outputs on opposite sides of the package to facilitate printed circuit board layout.

ORDERING INFORMATION

T_A	PACKAGE ⁽¹⁾		ORDERABLE PART NUMBER	TOP-SIDE MARKING
-40°C to 85°C	PDIP – N	Reel of 1000	SN74ABT541BN	SN74ABT541BN
		Tube of 25	SN74ABT541BDW	ABT541B
	SOIC – DW	Reel of 2000	SN74ABT541BDWR	
		Reel of 2000	SN74ABT541BDBR	AB541B
	SSOP – DB	Reel of 2000	SN74ABT541BDBRG4	
-55°C to 125°C	TSSOP – PW	Reel of 1050	SN74ABT541BPW	AB541B
		Reel of 2000	SN74ABT541BPWR	
	CDIP – J	Reel of 1000	SNJ54ABT541J	SNJ54ABT541J
	CFP – W	Reel of 510	SNJ54ABT541W	SNJ54ABT541W
	LCCC – FK	Reel of 2200	SNJ54ABT541FK	SNJ54ABT541FK

(1) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.



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EPIC-IIB is a trademark of Texas Instruments.

DESCRIPTION/ORDERING INFORMATION (CONTINUED)

The 3-state control gate is a two-input AND gate with active-low inputs so that if either output-enable ($\overline{OE1}$ or $\overline{OE2}$) input is high, all eight outputs are in the high-impedance state.

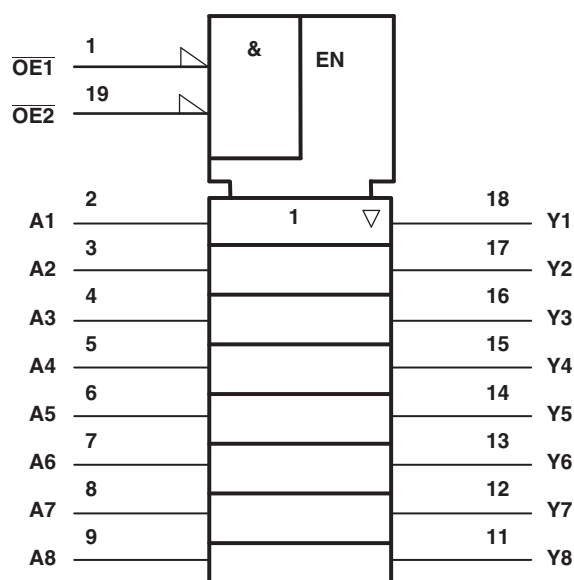
When VCC is between 0 and 2.1 V, the device is in the high-impedance state during power up or power down. However, to ensure the high-impedance state above 2.1 V, $\overline{OE}$ should be tied to VCC through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN54ABT541 is characterized for operation over the full military temperature range of -55°C to 125°C . The SN74ABT541B is characterized for operation from -40°C to 85°C .

FUNCTION TABLE

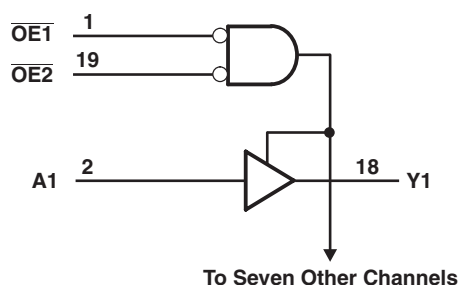
INPUTS			OUTPUTS Y
$\overline{OE1}$	$\overline{OE2}$	A	
L	L	L	L
L	L	H	H
H	X	X	Z
X	H	X	Z

LOGIC SYMBOL⁽¹⁾



(1) This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

LOGIC DIAGRAM (POSITIVE LOGIC)



Absolute Maximum Ratings⁽¹⁾

over recommended operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_{CC}	Supply voltage range	–0.5	7	V
V_I	Input voltage range ⁽²⁾	–0.5	7	V
V_O	Voltage range applied to any output in the high or power-off state	–0.5	5.5	V
I_O	Current into any output in the low state	SN54ABT541	96	mA
		SN74ABT541B	128	
I_{IK}	Input clamp current	$V_I < 0$	–18	mA
I_{OK}	Output clamp current	$V_O < 0$	–50	mA
θ_{JA}	Package thermal impedance ⁽³⁾	DB package	115	°C/W
		DW package	97	
		N package	67	
		PW package	128	
T_{stg}	Storage temperature range	–65	150	°C

(1) Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

(3) The package thermal impedance is calculated in accordance with JESD 51, except for through-hole packages, which use a trace length of zero.

Recommended Operating Conditions⁽¹⁾

over recommended operating free-air temperature range (unless otherwise noted)

		SN54ABT541		SN74ABT541B		UNIT
		MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage	4.5	5.5	4.5	5.5	V
V_{IH}	High-level input voltage	2		2		V
V_{IL}	Low-level input voltage		0.8		0.8	V
I_{OH}	High-level output current		–24		–32	mA
I_{OL}	Low-level output current		48		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate		5		5	ns/V
$\Delta t/\Delta V_{CC}$	Power-up ramp rate			200		μs/V
T_A	Operating free-air temperature	–55	125	–40	85	°C

(1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

SN54ABT541, SN74ABT541B

OCTAL BUFFERS/DRIVERS

WITH 3-STATE OUTPUTS

SCBS093L – DECEMBER 1993 – REVISED DECEMBER 2006

Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		T _A = 25°C			SN54ABT51		SN74ABT541B		UNIT
			MIN	TYP ⁽¹⁾	MAX	MIN	MAX	MIN	MAX	
V _{IK}	V _{CC} = 4.5 V,	I _I = –18 mA			–1.2		–1.2		–1.2	V
V _{OH}	V _{CC} = 4.5 V,	I _{OH} = –3 mA	2.5			2.5		2.5		V
	V _{CC} = 5 V,	I _{OH} = –3 mA	3			3		3		
	V _{CC} = 4.5 V,	I _{OH} = –24 mA	2			2				
		I _{OH} = –32 mA	2 ⁽²⁾					2		
V _{OL}	V _{CC} = 4.5 V,	I _{OL} = 48 mA			0.55		0.55			VV
		I _{OL} = 64 mA			0.55 ⁽²⁾				0.55	
V _{hys}				100						mV
I _I	V _{CC} = 5.5 V,	V _I = V _{CC} or GND			±1		±1		±1	μA
I _{OZPU}	V _{CC} = 0 to 2.1 V, V _O = 0.5 V to 2.7 V, $\overline{OE}$ = X				±50 ⁽³⁾		±50 ⁽³⁾		±50	μA
I _{OZPD}	V _{CC} = 2.1 V to 0, V _O = 0.5 V to 2.7 V, $\overline{OE}$ = X				±50 ⁽³⁾		±50 ⁽³⁾		±50	μA
I _{OZH}	V _{CC} = 5.5 V,	V _O = 2.7 V			10		10		10	μA
I _{OZL}	V _{CC} = 5.5 V,	V _O = 0.5 V			–10		–10		–10	μA
I _{off}	V _{CC} = 0 V,	V _I or V _O ≤ 4.5 V			±100				±100	μA
I _{CEX}	V _{CC} = 5.5 V, V _O = 5.5 V,	Outputs high			50				50	μA
I _O	V _{CC} = 5.5 V ⁽⁴⁾ ,	V _O = 2.5 V	–50	–140	–180	–50	–180	–50	–180	mA
I _{CC}	V _{CC} = 5.5 V, I _O = 0 V, V _I = V _{CC} or GND	Outputs high		5	250		250		250	μA
		Outputs low		22	30		30		30	mA
		Outputs disabled		1	250		250		250	μA
ΔI _{CC}	V _{CC} = 5.5 V, One input at 3.4 V, Other inputs at V _{CC} or GND ⁽⁵⁾	Outputs enabled			1.5		1.5		1.5	mA
		Outputs disabled			50		50		50	μA
		Control Inputs			1.5		1.2		1.5	mA
C _i	V _I = 2.5 V or 0.5 V			3						pF
C _o	V _O = 2.5 V or 0.5 V			6						pF

(1) All typical values are at V_{CC} = 5 V.

(2) On products compliant to MIL-PRF-38535, this parameter does not apply.

(3) On products compliant to MIL-PRF-38535, this parameter is not production tested.

(4) Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

(5) This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

Switching Characteristics, SN54ABT541

over recommended ranges of supply voltage and operating free-air temperature, $C_L = 50$ pF (unless otherwise noted)
(see [Figure 1](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	VCC = 5 V, TA = 25°C					UNIT
			MIN	TYP	MAX	MIN	MAX	
t_{PLH}	A	Y	1	2.6	4.1	1	4.6	ns
t_{PHL}			1	2.9	4.2	1	4.7	
t_{PZH}	$\overline{OE}$	Y	1.1	3.1	4.8	1.1	5.4	ns
t_{PZL}			2.1	4.4	5.9	2.1	7	
t_{PHZ}	$\overline{OE}$	Y	2.1	5.1	6.6	2.1	7.5	ns
t_{PLZ}			1.7	4.7	6.2	1.7	6.7	

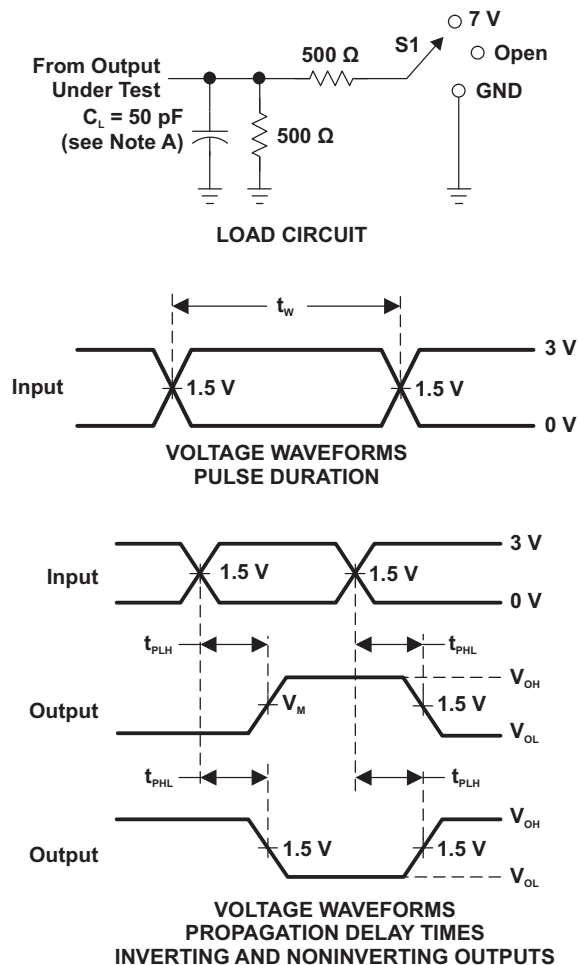
Switching Characteristics, SN74ABT541B

over recommended ranges of supply voltage and operating free-air temperature, $C_L = 50$ pF (unless otherwise noted)
(see [Figure 1](#))

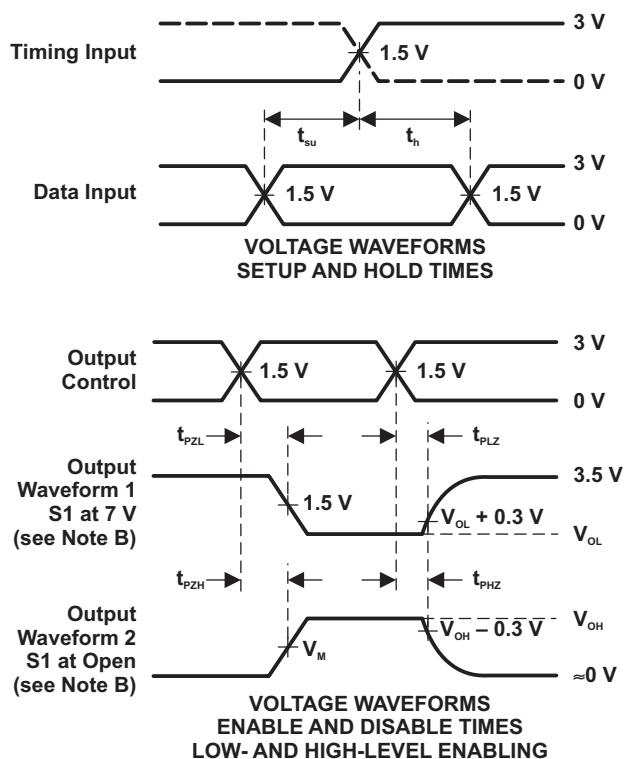
PARAMETER	FROM (INPUT)	TO (OUTPUT)	VCC = 5 V, TA = 25°C					UNIT
			MIN	TYP	MAX	MIN	MAX	
t_{PLH}	A	Y	1	2	3.2	1	3.9	ns
t_{PHL}			1	2.6	3.5	1	3.9	
t_{PZH}	$\overline{OE}$	Y	2	3.5	4.5	2	4	ns
t_{PZL}			1.9	4	5.1	1.9	5.9	
t_{PHZ}	$\overline{OE}$	Y	2.2	4.4	5.4	2.2	5.8	ns
t_{PLZ}			1.5	3	4	1.5	4.4	
$t_{sk(o)}^{(1)}$					0.5		0.5	ns

(1) Skew between any two outputs of the same package switching in the same direction.

PARAMETER MEASUREMENT INFORMATION



TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	Open



- NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_o = 50 \Omega$, $t_r \leq 2.5 \text{ ns}$, $t_f \leq 2.5 \text{ ns}$.
D. The outputs are measured one at a time, with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
5962-9471801Q2A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type
5962-9471801QRA	ACTIVE	CDIP	J	20	1	TBD	A42 SNPB	N / A for Pkg Type
5962-9471801QSA	ACTIVE	CFP	W	20	1	TBD	A42	N / A for Pkg Type
SN74ABT541BDBLE	OBSOLETE	SSOP	DB	20		TBD	Call TI	Call TI
SN74ABT541BDBR	ACTIVE	SSOP	DB	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ABT541BDBRE4	ACTIVE	SSOP	DB	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ABT541BDBRG4	ACTIVE	SSOP	DB	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ABT541BDW	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ABT541BDWE4	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ABT541BDWR	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ABT541BDWRE4	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ABT541BN	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN74ABT541BNE4	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN74ABT541BNSR	ACTIVE	SO	NS	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ABT541BNSRE4	ACTIVE	SO	NS	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ABT541BPW	ACTIVE	TSSOP	PW	20	70	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ABT541BPWE4	ACTIVE	TSSOP	PW	20	70	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ABT541BPWLE	OBSOLETE	TSSOP	PW	20		TBD	Call TI	Call TI
SN74ABT541BPWR	ACTIVE	TSSOP	PW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ABT541BPWRE4	ACTIVE	TSSOP	PW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SNJ54ABT541FK	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type
SNJ54ABT541J	ACTIVE	CDIP	J	20	1	TBD	A42 SNPB	N / A for Pkg Type
SNJ54ABT541W	ACTIVE	CFP	W	20	1	TBD	A42	N / A for Pkg Type

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

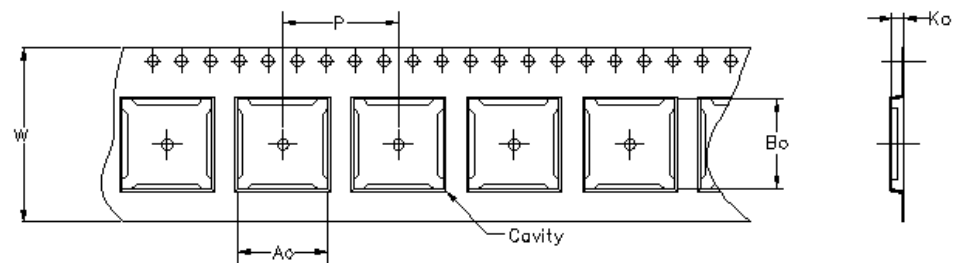
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

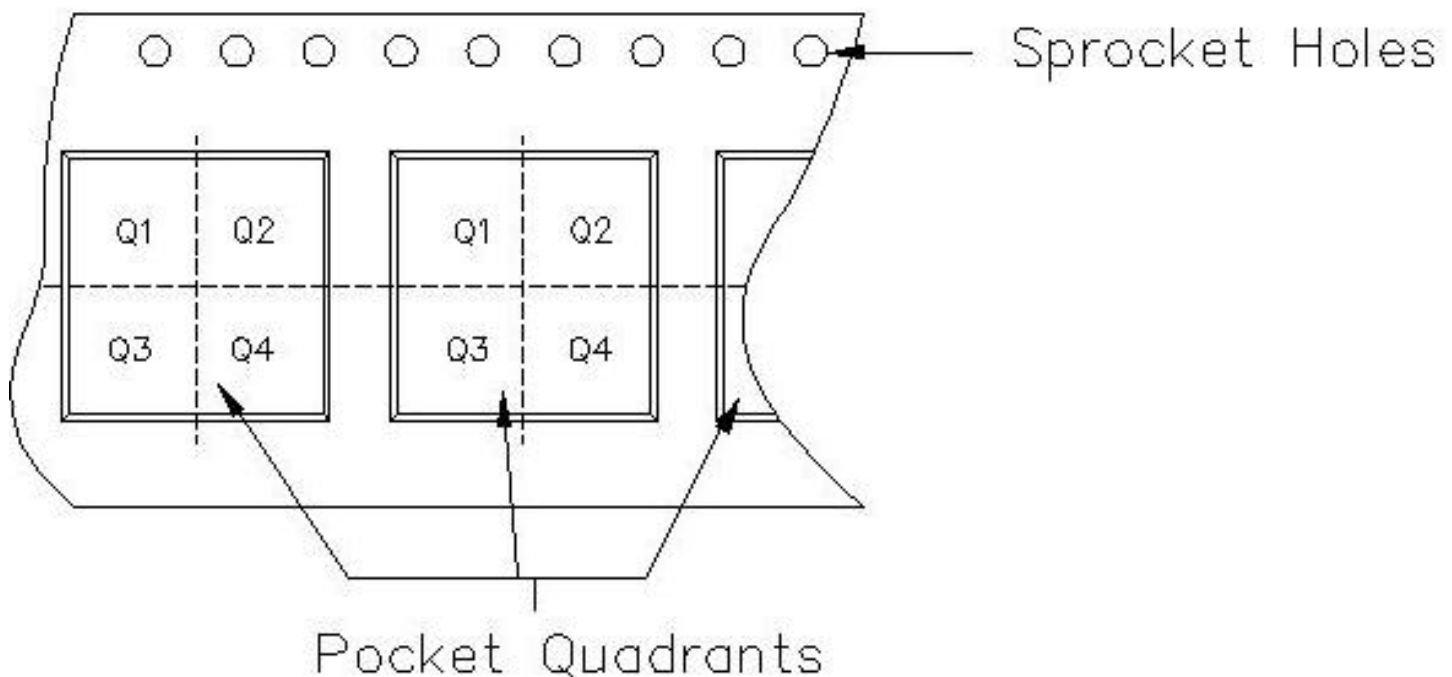
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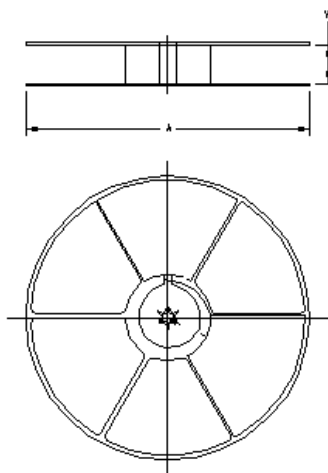
Carrier tape design is defined largely by the component length, width, and thickness.

A_o = Dimension designed to accommodate the component width.
B_o = Dimension designed to accommodate the component length.
K_o = Dimension designed to accommodate the component thickness.
W = Overall width of the carrier tape.
P = Pitch between successive cavity centers.



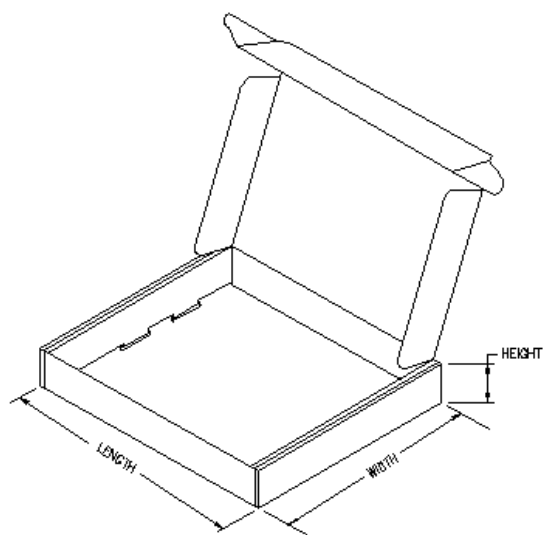
TAPE AND REEL INFORMATION

Device	Package	Pins	Site	Reel Diameter (mm)	Reel Width (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74ABT541BDBR	DB	20	MLA	330	16	8.2	7.5	2.5	12	16	Q1
SN74ABT541BDWR	DW	20	MLA	330	24	10.8	13.0	2.7	12	24	Q1
SN74ABT541BNSR	NS	20	MLA	330	24	8.2	13.0	2.5	12	24	Q1
SN74ABT541BPWR	PW	20	MLA	330	16	6.95	7.1	1.6	8	16	Q1



TAPE AND REEL BOX INFORMATION

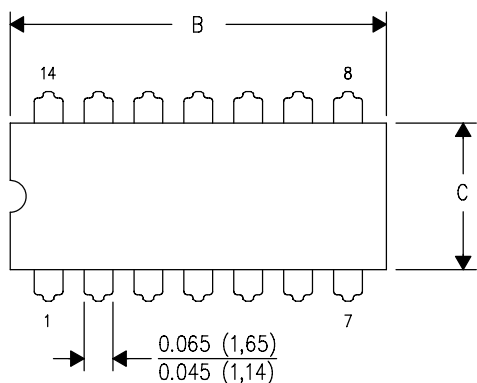
Device	Package	Pins	Site	Length (mm)	Width (mm)	Height (mm)
SN74ABT541BDBR	DB	20	MLA	333.2	333.2	28.58
SN74ABT541BDWR	DW	20	MLA	333.2	333.2	31.75
SN74ABT541BNSR	NS	20	MLA	333.2	333.2	31.75
SN74ABT541BPWR	PW	20	MLA	333.2	333.2	28.58



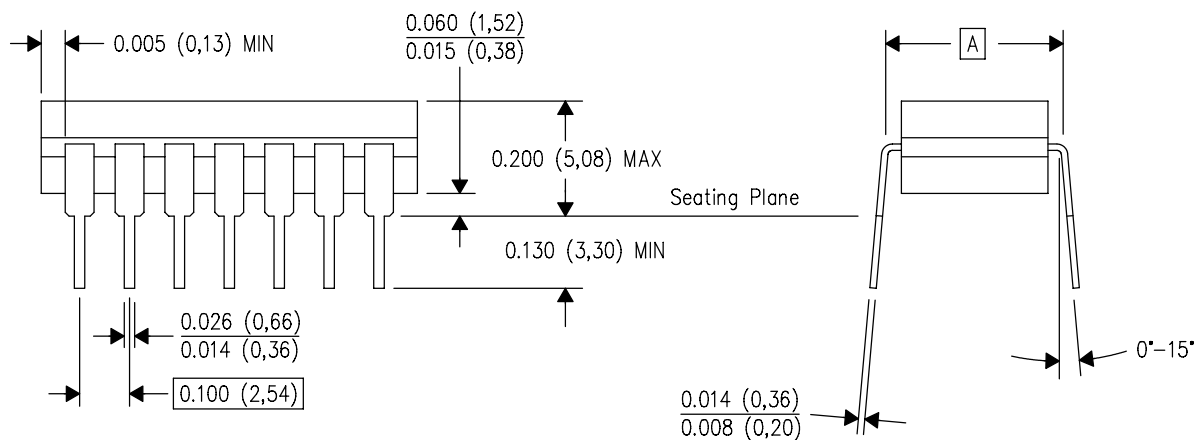
J (R-GDIP-T**)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



PINS ** DIM	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)

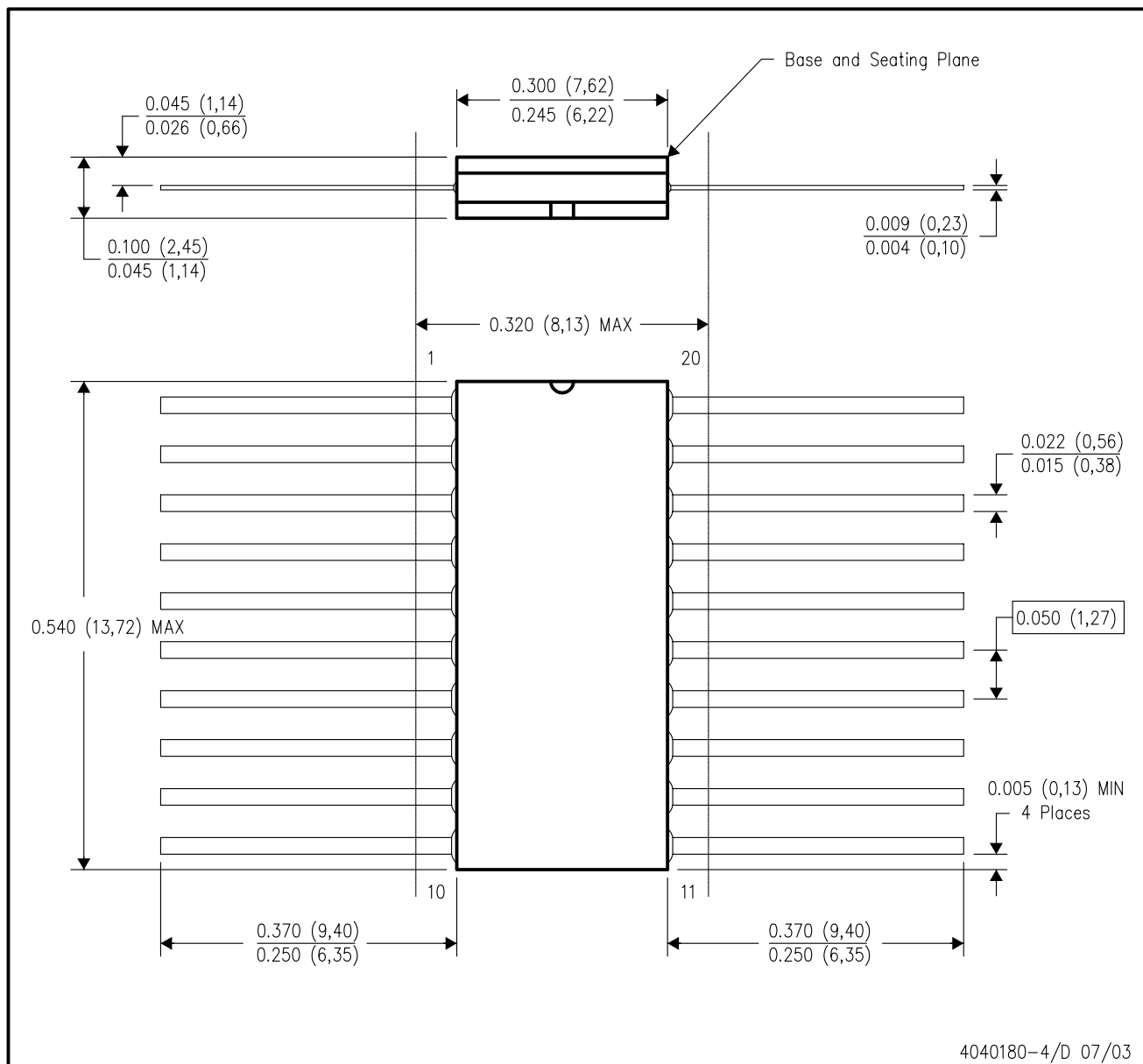


4040083/F 03/03

- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. This package is hermetically sealed with a ceramic lid using glass frit.
 - D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
 - E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

W (R-GDFP-F20)

CERAMIC DUAL FLATPACK

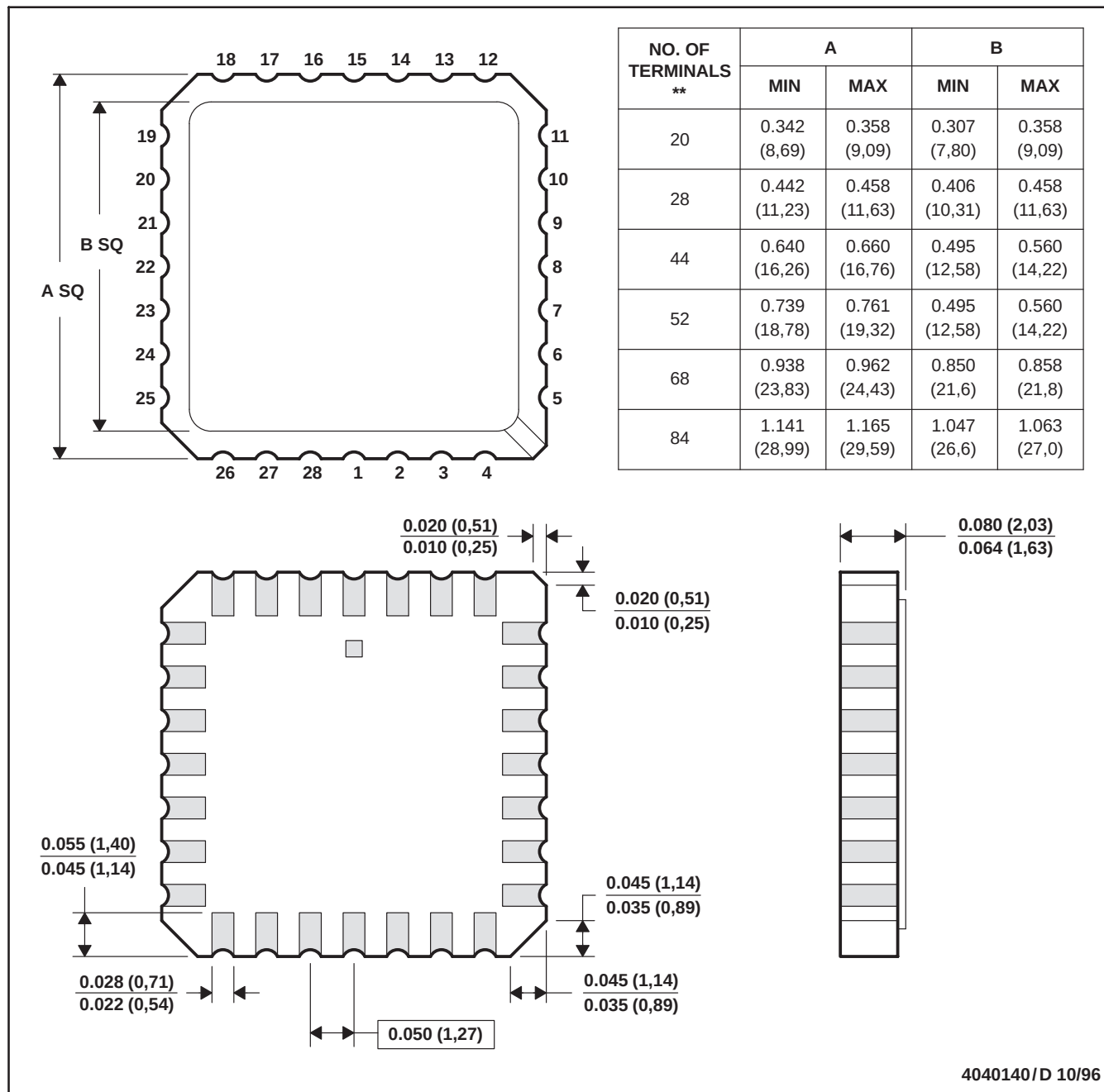


- NOTES:
- All linear dimensions are in inches (millimeters).
 - This drawing is subject to change without notice.
 - This package can be hermetically sealed with a ceramic lid using glass frit.
 - Index point is provided on cap for terminal identification only.
 - Falls within Mil-Std 1835 GDFP2-F20

FK (S-CQCC-N**)

LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN

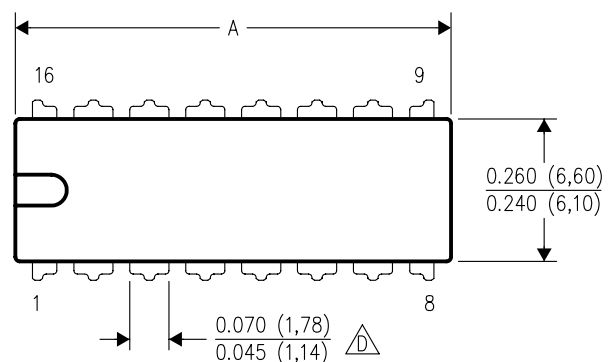


- NOTES:
- All linear dimensions are in inches (millimeters).
 - This drawing is subject to change without notice.
 - This package can be hermetically sealed with a metal lid.
 - The terminals are gold plated.
 - Falls within JEDEC MS-004

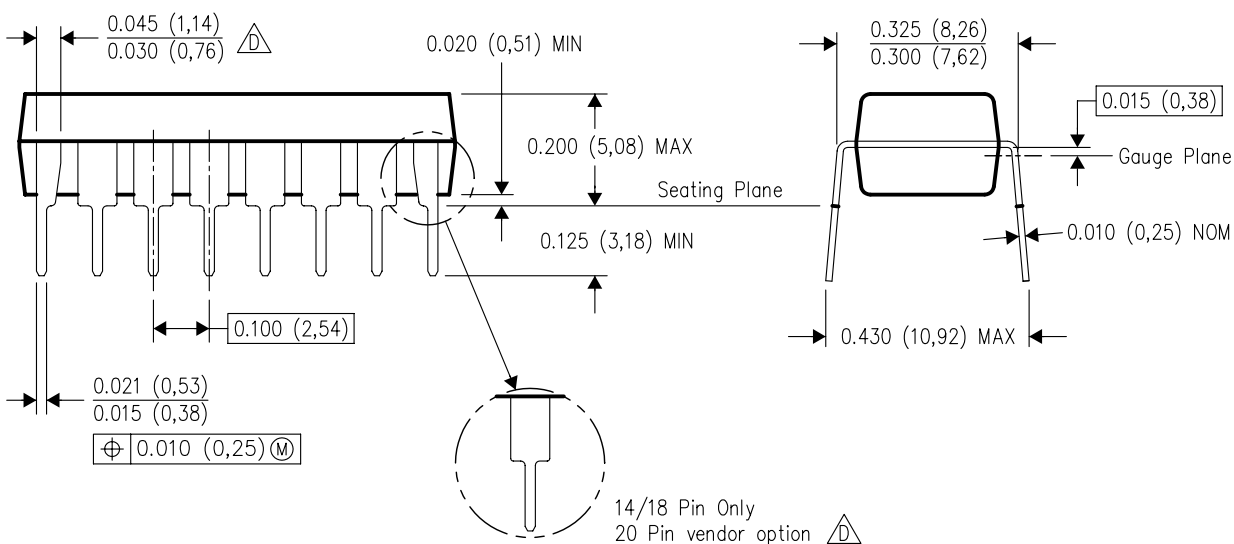
N (R-PDIP-T**)

16 PINS SHOWN

PLASTIC DUAL-IN-LINE PACKAGE



PINS ** DIM	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS-001 VARIATION	AA	BB	AC	AD

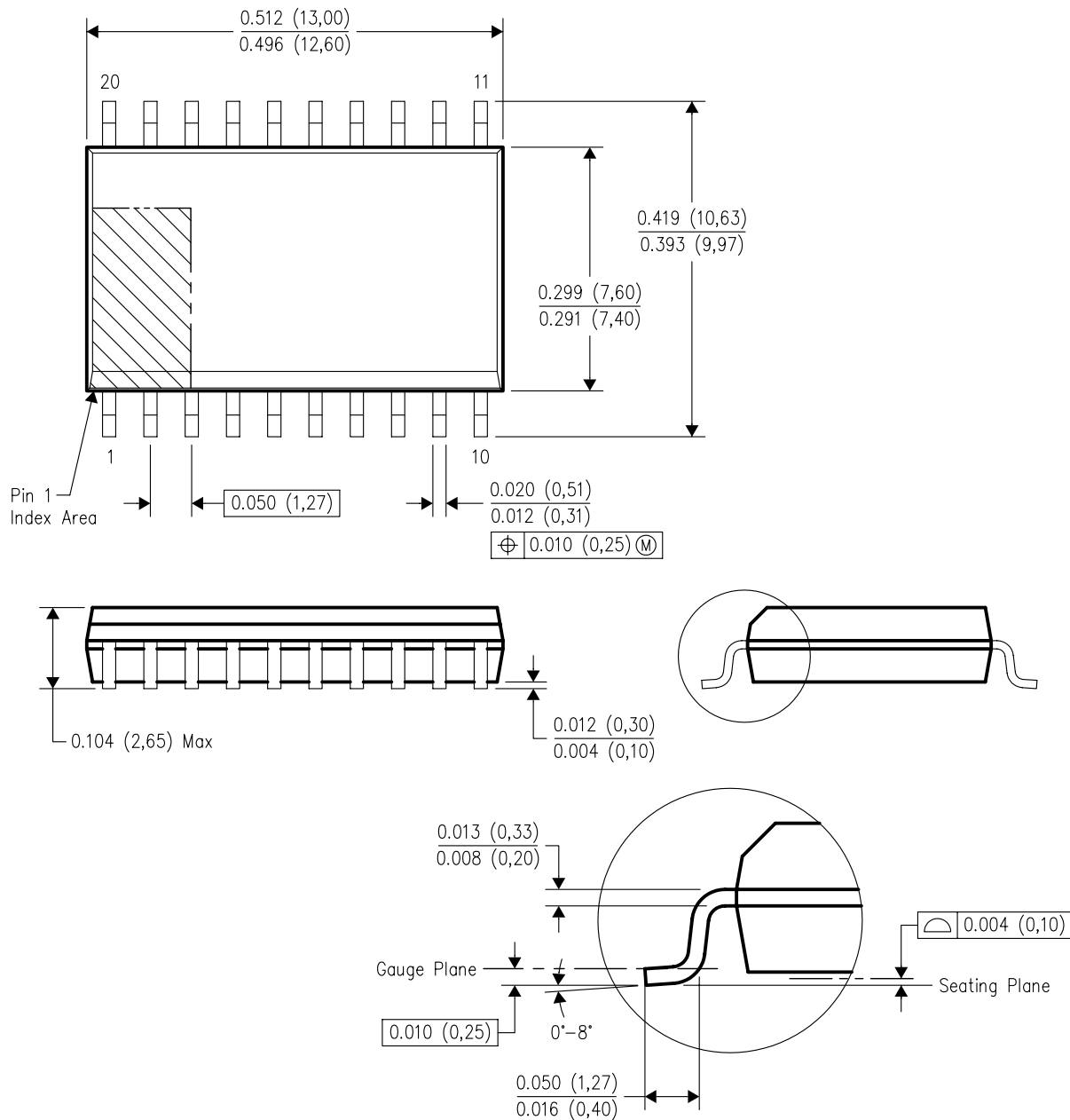


4040049/E 12/2002

- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 -  Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 -  The 20 pin end lead shoulder width is a vendor option, either half or full width.

DW (R-PDSO-G20)

PLASTIC SMALL-OUTLINE PACKAGE



4040000-4/F 06/2004

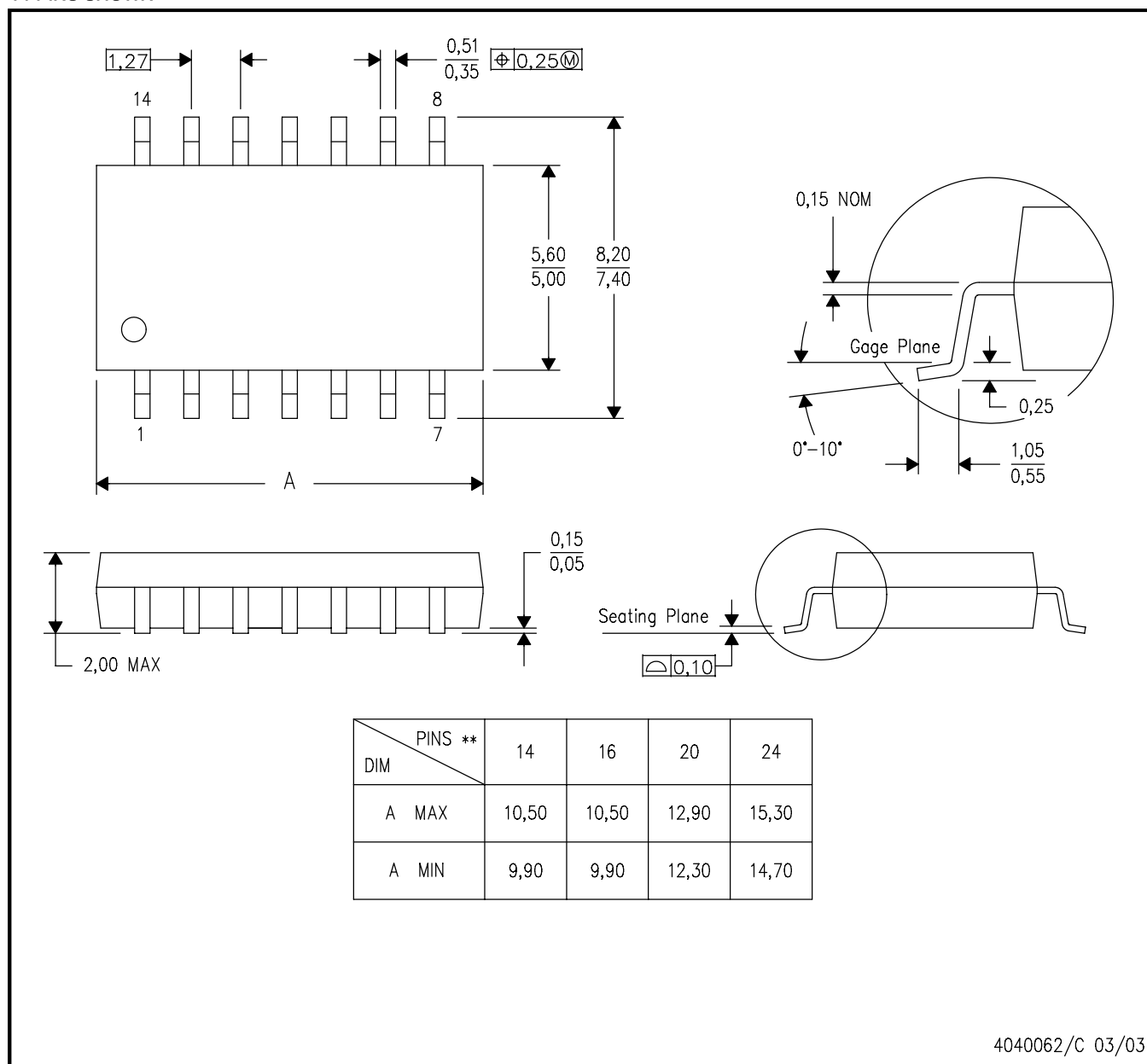
- NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
D. Falls within JEDEC MS-013 variation AC.

MECHANICAL DATA

NS (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN

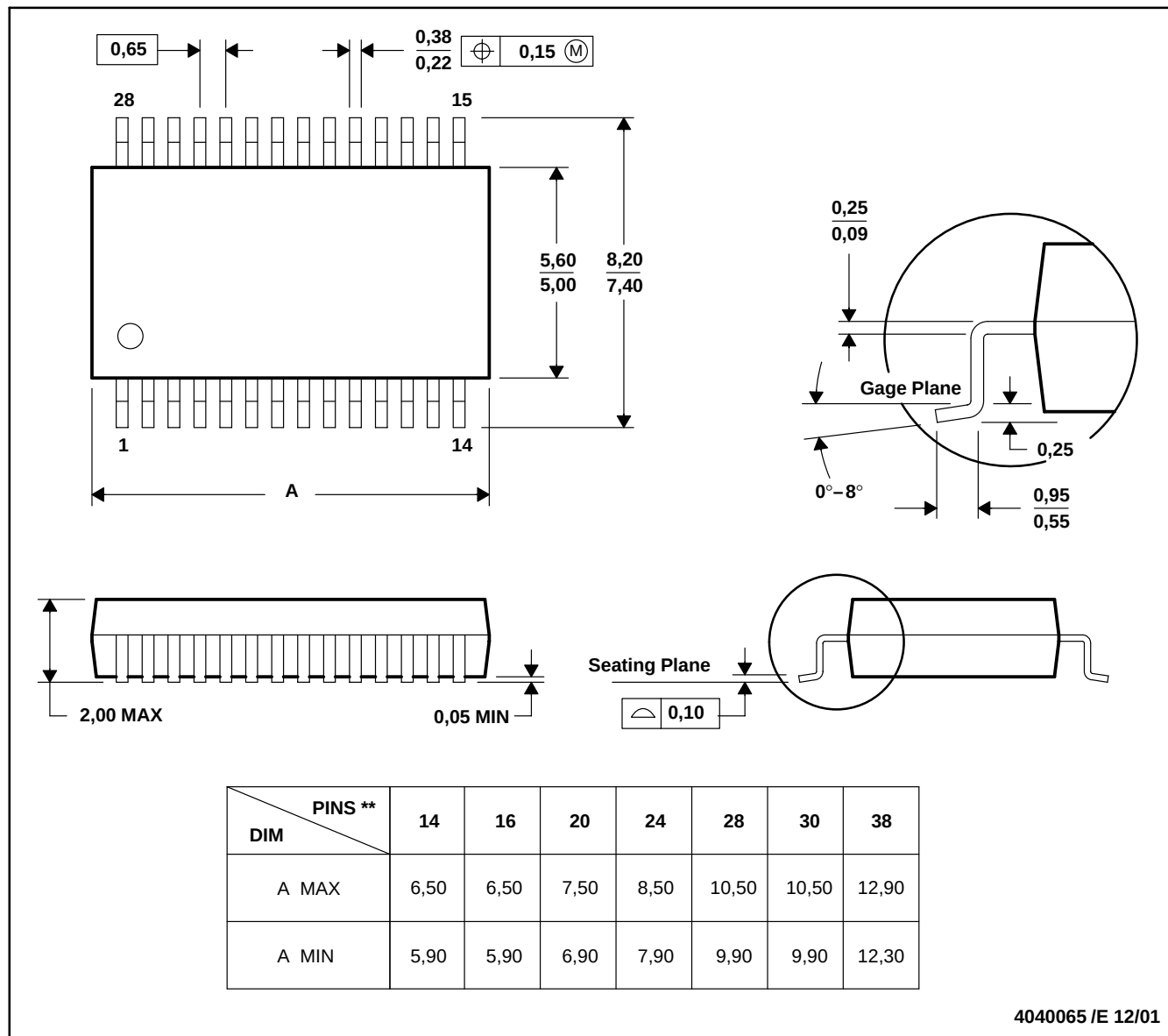


- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

DB (R-PDSO-G**)

PLASTIC SMALL-OUTLINE

28 PINS SHOWN

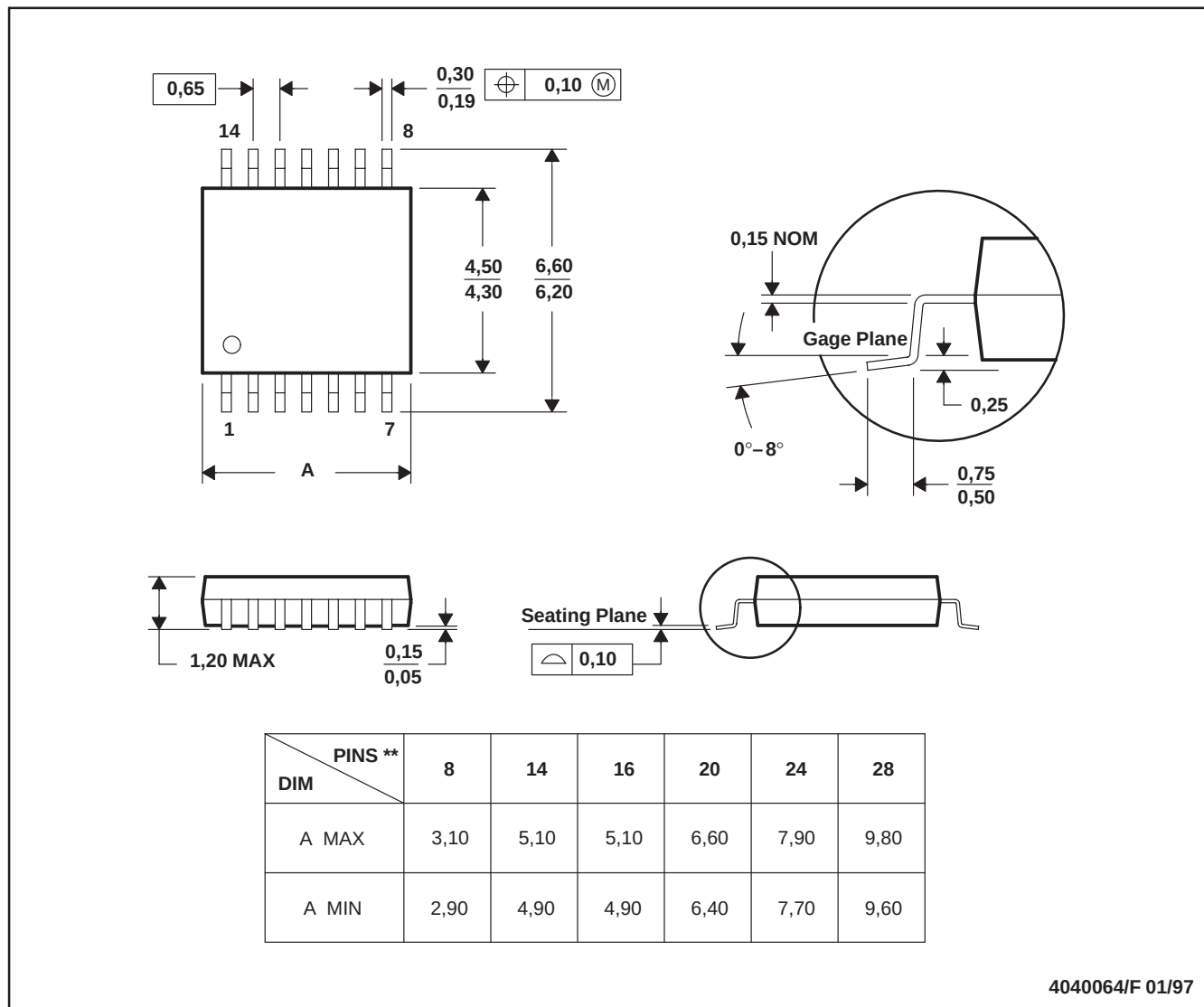


- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-150

PW (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-153

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