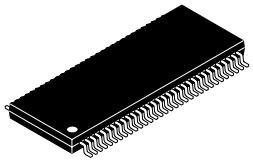


SLLS462 – AUGUST 2001

HIGH-SPEED DIFFERENTIAL 8-BIT REGISTERED TRANSCEIVER

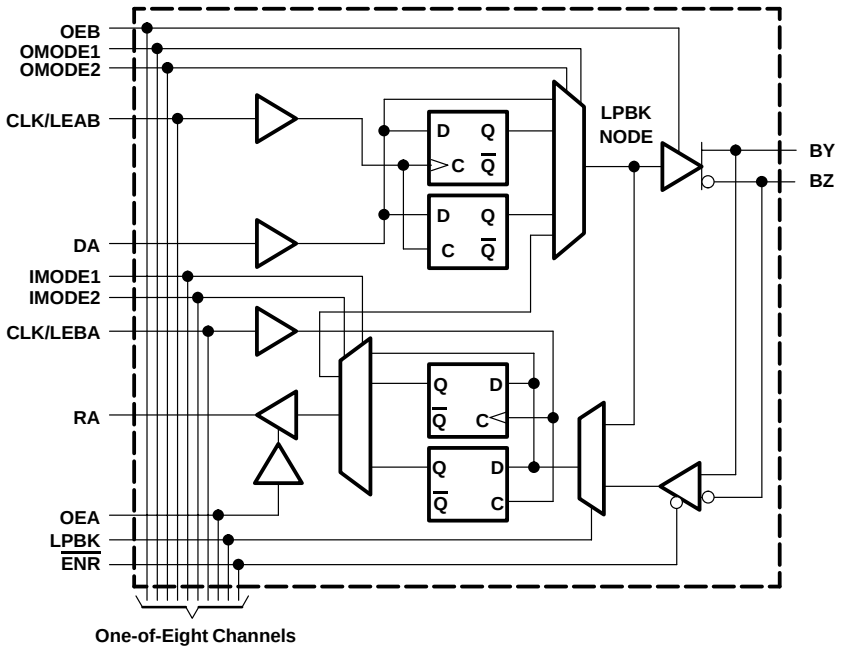
FEATURES

- 8-Bit Bidirectional Data Storage Register With Full Parallel Access
- Parallel Transfer Rates†
  - Buffer Mode: Up to 475 Megatransfers
  - Flip-Flop Mode: Up to 300 Megatransfers
  - Latch Mode: Up to 300 Megatransfers
- Operates With a Single 3.3-V Supply
- Low-Voltage Differential Signaling With Typical Output Voltage of 350 mV Across a 50-Ω Load
- Bus and Logic Loopback Capability
- Very Low Radiation Emission
- Low Skew Performance
  - Pulse Skew Less Than 100 ps
  - Output Skew Less Than 320 ps
  - Part-to-Part Skew Less Than 1 ns
- Open-Circuit Differential Receiver Fail Safe Assures a Low-Level Output
- Reset at Power Up
- 12-kV Bus-Pin ESD Protection
- Bus Pins Remain High-Impedance When Disabled or With V_{CC} Below 1.5 V for Power-Up/Down Glitch-Free Performance and Hot Plugging
- 5-V Tolerant LVCMOS Inputs

APPLICATIONS

- Telecom Switching
- Printers and Copiers
- Audio Mixing Consoles
- Automated Test Equipment

logic diagram



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

†Parallel data transfer through all channels simultaneously as defined by TIA/EIA–644 with t_r of t_f less than 30%of the unit interval.

DESCRIPTION

The SN65LVDM320 is an 8-bit data storage register with differential line drivers and receivers that are electrically compatible with ANSI EIA/TIA-644 for multipoint architectures with standard-compliant parallel transfer rates of 475 Mbps. The SN65LVDM320 includes transmitter and receiver data registers that remain active regardless of the state of their associated outputs.

The logic element for data flow in each direction is configured by mode-control inputs. IMODE1 and IMODE2 control data flow in the B-to-A (bus side to digital side) direction when configured as a buffer, a D-type flip-flop, or a D-type latch. OMODE1 and OMODE2 control data flow in each of the operating modes for the A-to-B (digital side to bus side) direction. When configured in buffer mode, input data appears at the output port. In the flip-flop mode, data is stored on the rising edge of the appropriate clock input, CLKAB/LEAB or CLKBA/LEBA. In the latch mode, this clock pin also serves as an active-high transparent latch enable.

Data flow is further controlled by the A-side loopback (LPBK) input. When LPBK is high, DA input data is looped back to the RA output. B-side bus data is looped back to the bus in latch mode by means of the IMODE and OMODE logic states.

The A-side output enable/disable control is provided by OEA. When OEA is low or V_{CC} is less than 2 V, the A side is in the high-impedance state. When OEA is high, the A side is active (high or low logic levels). The B-side output enable/disable control is provided by OEB. When OEB is low or V_{CC} is less than 2 V, the B side is in the high impedance state. When OEB is high, the B side is active (high or low logic levels).

The A-to-B and B-to-A logic elements are active regardless of the state of their associated outputs. New data can be entered (in latch and flip-flop modes) or previously stored data can be retained while the associated outputs are in the high-impedance or inactive states. The SN65LVDM320 also includes internally isolated analog (B-side) and digital (A-side) grounds for enhanced operation.

The SN65LVDM320 is characterized for operation from –40°C to 85°C.

Table 1. Mode Functions

INPUTS										MODE
CLK/LEAB	CLK/LEBA	OEA	OEB	$\overline{ENR}$	OMODE1	OMODE2	IMODE1	IMODE2	LPBK	
X	X	L	L	X	X	X	X	X	X	Isolation
X	X	X	H	X	L	L	X	X	X	A-to-B buffer mode (see Figure 1)
↑	X	X	H	X	L	H	X	X	X	A-to-B flip-flop mode (see Figure 2)
H (B follows A)	X	X	H	X	H	L	X	X	X	A-to-B latch mode (see Figure 3)
L (B latched)										
X	X	H	L	L	X	X	L	L	L	B-to-A buffer mode (see Figure 4)
X	↑	H	L	L	X	X	L	H	L	B-to-A flip-flop mode (see Figure 5)
X	H (A follows B)	H	L	L	X	X	H	L	L	B-to-A latch mode (see Figure 6)
	L (A latched)									
X	X	L	L	H	H	H	H	H	L	Bus loopback latch mode (see Figure 7)
X	X	H	L	H	X	X	X	X	H	DA to RA loopback mode (see Figures 8 through 10)

H = high level, L = low level, X = don't care, ↑ = low-to-high

Table 2. Pin Descriptions

PIN NAME	PIN NO.	DESCRIPTION
AGND	36, 44, 54, 58, 62	Analog (B-side) ground
1BY–8BY & 1BZ–8BZ	64 & 63, 60 & 59, 56 & 55, 52 & 51, 46 & 45, 42 & 41, 38 & 37, 34 & 33	Differential I/O pair
CLK/LEBA	18	B-side to A-side clock input or latch enable
CLK/LEAB	14	A-side to B-side clock input or latch enable
1DA–8DA	1, 3, 7, 9, 21, 25, 29, 31	Single-ended input
DGND	5, 11, 15, 19, 23, 27	Digital (A-side) ground
$\overline{\text{ENR}}$	39	Receiver differential data enable
IMODE1 IMODE2	50, 49	B-side to A-side buffer, flip-flop, or latch mode control and bus loopback control (see Table 3)
LPBK	48	A-side loopback enable
OEA	47	A-side output enable
OEB	40	B-side output enable
OMODE1, OMODE2	13, 17	A-side to B-side buffer, flip-flop, or latch mode control and bus loopback control (see Table 3)
RA	2, 4, 8, 10, 22, 26, 30, 32	Single-ended output
VCC	6, 12, 16, 20, 24, 28, 35, 43, 53, 57, 61	Supply voltage

pin assignments

SN65LVDM320DGG
(Marked as LVDM320)
(TOP VIEW)

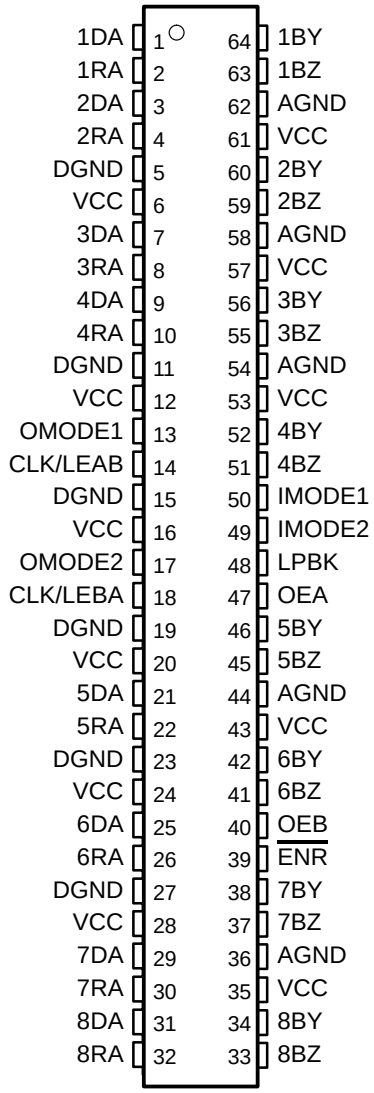


Table 3. IMODE Logic

IMODE1	IMODE2	MODE FUNCTION (B SIDE TO A SIDE)
0	0	Buffer
0	1	Flip-Flop
1	0	Latch
1	1	Bus loopback†

Table 4. OMODE Logic

IMODE1	IMODE2	MODE FUNCTION (A SIDE TO B SIDE)
0	0	Buffer
0	1	Flip-Flop
1	0	Latch
1	1	Bus loopback†

† All IMODE and OMODE pins must be high for the differential bus loopback latch mode.

mode function diagrams

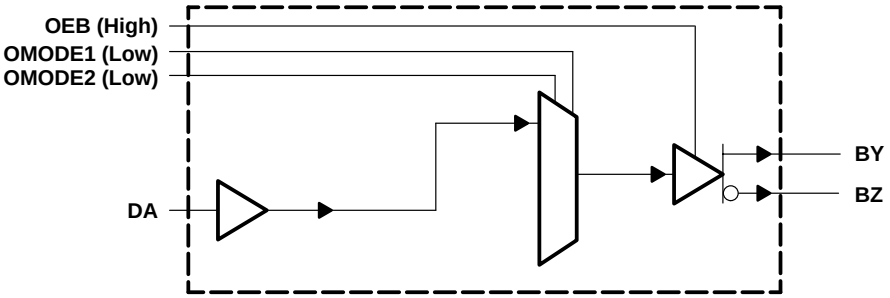


Figure 1. A-to-B Buffer Mode

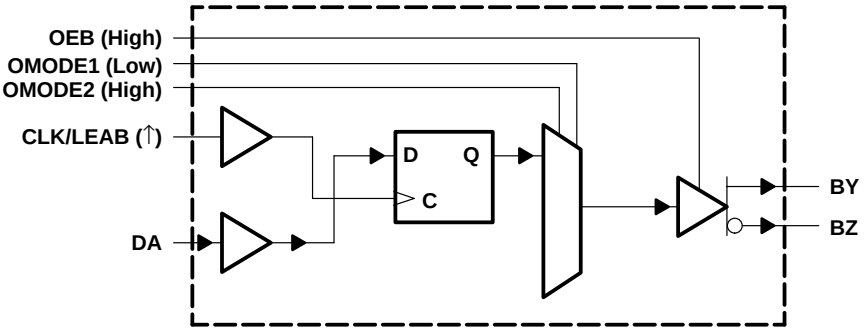


Figure 2. A-to-B Flip-Flop Mode

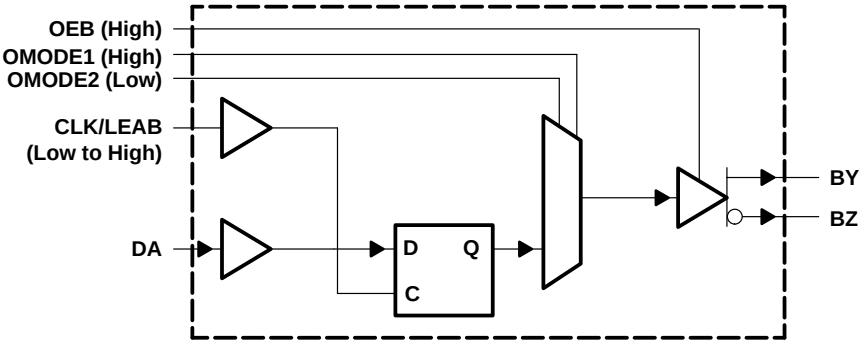


Figure 3. A-to-B Latch Mode

mode function diagrams (continued)

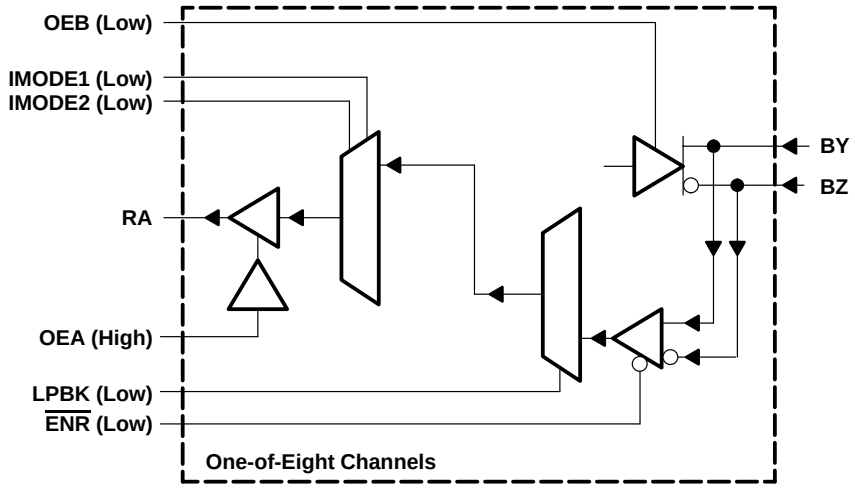


Figure 4. B-to-A Buffer Mode

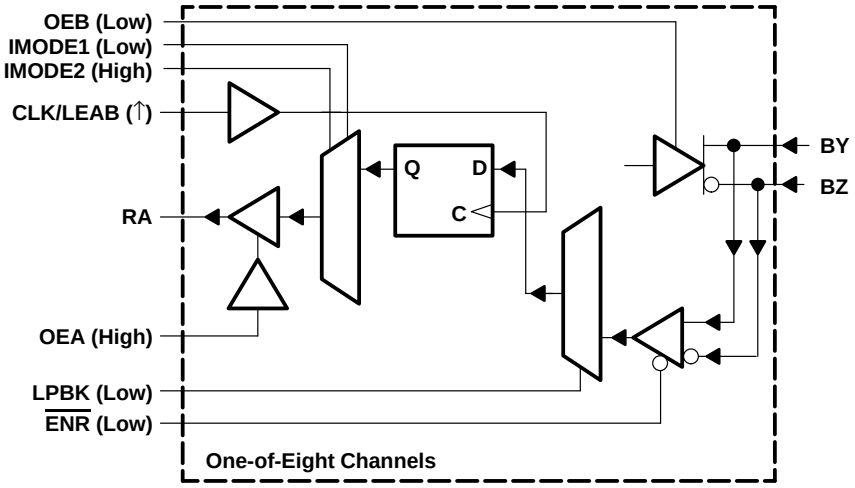


Figure 5. B-to-A Flip-Flop Mode

mode function diagrams (continued)

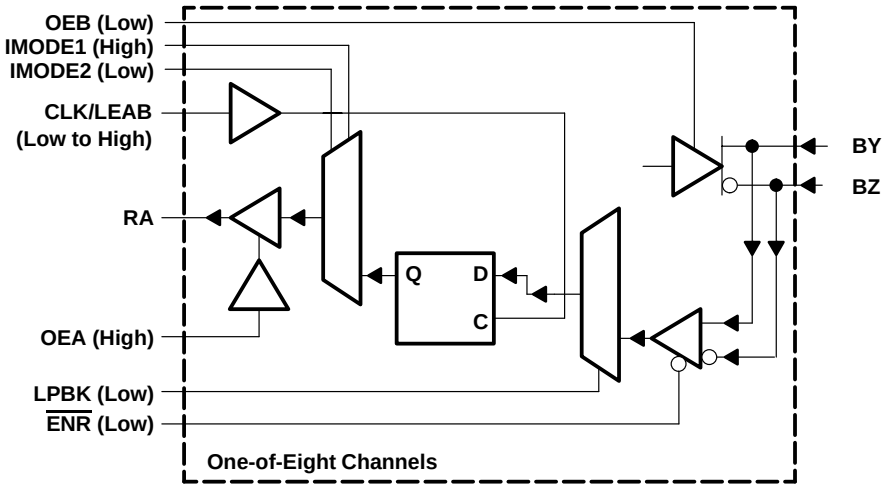


Figure 6. B-to-A Latch Mode

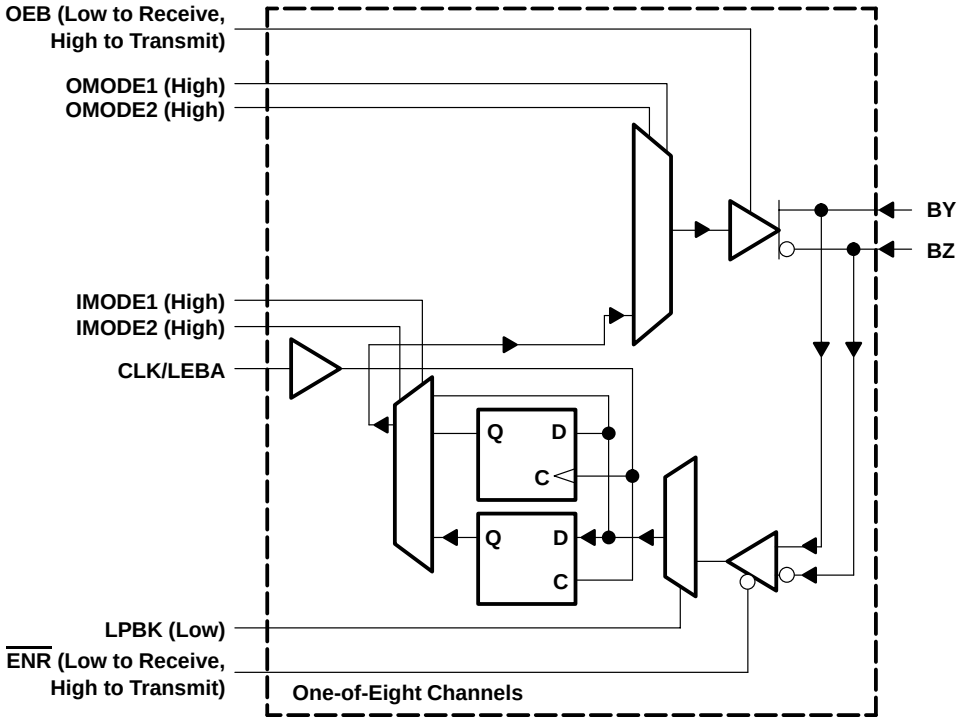


Figure 7. Bus Loopback Latch Mode

mode function diagrams (continued)

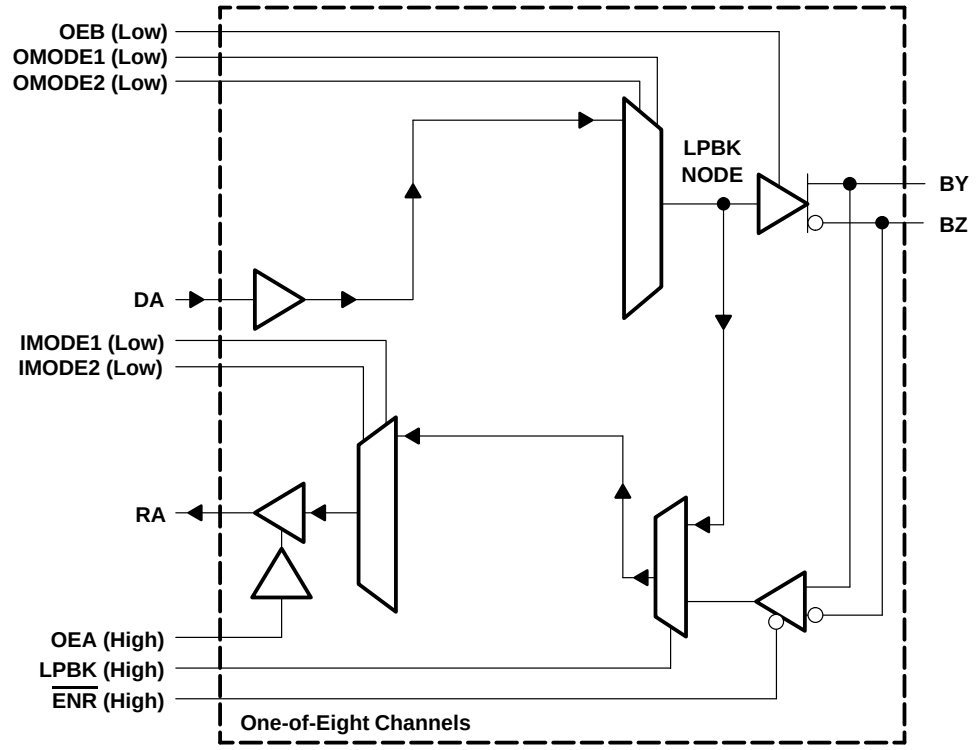


Figure 8. DA to RA Buffer Mode

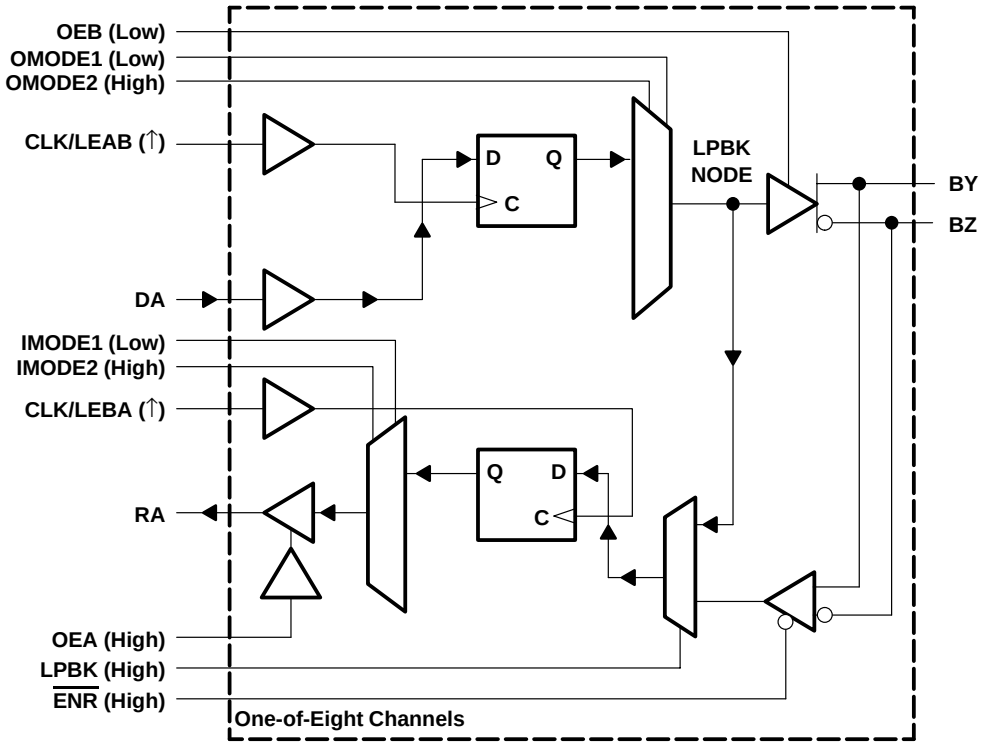


Figure 9. DA to RA Flip-Flop Mode

mode function diagrams (continued)

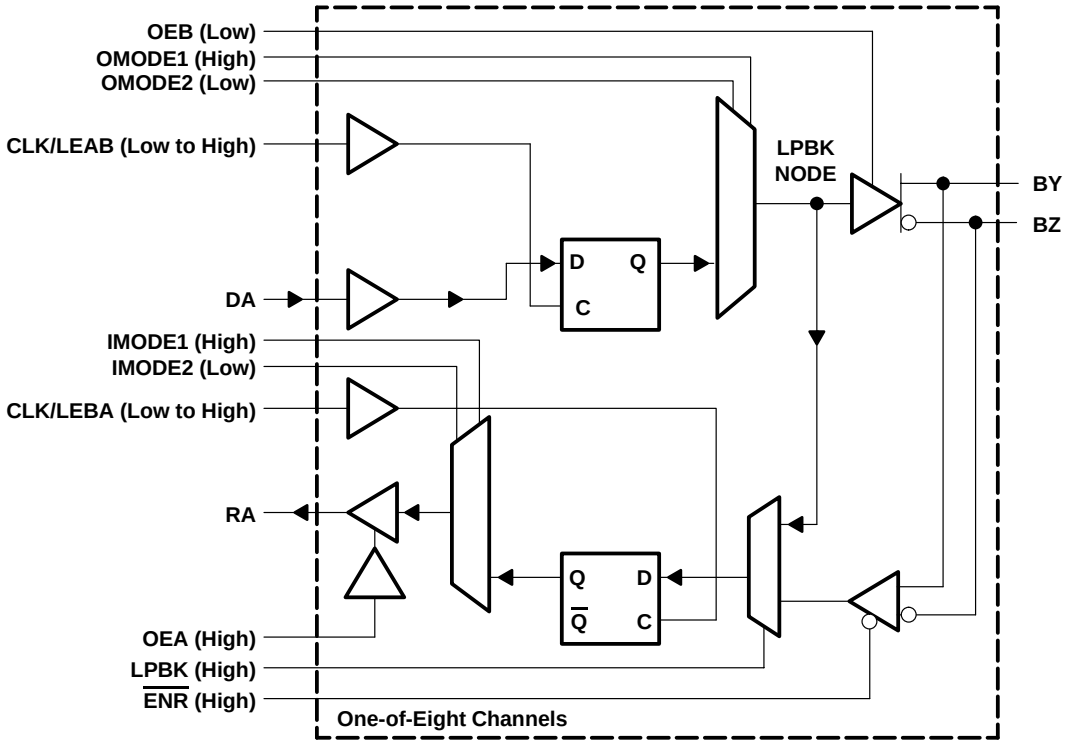


Figure 10. DA to RA Latch Mode

equivalent input and output schematic diagrams

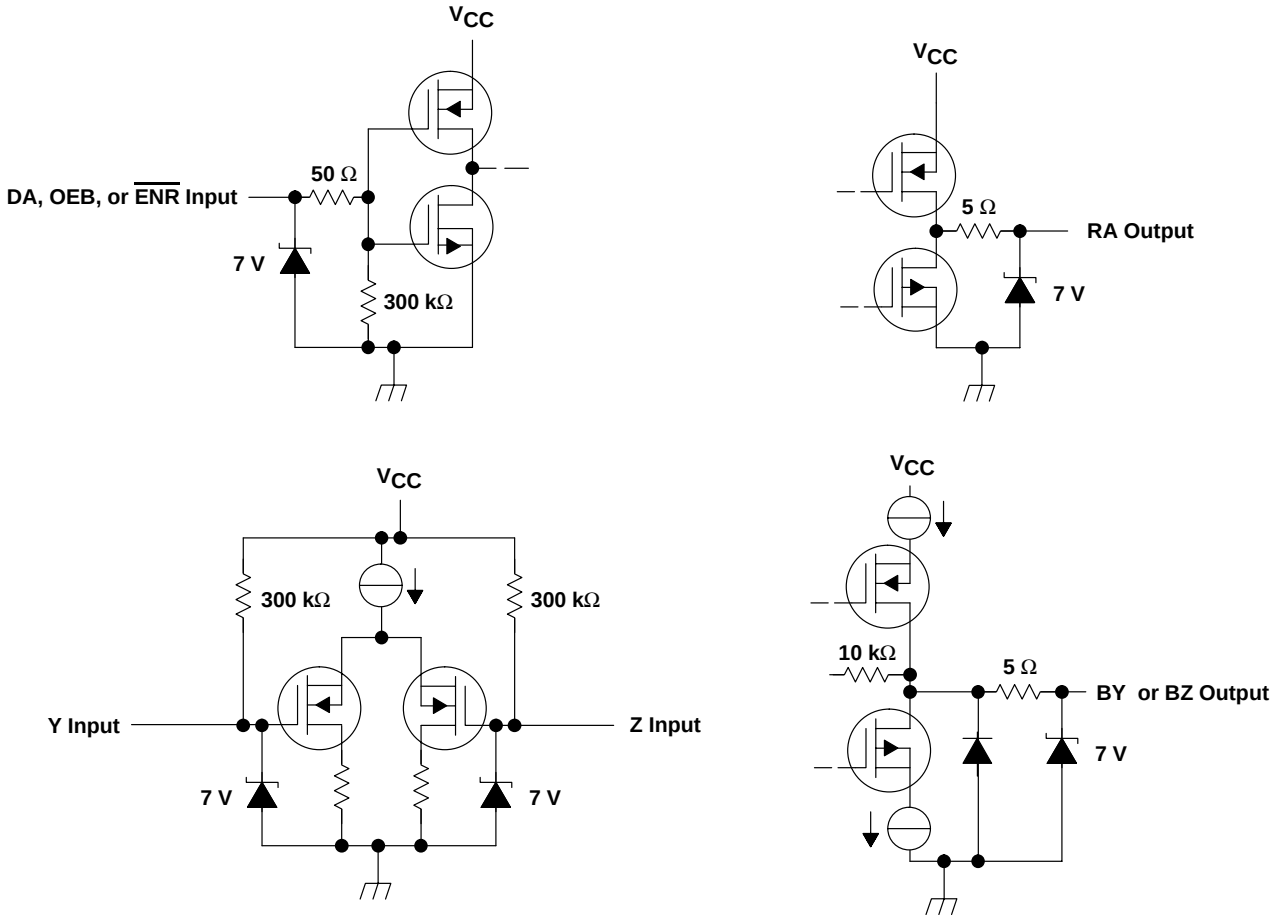


Table 5. LVDM Receiver Function Table

BUS INPUTS	OUTPUT
$V_{ID} = V_Y - V_Z$	
$V_{ID} \geq 100$ mV	H
-100 mV $< V_{ID} < 100$ mV	?
$V_{ID} \leq -100$ mV	L
Open	L

H = high-level, L = low-level, ? = indeterminate

absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

Supply voltage range, VCC (see Note 1) . . . . . –0.5 V to 4 V
Voltage range (TTL pins) . . . . . –0.5 V to 6 V
Voltage range BY and BZ . . . . . –0.5 V to 4 V
Electrostatic discharge: Y, Z, and GND (see Note 2) . . . . . Class 3, A: 12 kV, B: 600 V
All pins . . . . . Class 3, A: 7 kV, B: 500 V
Continuous power dissipation . . . . . (see Dissipation Rating Table)
Storage temperature range . . . . . –65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values, except differential I/O bus voltages, are with respect to network ground terminal.
2. Tested in accordance with MIL-STD-883E Method 3015.7.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$	DERATING FACTOR (see Note 3) ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING
DGG (see Note 4)	2094 mW	16.7 mW/°C	1340 mW	1089 mW
DGG (see Note 5)	3765 mW	30.1 mW/°C	2410 mW	1958 mW

NOTES: 3. This is the inverse of the junction-to-ambient thermal resistance when board-mounted and with no air flow.
4. Tested in accordance with the Low-K thermal metric definitions of EIA/JESD51–3.
5. Tested in accordance with the High-K thermal metric definitions of EIA/JESD51–7.

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	3	3.3	3.6	V
High-level input voltage, V_{IH}	2			V
Low-level input voltage, V_{IL}			0.8	V
Magnitude of differential input voltage, $\lvert V_{ID}\rvert$	0.1		0.6	V
Common-mode input voltage, V_{IC}	$\frac{\lvert V_{ID}\rvert}{2}$		$2.4 - \frac{\lvert V_{ID}\rvert}{2}$	V
			$V_{CC} - 0.8$	
Operating free-air temperature, T_A	–40		85	°C

supply current

PARAMETER		TEST CONDITIONS	MIN	NOM	MAX	UNIT
I_{CC}	Supply current	Driver enabled, receiver enabled, R_L = 50 Ω (DA, OEA, OEB to V_{CC}, $\overline{ENR}$ to GND)		75	130	mA
		Driver disabled, receiver disabled (DA, OEA, OEB to GND, $\overline{ENR}$ to V_{CC})		1	3	mA
		Driver enabled, receiver disabled, R_L = 50 Ω (DA, OEB, $\overline{ENR}$ to V_{CC}, OEA to GND)		60	100	mA
		Driver disabled, receiver enabled (DA, OEB, $\overline{ENR}$ to GND, OEA to V_{CC})		20	40	mA

electrical characteristics over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
$\|V_{OD}\|$	Differential output voltage magnitude	R_L = 50 Ω, See Figures 11 and 12	247	330	454	mV
$\Delta\|V_{OD}\|$	Change in differential output voltage magnitude between logic states		–50‡		50	
$V_{OC(SS)}$	Steady-state common-mode B-port output voltage	See Figure 13	1.125		1.375	V
$\Delta V_{OC(SS)}$	Change in steady-state common-mode B-port output voltage between logic states		–50		50	mV
$V_{OC(PP)}$	Peak-to-peak common-mode B-port output voltage			50	150	
I_{OZ}	RA-port high-impedance output current	V_O = 0 V or 3.6 V	–10		10	µA
I_{IH}	DA port high-level input current	V_{IH} = 2 V			20	µA
I_{IL}	DA port low-level input current	V_{IL} = 0.8 V			10	µA
I_{OS}	Differential short-circuit output current	V_{OY} or V_{OZ} = 0	–10		10	mA
		V_{OD} = 0	–10		10	mA
$I_{O(OFF)}$	Power-off differential output current	V_{OD} = 2.4 V, V_{CC} = 1.5 V	–10		10	µA
V_{IT+}	Positive-going differential input voltage threshold	See Figure 16 and Table 6			100	mV
$V_{IT–}$	Negative-going differential input voltage threshold		–100			
V_{OH}	High-level RA port output voltage	I_{OH} = –8 mA	2.4			V
V_{OL}	Low-level RA port output voltage	I_{OL} = 8 mA			0.4	V
I_I	Input current (Y or Z inputs)	V_I = 0 V	–35			µA
		V_I = 2.4 V	–10			µA
I_{ID}	Differential input current $\|I_{IY} – I_{IZ}\|$	V_{IY} = 0 and V_{IZ} = 100 mV, V_{IY} = 2.4 V and V_{IZ} = 2.3 V	–10		10	µA
$I_{I(OFF)}$	Power-off input current (Y or Z inputs)	V_{CC} 0 V, V_I = 2.4 V	–20		20	µA
$C_{(INA)}$	DA port Input capacitance	V_I = 0.4 sin (4E6πt) + 0.5 V		5		pF
$C_{(INB)}$	B-port Input capacitance	V_I = 0.4 sin (4E6πt) + 0.5 V		6		pF
$V_{O(0PX)}$	B-port crosstalk output voltage (zero-to-peak)	See Figure 20		0.1		mV

† All typical values are at 25°C and with a 3.3-V supply voltage.
‡ The algebraic convention, in which the least positive (most negative) limit is designated as minimum is used in this data sheet.

device switching characteristics over recommended operating conditions (unless otherwise noted)

PARAMETER		FROM (INPUT)	TO (OUTPUT)	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	DA (buffer mode) See Figures 1 & 14	BY, BZ	1.4	3.3	5.2	ns
t_{PHL}	Propagation delay time, high-to-low-level output			1.4	3.3	5.3	
t_{PLH}	Propagation delay time, low-to-high-level output	BY, BZ (buffer mode) See See Figures 4 & 17	RA	2.5	4.3	6.2	ns
t_{PHL}	Propagation delay time, high-to-low-level output			2.5	4.3	6.5	
t_{PLH}	Propagation delay time, low-to-high-level output	DA (latch mode) See Figures 3 & 14	BY, BZ	3	5.5	8.5	ns
t_{PHL}	Propagation delay time, high-to-low-level output			3	5.5	8.7	
t_{PLH}	Propagation delay time, low-to-high-level output	BY,BZ (latch mode) See Figure 6	RA	4	6.5	9.3	ns
t_{PHL}	Propagation delay time, high-to-low-level output			4	6.5	9.8	
t_{PLH}	Propagation delay time, low-to-high-level output	CLKAB See Figures 2 & 22	BY, BZ	3.5	6.5	9.5	ns
t_{PHL}	Propagation delay time, high-to-low-level output			3.5	6.5	9.5	
t_{PLH}	Propagation delay time, low-to-high-level output	CLKBA See Figures 5 & 23	RA	3.8	6.5	10.5	ns
t_{PHL}	Propagation delay time, high-to-low-level output			3.8	6.5	10.5	
t_{PLH}	Propagation delay time, low-to-high-level output	DA See Figures 8 & 19	RA	1.8	3.2	7	ns
t_{PHL}	Propagation delay time, high-to-low-level output			1.8	3.2	7	
t_{PHZ}	Propagation delay time, high-level-to-high-impedance output	OEA See Figure 20	RA		15	26	ns
t_{PLZ}	Propagation delay time, low-level-to-high-impedance output				15	23	
t_{PZH}	Propagation delay time, high-impedance-to-high-level output				15	26	ns
t_{PZL}	Propagation delay time, high-impedance-to-low-level output				15	23	
t_{PHZ}	Propagation delay time, high-level-to-high-impedance output	OEB See Figure 15	BY, BZ		10	15	ns
t_{PLZ}	Propagation delay time, low-level-to-high-impedance output				10	17	
t_{PZH}	Propagation delay time, high-impedance-to-high-level output				10	15	ns
t_{PZL}	Propagation delay time, high-impedance-to-low-level output				10	17	
$t_{r(B)}$	Output signal rise time B port	See Figure 14			470		ps
$t_{f(B)}$	Output signal fall time B port				450		
$t_{r(A)}$	Output signal rise time A port	See Figure 17			580		ps
$t_{f(A)}$	Output signal fall time A port				630		
$t_{sk(o)}$†	Output skew channel-to-channel				0.3		ns
$t_{sk(p)}$	Pulse skew ($\lvert t_{PHL} - t_{PLH} \rvert$)—A-port				0.7		ns
$t_{sk(p)}$	Pulse skew ($\lvert t_{PHL} - t_{PLH} \rvert$)—B-port				0.7		ns
$t_{sk(pp)}$‡	Part-to-part skew				0.6		ns

† $t_{sk(o)}$ is the skew between specified outputs of a single device with all driving inputs connected together and the outputs switching in the same direction while driving identical specified loads.

‡ $t_{sk(pp)}$ is the magnitude of the difference delay times between any specified terminals of two devices when both devices operate with the same supply voltages, at the same temperature, and have identical packages and test circuits.

timing requirements over recommended operating conditions (see Figure 21) (unless otherwise noted)

			MIN	TYP	MAX	UNIT
f_{max}		CLK/LEAB or CLK/LEBA in flip-flop mode			300	MHz
t_{SU}	Setup time	Setup for flip-flop	0.2			ns
		Setup for latch	1.0			ns
t_h	Hold time	Hold time for flip-flop	1.9			ns
		Hold time for latch	1.0			ns

PARAMETER MEASUREMENT INFORMATION

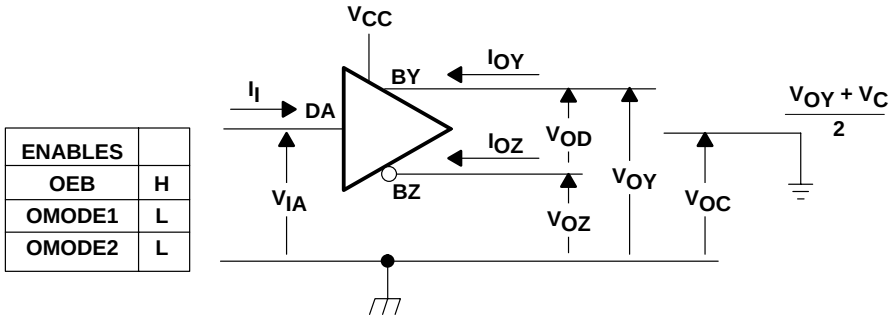


Figure 11. Driver Voltage and Current Definitions

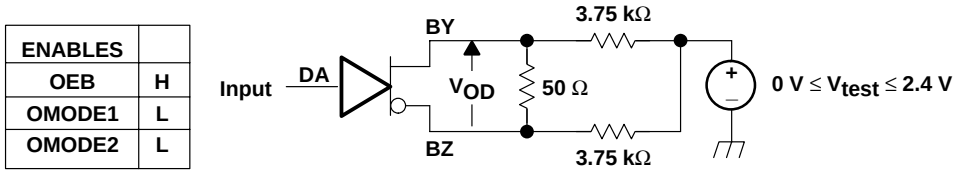


Figure 12. VOD Test Circuit

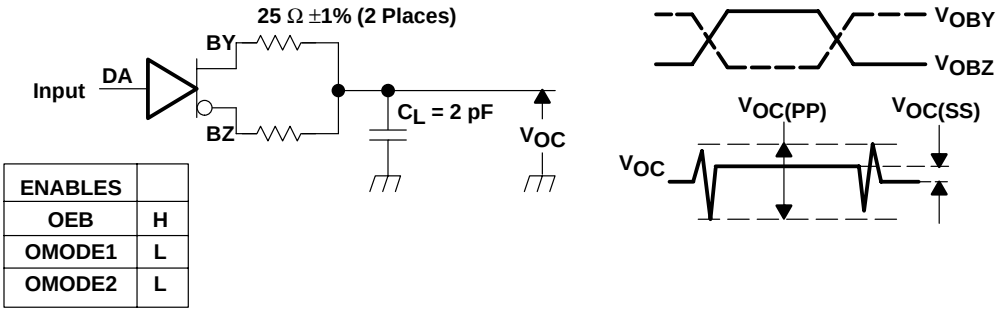
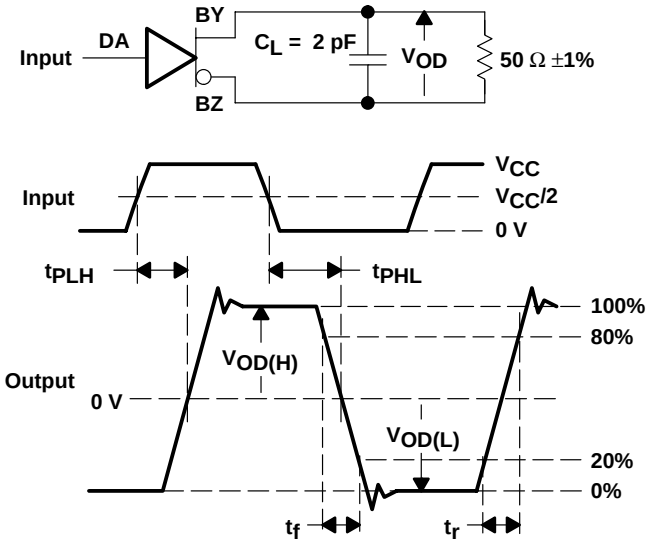


Figure 13. Test Circuit and Definitions for the Differential Common-Mode Output Voltage

NOTE: All input pulses are supplied by a generator having the following characteristics: t_r or $t_f \le 1$ ns, pulse repetition rate (PRR) = 0.5 Mpps, pulse width = 500 ± 10 ns . C_L includes instrumentation and fixture capacitance within 0,06 m of the device under test. The measurement of $V_{OC(PP)}$ is made on test equipment with a –3-dB bandwidth of at least 300 MHz.

PARAMETER MEASUREMENT INFORMATION



NOTE: All input pulses are supplied by a generator having the following characteristics: t_r or $t_f \leq 1$ ns, pulse repetition rate (PRR) = 50 Mpps, pulse width = 10 ± 0.2 ns . C_L includes instrumentation and fixture capacitance within 0,06 m of the device under test.

Figure 14. Test Circuit, Timing, and Voltage Definitions for the DIfferential Output Signal

PARAMETER MEASUREMENT INFORMATION

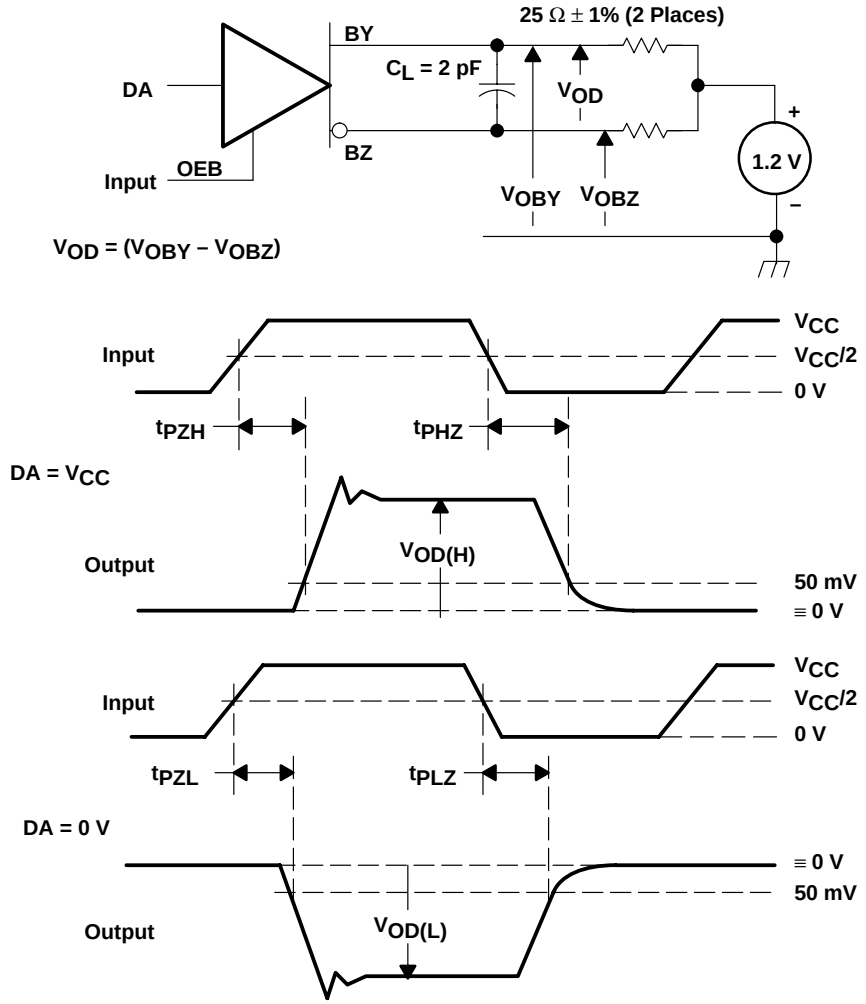


Figure 15. A-to-B Enable/Disable Time Test Circuit and Definitions

ENABLES	
$\overline{\text{ENR}}$	L
IMODE1	L
IMODE2	L
OEA	H

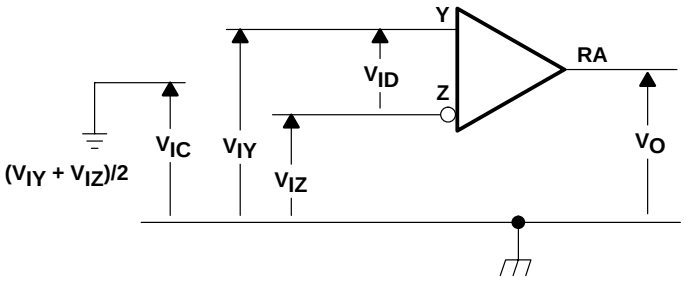
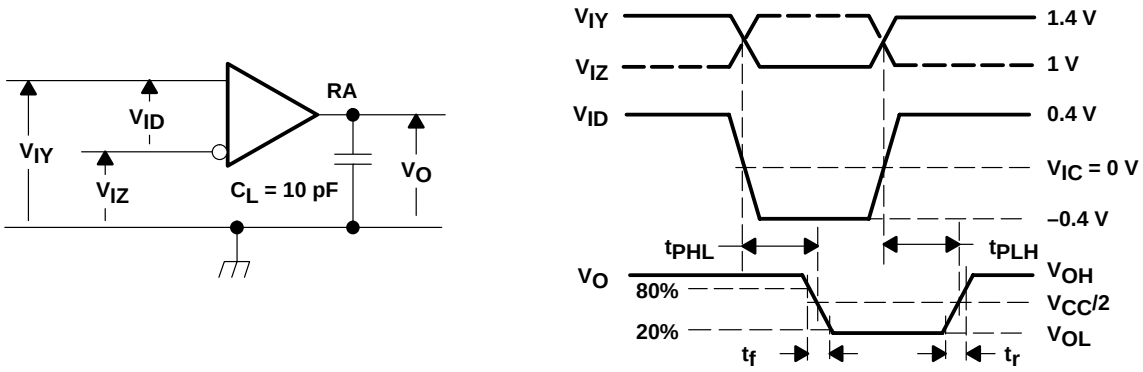


Figure 16. Voltage Definitions

PARAMETER MEASUREMENT INFORMATION

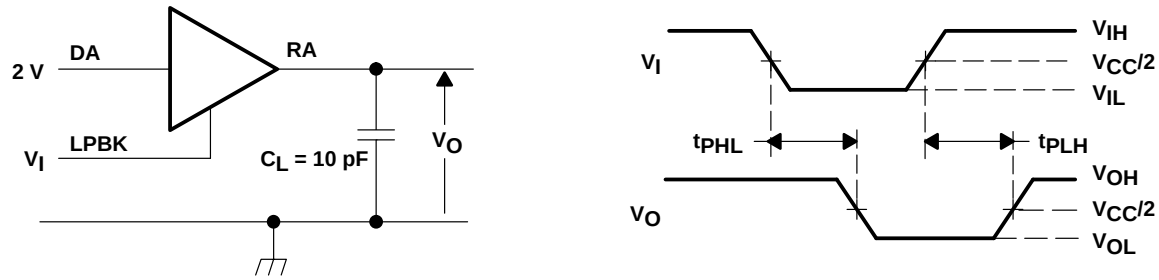
Table 6. Receiver Minimum and Maximum Fail-Safe Input Threshold Test Voltages

APPLIED VOLTAGES		RESULTING DIFFERENTIAL INPUT VOLTAGE	RESULTING COMMON-MODE INPUT VOLTAGE
V_{IY}	V_{IZ}	V_{ID}	V_{IC}
1.25 V	1.15 V	100 mV	1.2 V
1.15 V	1.25 V	–100 mV	1.2 V
2.4 V	2.3 V	100 mV	2.35 V
2.3 V	2.4 V	–100 mV	2.35 V
0.1 V	0 V	100 mV	0.05 V
0 V	0.1 V	–100 mV	0.05 V
1.5 V	0.9 V	600 mV	1.2 V
0.9 V	1.5 V	–600 mV	1.2 V
2.4 V	1.8 V	600 mV	2.1 V
1.8 V	2.4 V	–600 mV	2.1 V
0.6 V	0 V	600 mV	0.3 V
0 V	0.6 V	–600 mV	0 .3V



NOTE: All input pulses are supplied by a generator having the following characteristics: t_r or $t_f \leq 1$ ns, pulse repetition rate (PRR) = 50 Mpps, pulse width = 10 ± 0.2 ns . C_L includes instrumentation and fixture capacitance within 0,06 m of the device under test.

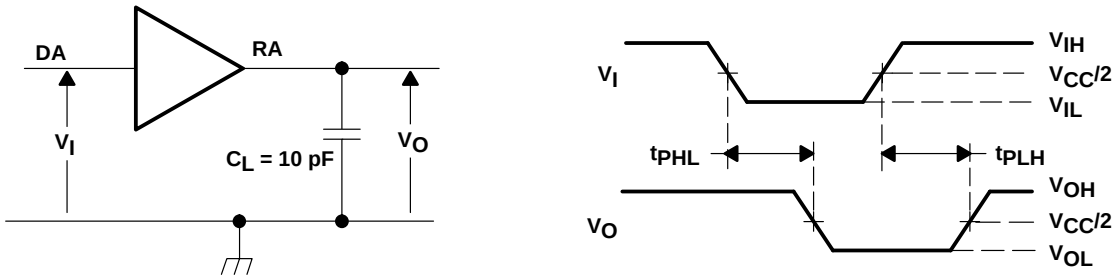
Figure 17. Timing Test Circuit and Waveforms



NOTE: All input pulses are supplied by a generator having the following characteristics: t_r or $t_f \leq 1$ ns, pulse repetition rate (PRR) = 50 Mpps, pulse width = 10 ± 0.2 ns . C_L includes instrumentation and fixture capacitance within 0,06 m of the device under test.

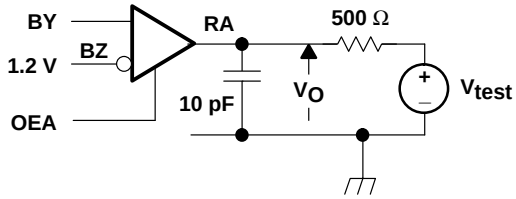
Figure 18. LPBK Timing Test Circuit and Waveforms

PARAMETER MEASUREMENT INFORMATION



NOTE: All input pulses are supplied by a generator having the following characteristics: t_r or $t_f \le 1$ ns, pulse repetition rate (PRR) = 50 Mpps, pulse width = 10 ± 0.2 ns . C_L includes instrumentation and fixture capacitance within 0,06 m of the device under test.

Figure 19. DA to RA Timing Test Circuit and Waveforms



NOTE: All input pulses are supplied by a generator having the following characteristics: t_r or $t_f \le 1$ ns, pulse repetition rate (PRR) = 0.5 Mpps, pulse width = 500 ± 10 ns . C_L includes instrumentation and fixture capacitance within 0,06 m of the device under test.

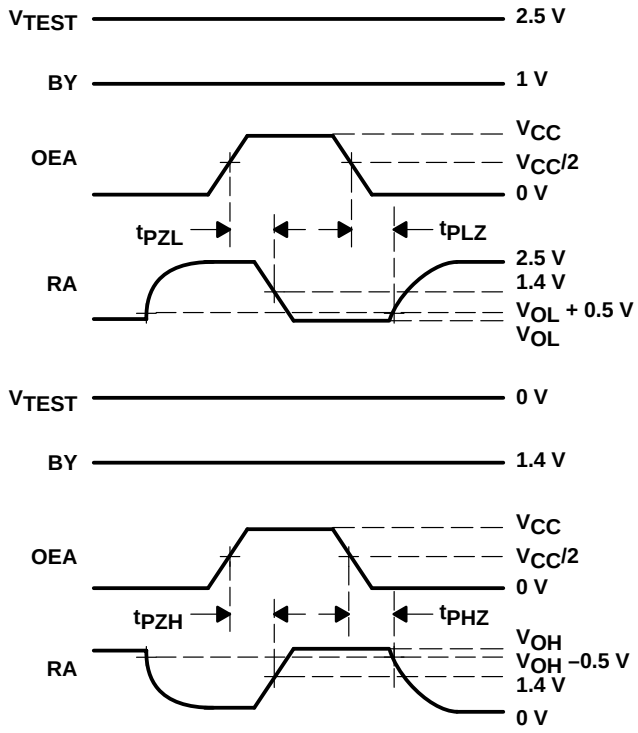


Figure 20. B-to-A Enable/Disable Time Test Circuit and Definitions

PARAMETER MEASUREMENT INFORMATION

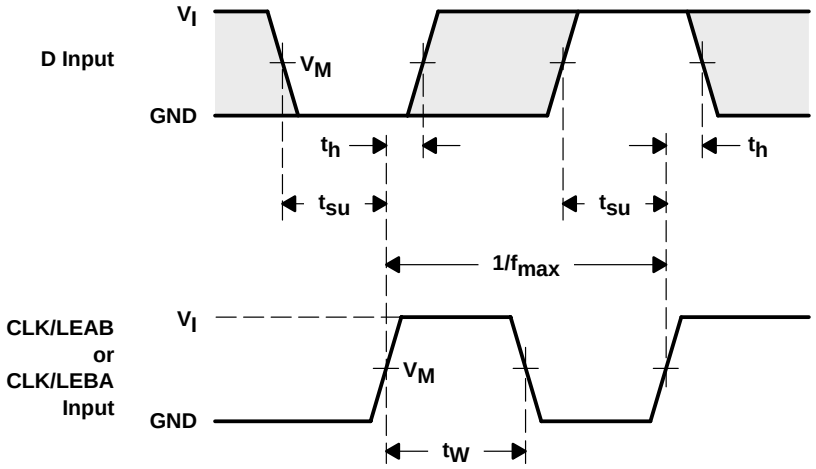


Figure 21. Setup and Hold Time Definition

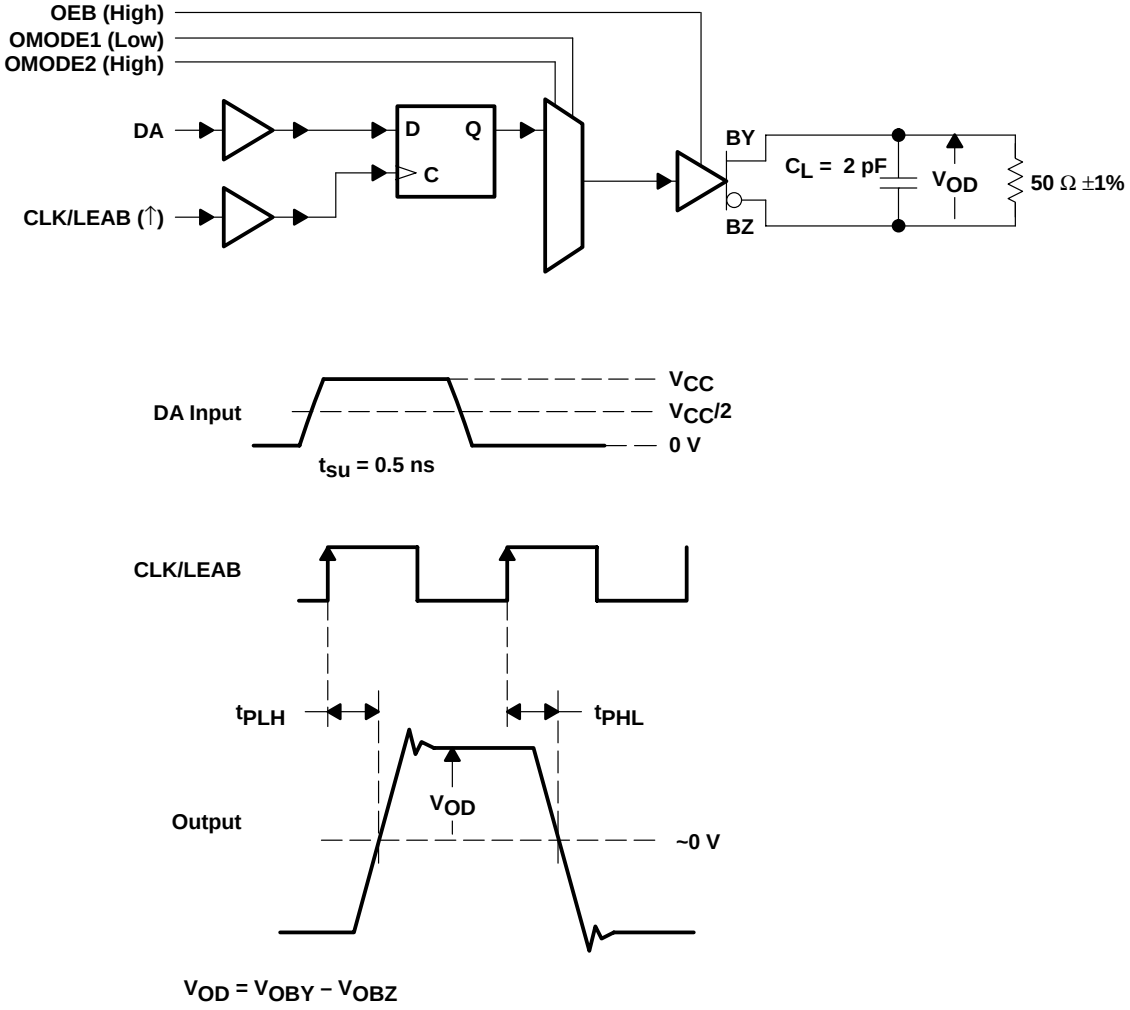


Figure 22. A-to-B Flip-Flop Mode Timing Circuit

PARAMETER MEASUREMENT INFORMATION

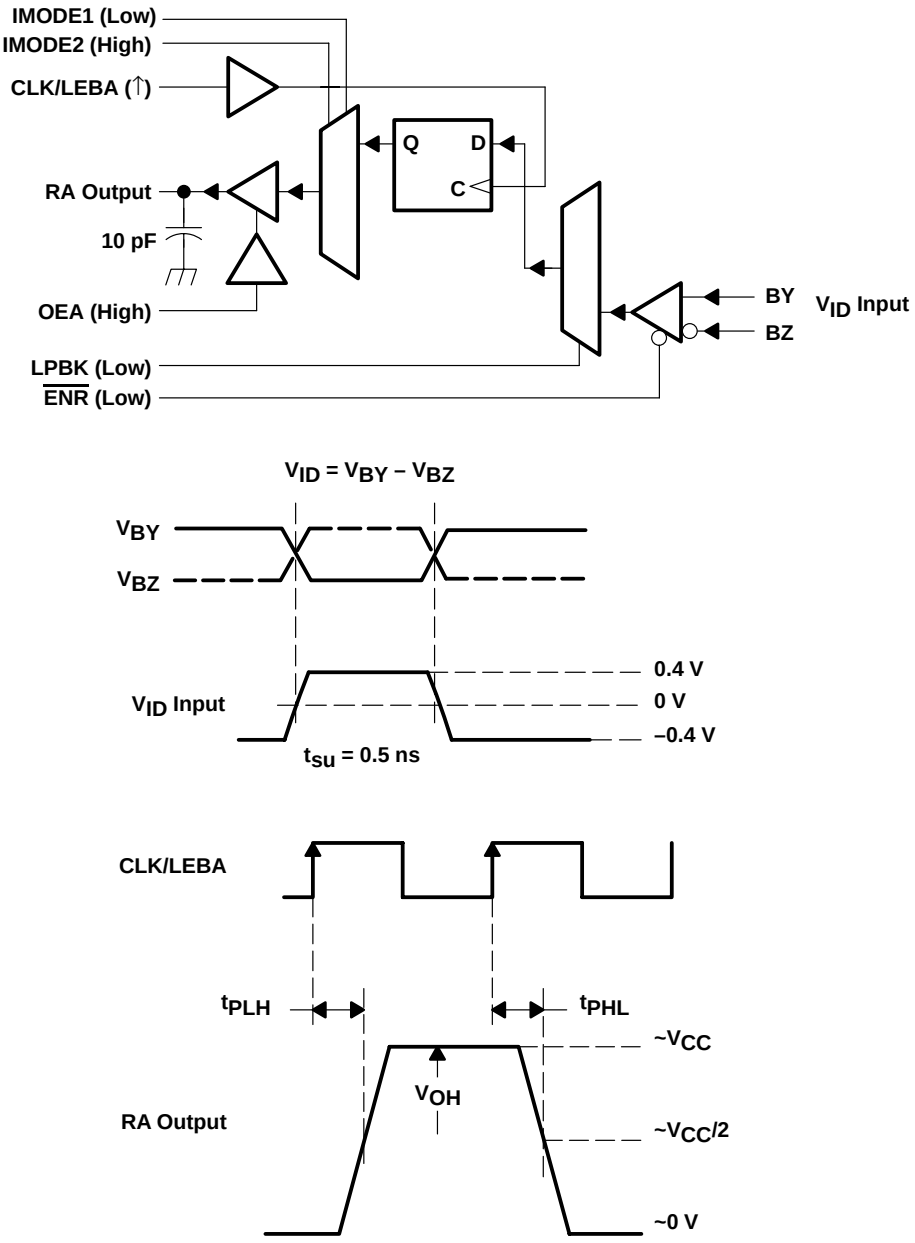


Figure 23. B-to-A Flip-Flop Mode Timing Circuit

APPLICATION INFORMATION

abstract

This section discusses electrical and operational topics not previously covered in this document, such as error detection and the device's ability to synchronize clock signals or manage data transfer between systems with different clock speeds. Basic applications of the analog and digital system diagnostic loopback functions and timing considerations are also analyzed. The SN65LVDM320 is resistant, although not immune, to the effect of setup and hold-time violations; therefore, the penalties of a violation are also examined.

introduction

The SN65LVDM320 is a versatile, multifunctional device with many applications. Low EMI, low crosstalk, and high differential-current output makes the SN65LVDM320 ideally suited for sensitive multipoint applications and low-impedance loads. Balanced differential signaling reduces noise coupling and allows high signaling rates. Balanced means that the current flowing in each signal line is equal but opposite in direction, resulting in a field canceling effect. This is one of the keys to the low-noise performance of an LVDS differential bus.

Balanced differential input signals eliminate induced noise with efficient common mode rejection (CMR). Internal chip design techniques reduce noise generated by inductive and capacitive mutual coupling, thereby increasing signal integrity. One of the techniques employed to reduce internal noise is the design of separate, dedicated grounds for the single-ended and differential circuitry incorporated within the device.

applications

The SN65LVDM320 may be used to connect major system blocks, including parallel processors, DRAMs, fast-cache SRAMs, and complex ASIC gate arrays. It effectively transceives the addresses, data, and control signals of these integrated-circuit elements to and from system blocks and backplanes.

The SN65LVDM320 not only facilitates extremely-high parallel burst-transfer rates, but in buffer mode, can move a constant stream of data at 475 Mbps through all of the eight channels simultaneously for a total data throughput exceeding 5 Gbps (transfer rate).

Deskewing clock signals is a requirement in many complex high-speed circuits, and the SN65LVDM320 performs this function at synchronous parallel transfers of 300 megatransfers per second (Mxferps) with very-low channel-to-channel output skew.

The SN65LVDM320 is also ideally suited for connecting system blocks operating at different clock speeds. When OEA and OEB are low, the system on the A-side of the device may be operated independently of the system on the B-side.

APPLICATION INFORMATION

diagnostics and error detection

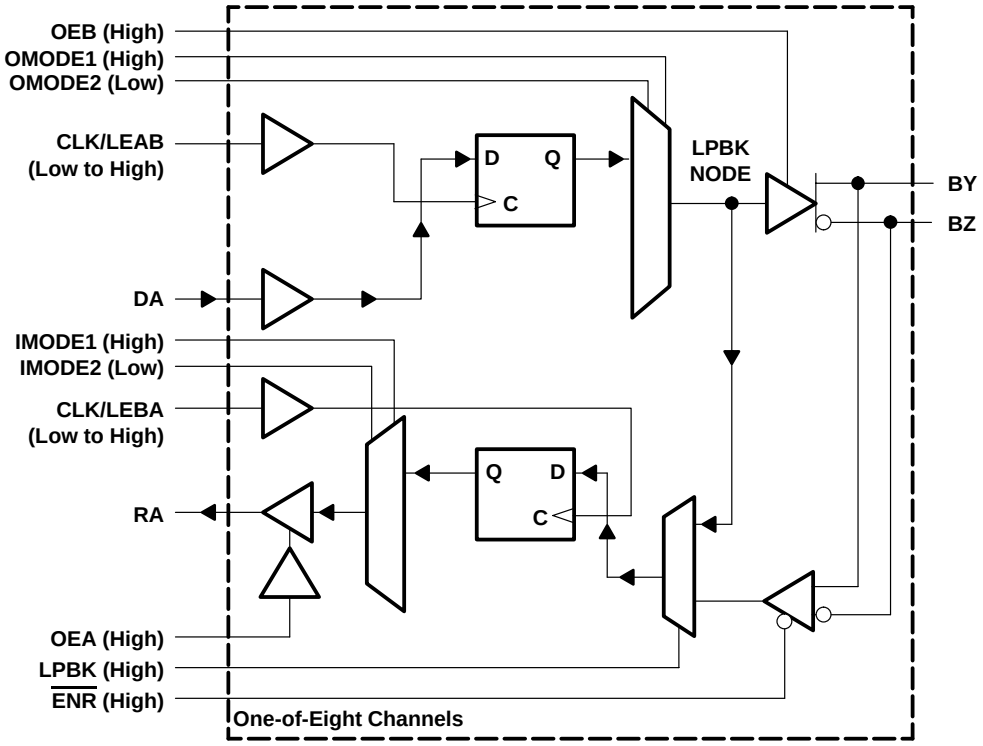


Figure 24. Loopback Error Detection

It is not a requirement that the driver be disabled (OEB low) during loopback. The driver may be enabled (OEB high) while loopback is engaged at any time without damaging the circuit. The loopback configuration in Figure 24 with the differential driver enabled provides error assessment in which transmitted data is looped back and compared to the original data by the microprocessor/microcontroller host. This may be implemented in buffer, flip-flop, or in the latch mode shown in Figure 24, and in accordance with the logic of Tables 2 and 3.

The SN65LVDM320 has been designed to improve a circuit's fault detection capabilities. 100% of the circuitry of the SN65LVDM320 may be functionally checked by activating the A-side and B-side loopback modes. With this functionality, a problem rack, card, circuit block, and even a chip can be located without the burden of boundary-scan protocols.

Traditionally, testability functions such as read-back, pattern insertion, and functional hardware test control require additional part count, connector pins, board space, power, and cost. However, the SN65LVDM320 provides full circuit observability and controllability within the package of an 8-bit LVDM transceiver.

APPLICATION INFORMATION

metastability in latches and flip-flops

Interfacing the asynchronous world to synchronous logic systems can cause problems. Latches and flip-flops, or basically, registers which are normally considered to have only two stable states (low and high) actually have a third state, the metastable state. Metastability can occur when the setup or the hold time is violated and the latch remains balanced in its threshold region. While in this metastable state, system noise can trigger either a high or low state.

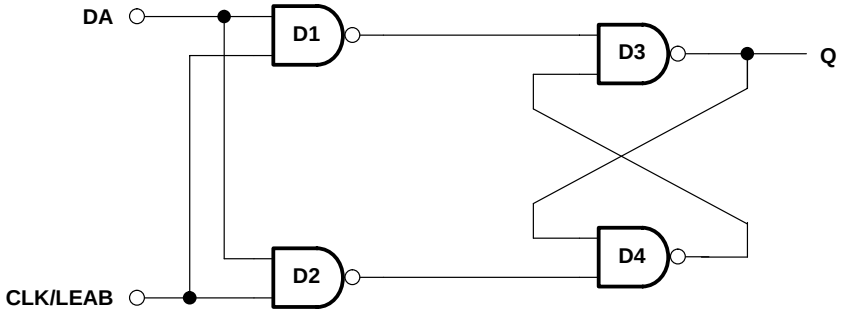


Figure 25. The A-Side to B-Side Signal Path

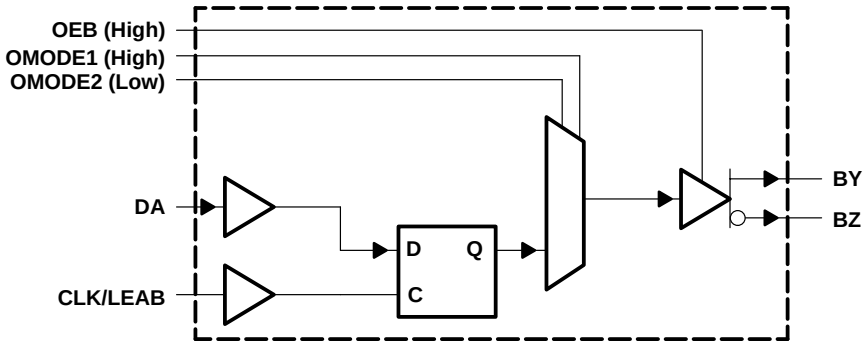


Figure 26. SN65LVDM320 D-Type latch

The SN65LVDM320 D-type latch circuitry of Figure 26 is shown in Figure 25. When data at pin DA is applied to D1, data is internally applied to D2. Therefore, when the CLK/LEAB pin is low, the outputs of D1 and D2 are high and the D3/D4 R-S latch is latched and stable. When CLK/LEAB transitions to high, the latch is transparent to the data input to DA and Q equals DA.

If data changes during the setup to hold time period, it is possible for the D1 and D2 outputs to be in the threshold region of D3 and D4. Under these conditions, D3 and D4 could be perfectly balanced in a metastable condition, allowing system noise to force the latch into a high or low state. This metastable condition can theoretically last as long as 25 ns and cause a system to crash if care is not taken with the asynchronous/synchronous interface. Although the SN65LVDM320 is metastable resistant by design, it is not entirely immune, and the setup and hold times must adhere to those listed in the timing requirements section.

APPLICATION INFORMATION

typical SN65LVDM320 output waveform—the eye pattern

Figure 27 displays a receiver's detection window in a typical LVDS output signal. When a receiver's differential-input voltage level drops, the system noise margin is reduced. Lowering the height enters the input voltage threshold of a receiver, eventually closing the eye and corrupting the data. Jitter content decreases the available time for accurate reception, and depending upon the application, may exceed 50% of the bit width without any problems. To read more about the terms and sources of jitter, see the *Jitter Analysis* application report, literature number SLLA075.

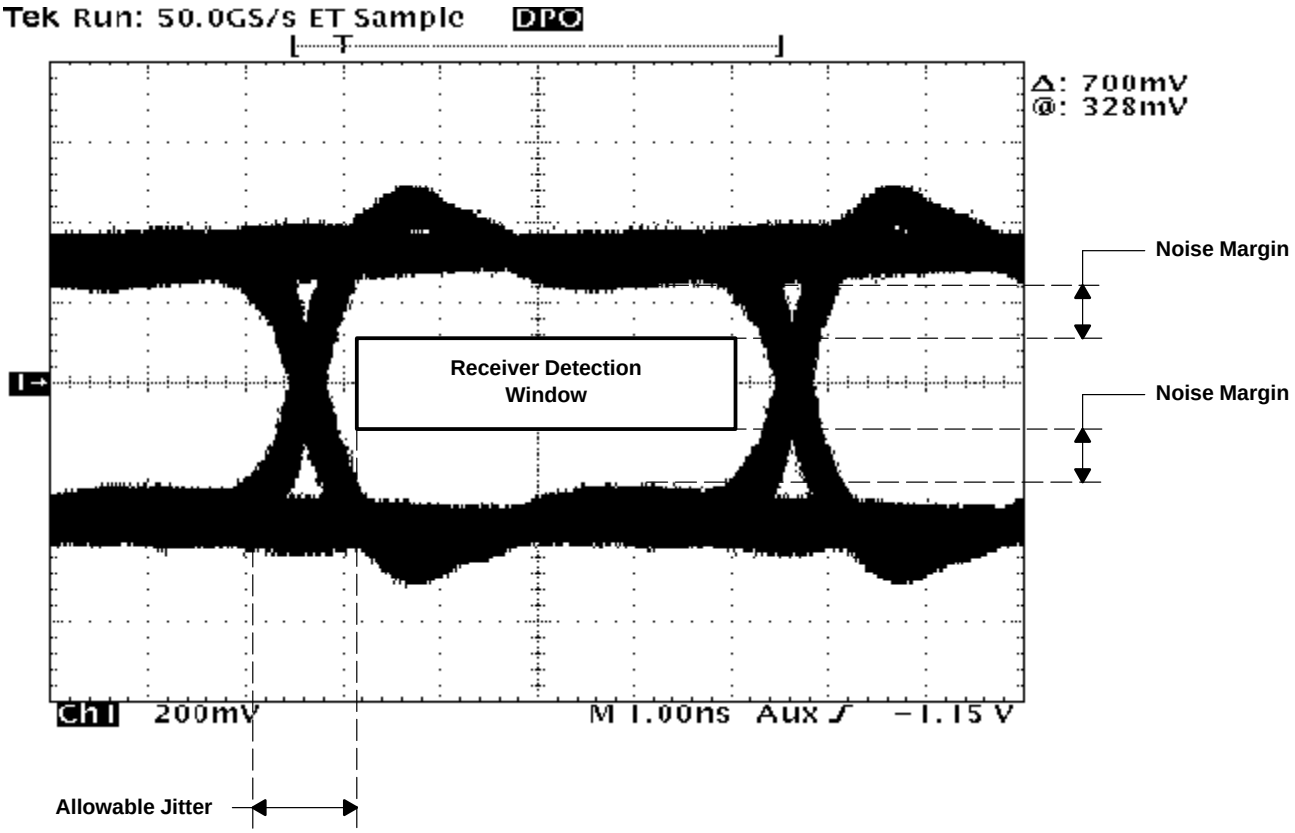


Figure 27. Receiver Detection Window in a Typical LVDS Driver Output

APPLICATION INFORMATION

typical SN65LVDM320 output waveform—the eye pattern (continued)

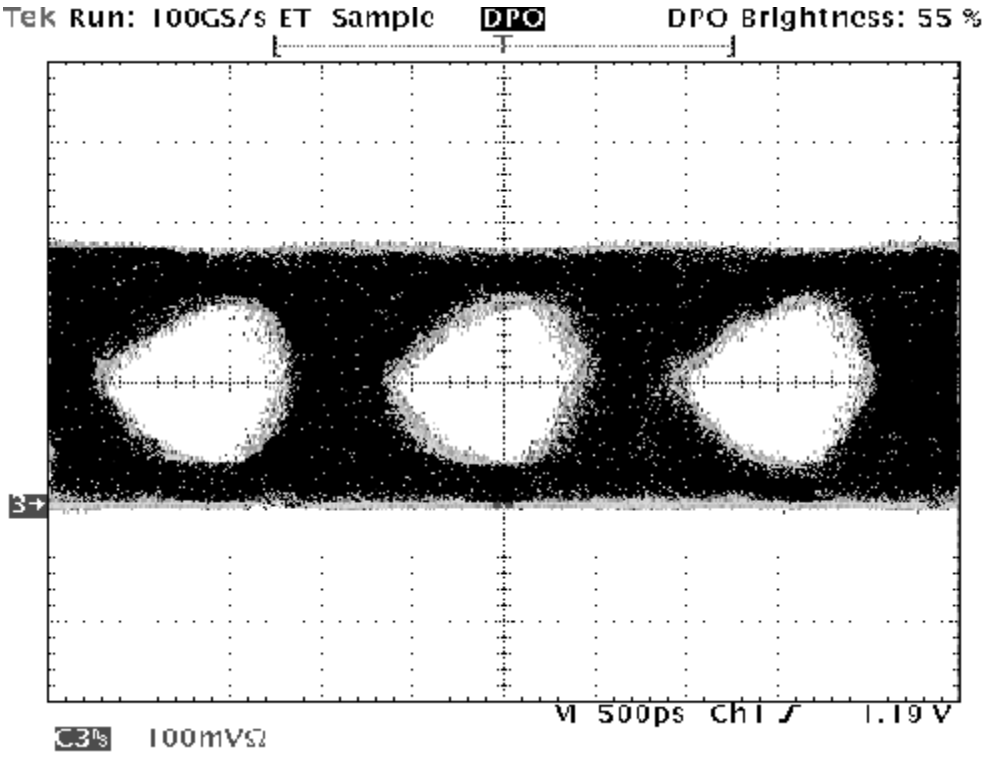


Figure 28. A Receiver Output With All Eight Channels at 630 Megatransfers per Second

The highest signaling rate measurable is 630 Mbps due to the limitations of the test circuit and equipment used to capture this oscillograph. It was captured while all eight channels were transmitting data in B-to-A buffer mode from the differential bus to the receiver. The measurement is taken from a receiver output test point across a 1.75-in, 50-Ω characteristic impedance trace of a TI bench evaluation board.

test equipment

HP 6236B dc power supply provides the required supply voltage of 3.3 V for the LVDM320. A Tektronix HFS9009 signal generator is employed as a nonreturn-to-zero (NRZ), pseudo-random binary sequence (PRBS) signal source for the LVDM320 and is adjusted as follows:

- Pattern: NRZ, PRBS
- Differential input high level: 1.6 V
- Differential input low level: 0.8 V
- Transition time: 800 ps

At high signaling rates, the influence of the equipment used to measure a signal of concern must be minimized. A Tektronix 794D oscilloscope and Tektronix P6247 differential probes are used in this test. Each probe has a bandwidth of 1 GHz and the probe capacitance is less than 1 pF.

APPLICATION INFORMATION

DRIVER BUFFER MODE
LOW-TO-HIGH-LEVEL PROPAGATION TIME
vs
FREE-AIR TEMPERATURE

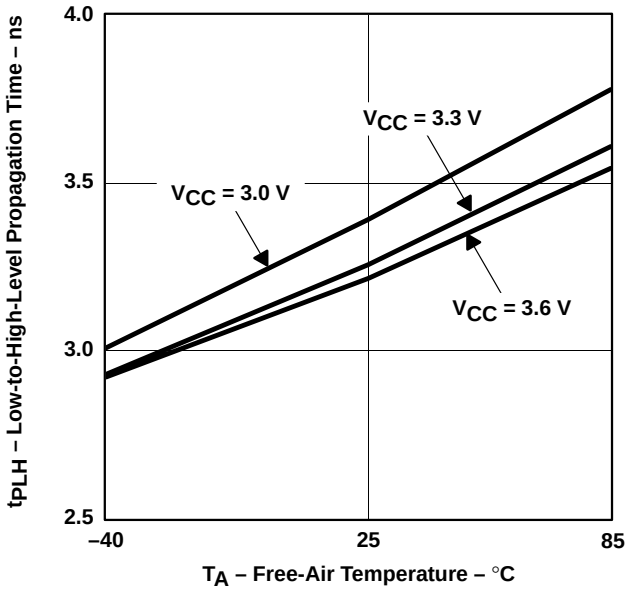


Figure 29

DRIVER BUFFER MODE
HIGH-TO-LOW-LEVEL PROPAGATION TIME
vs
FREE-AIR TEMPERATURE

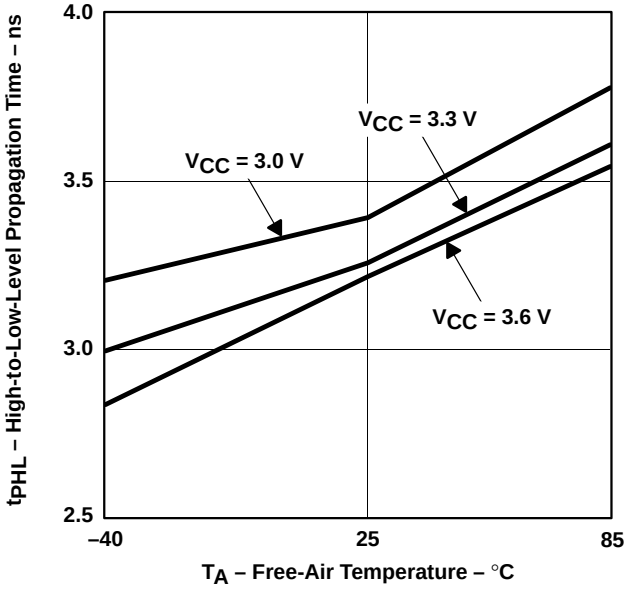


Figure 30

DRIVER LATCH MODE
LOW-TO-HIGH-LEVEL PROPAGATION TIME
vs
FREE-AIR TEMPERATURE

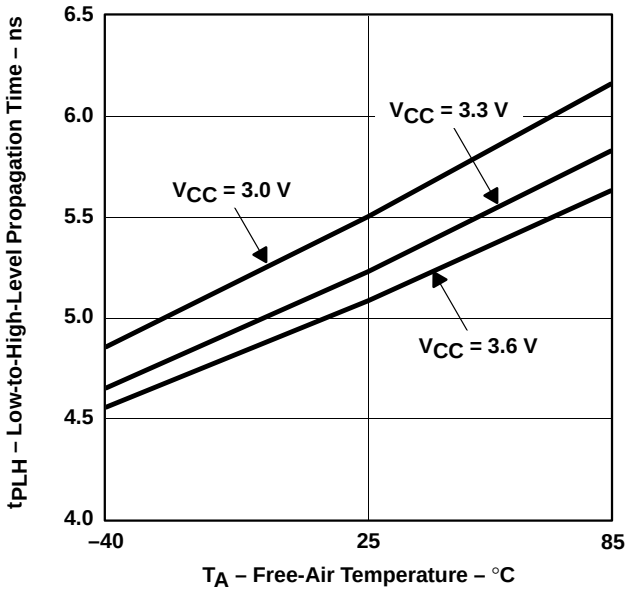


Figure 31

DRIVER LATCH MODE
HIGH-TO-LOW-LEVEL PROPAGATION TIME
vs
FREE-AIR TEMPERATURE

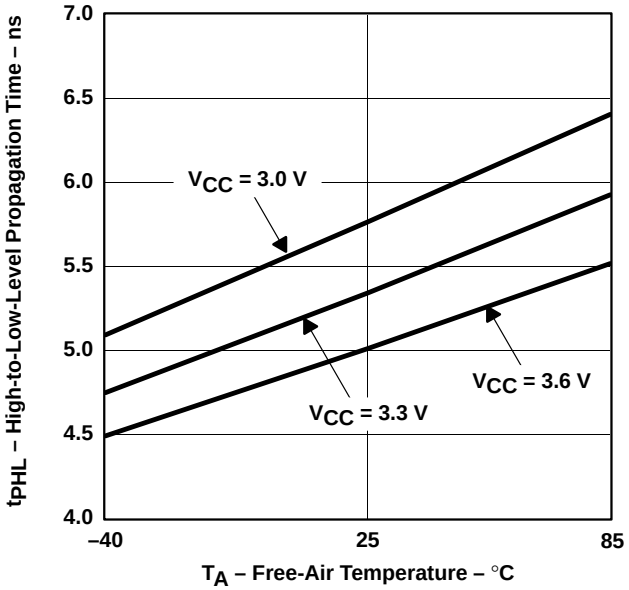


Figure 32

APPLICATION INFORMATION

DRIVER FLIP-FLOP MODE
LOW-TO-HIGH-LEVEL PROPAGATION TIME
vs
FREE-AIR TEMPERATURE

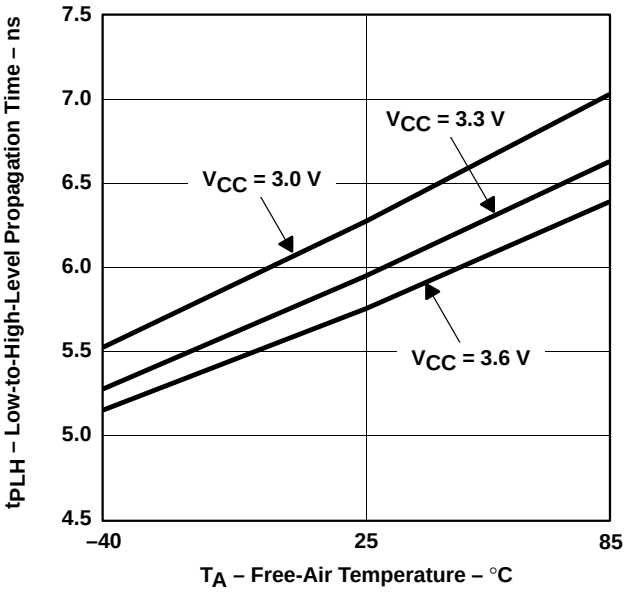


Figure 33

DRIVER FLIP-FLOP MODE
HIGH-TO-LOW-LEVEL PROPAGATION TIME
vs
FREE-AIR TEMPERATURE

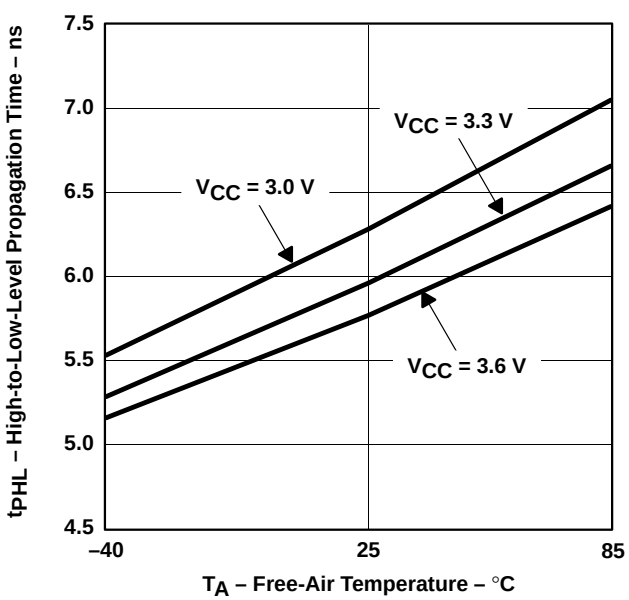


Figure 34

RECEIVER BUFFER MODE
LOW-TO-HIGH-LEVEL PROPAGATION TIME
vs
FREE-AIR TEMPERATURE

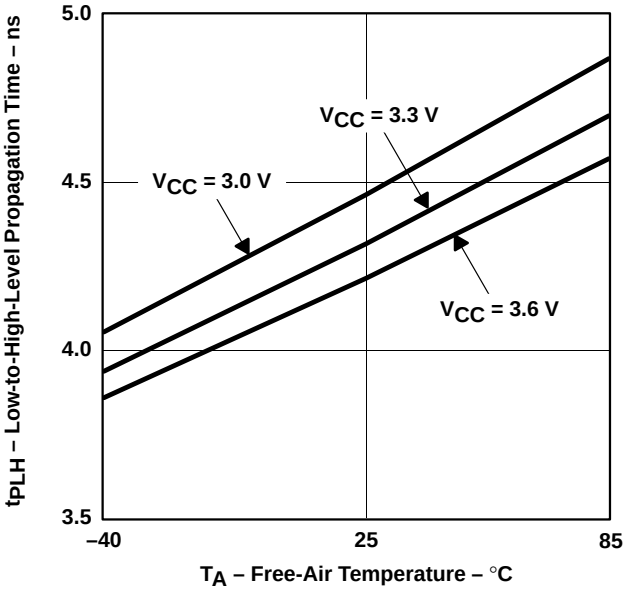


Figure 35

RECEIVER BUFFER MODE
HIGH-TO-LOW-LEVEL PROPAGATION TIME
vs
FREE-AIR TEMPERATURE

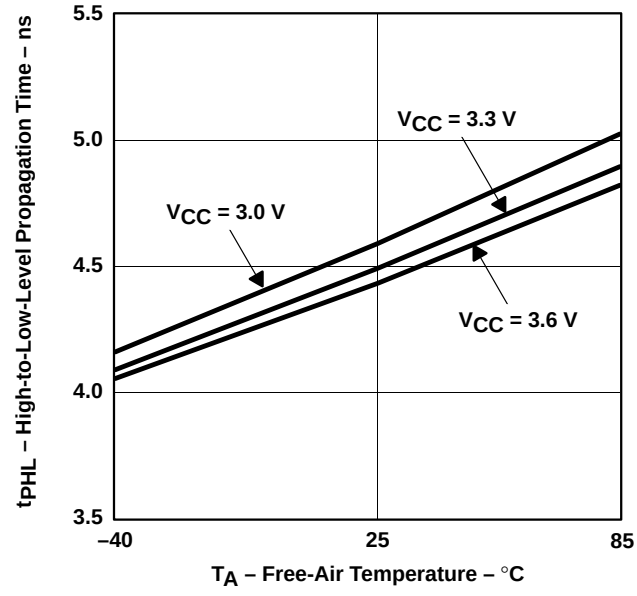


Figure 36

APPLICATION INFORMATION

RECEIVER LATCH MODE
LOW-TO-HIGH-LEVEL PROPAGATION TIME
vs
FREE-AIR TEMPERATURE

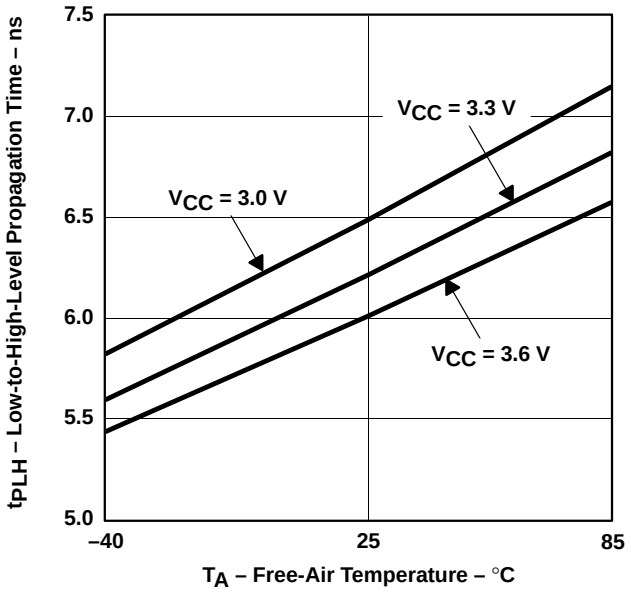


Figure 37

RECEIVER LATCH MODE
HIGH-TO-LOW-LEVEL PROPAGATION TIME
vs
FREE-AIR TEMPERATURE

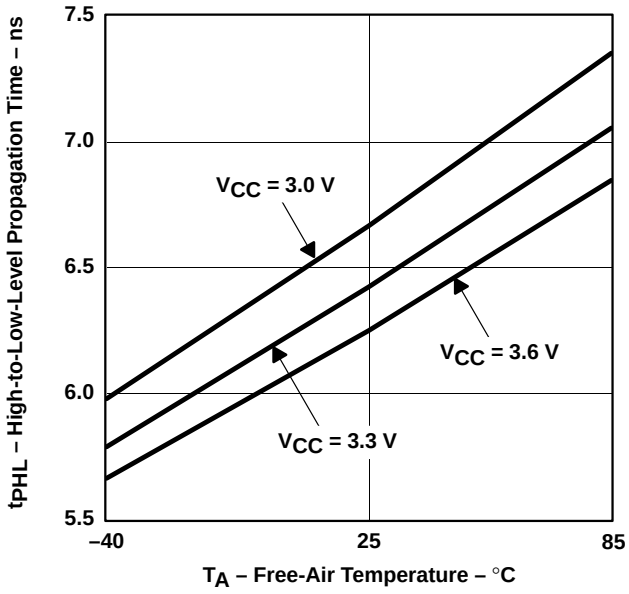


Figure 38

RECEIVER FLIP-FLOP MODE
LOW-TO-HIGH-LEVEL PROPAGATION TIME
vs
FREE-AIR TEMPERATURE

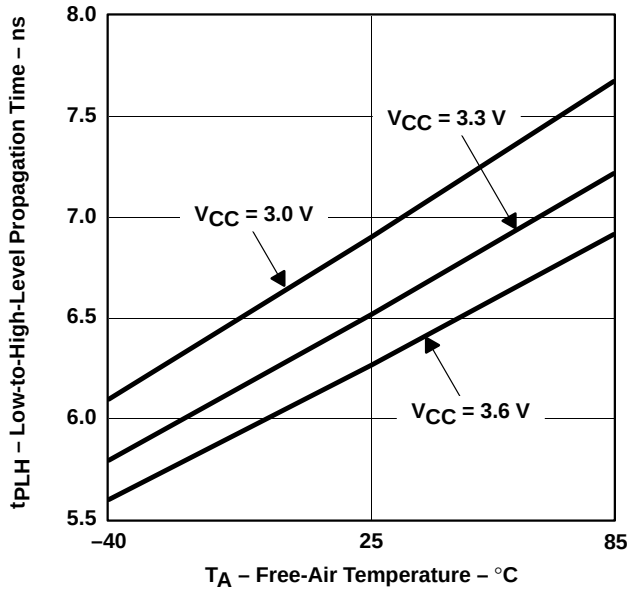


Figure 39

RECEIVER FLIP-FLOP MODE
HIGH-TO-LOW-LEVEL PROPAGATION TIME
vs
FREE-AIR TEMPERATURE

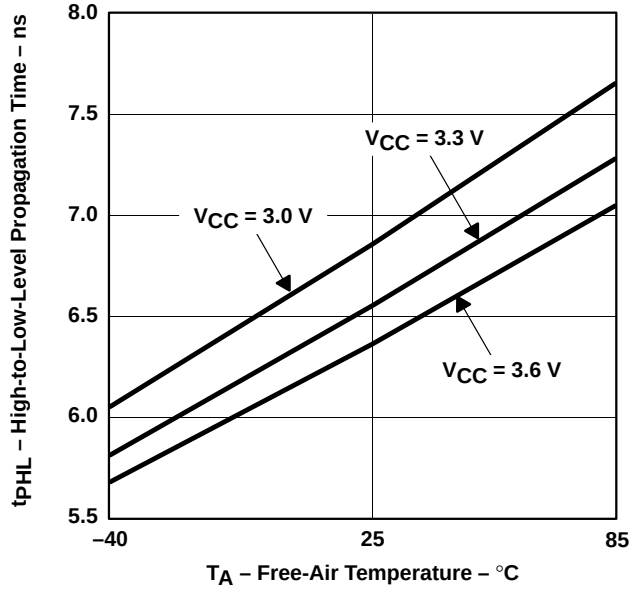


Figure 40

APPLICATION INFORMATION

DRIVER
LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

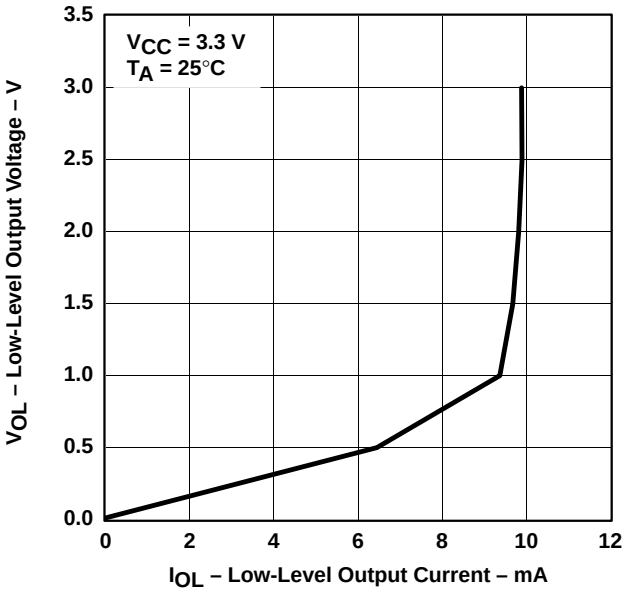


Figure 41

DRIVER
HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

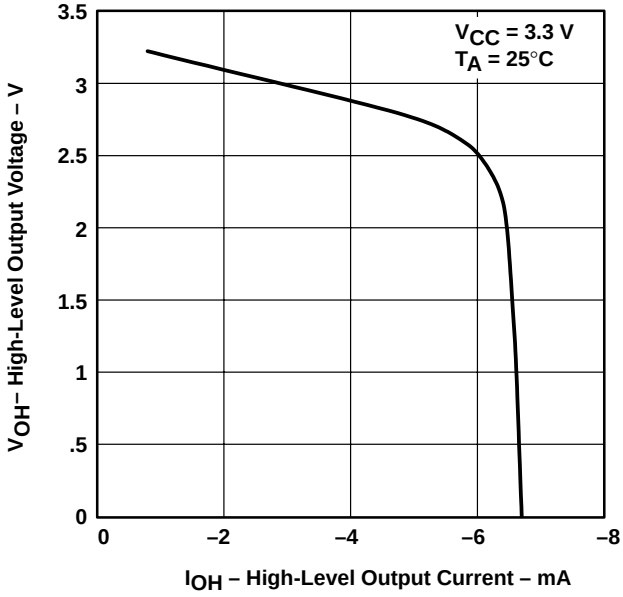


Figure 42

RECEIVER
LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

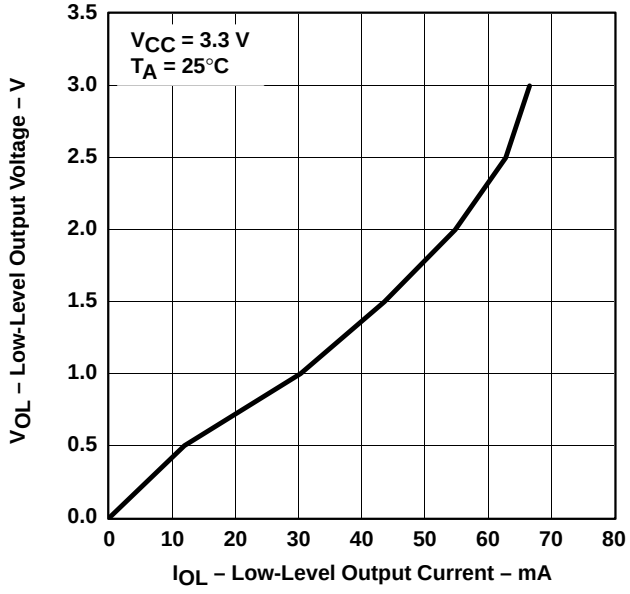


Figure 43

RECEIVER
HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

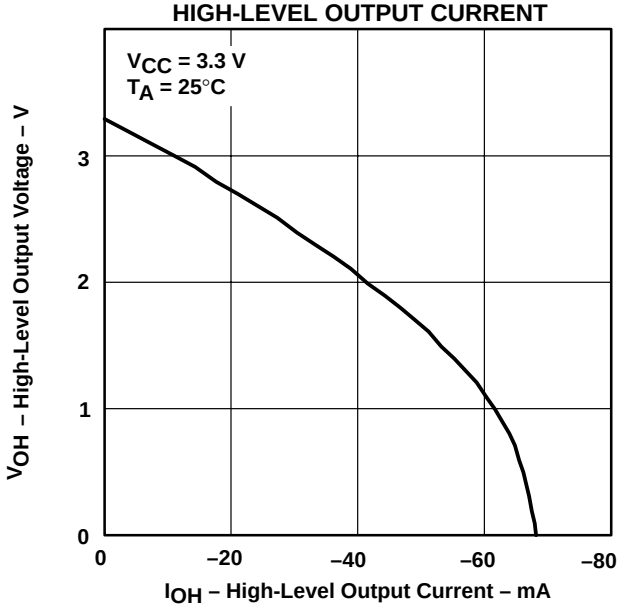


Figure 44

APPLICATION INFORMATION

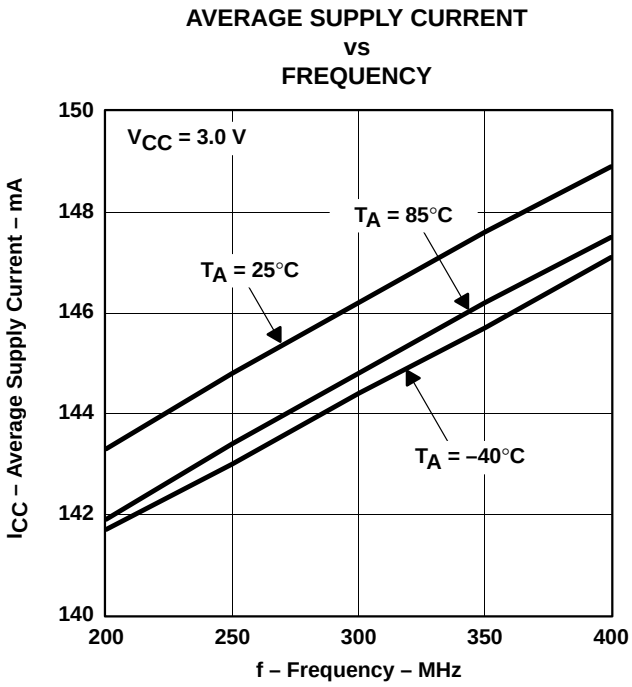


Figure 45

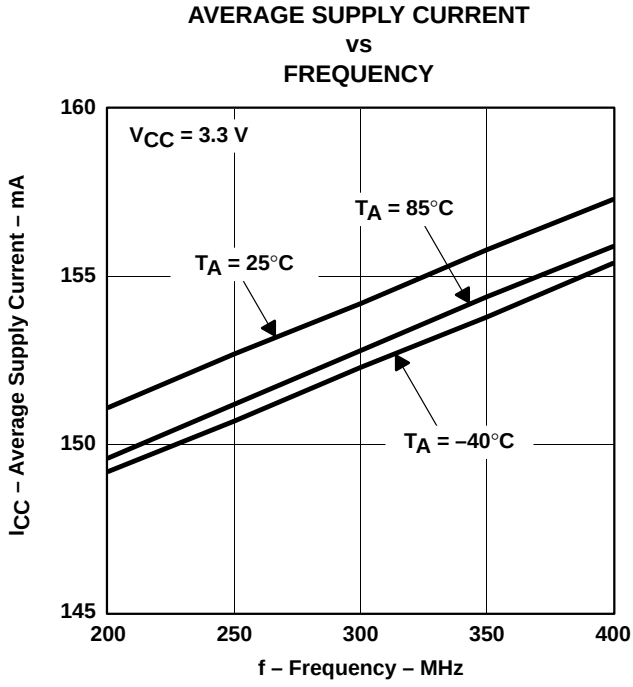


Figure 46

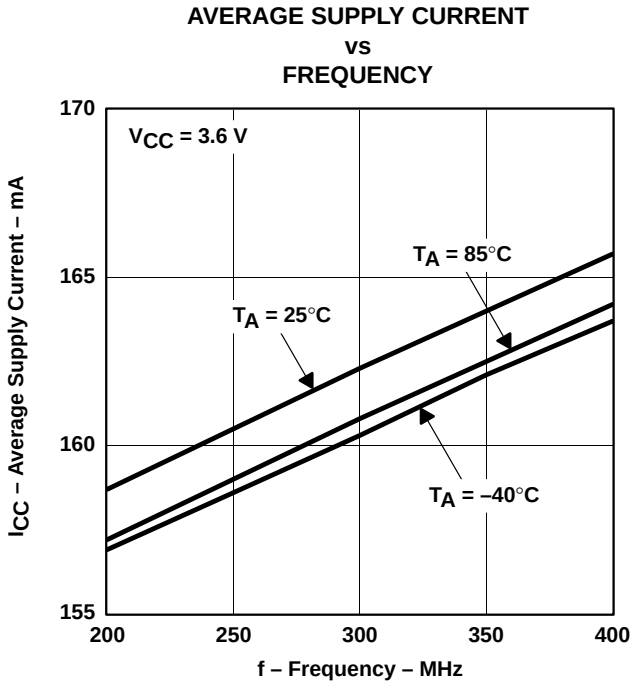
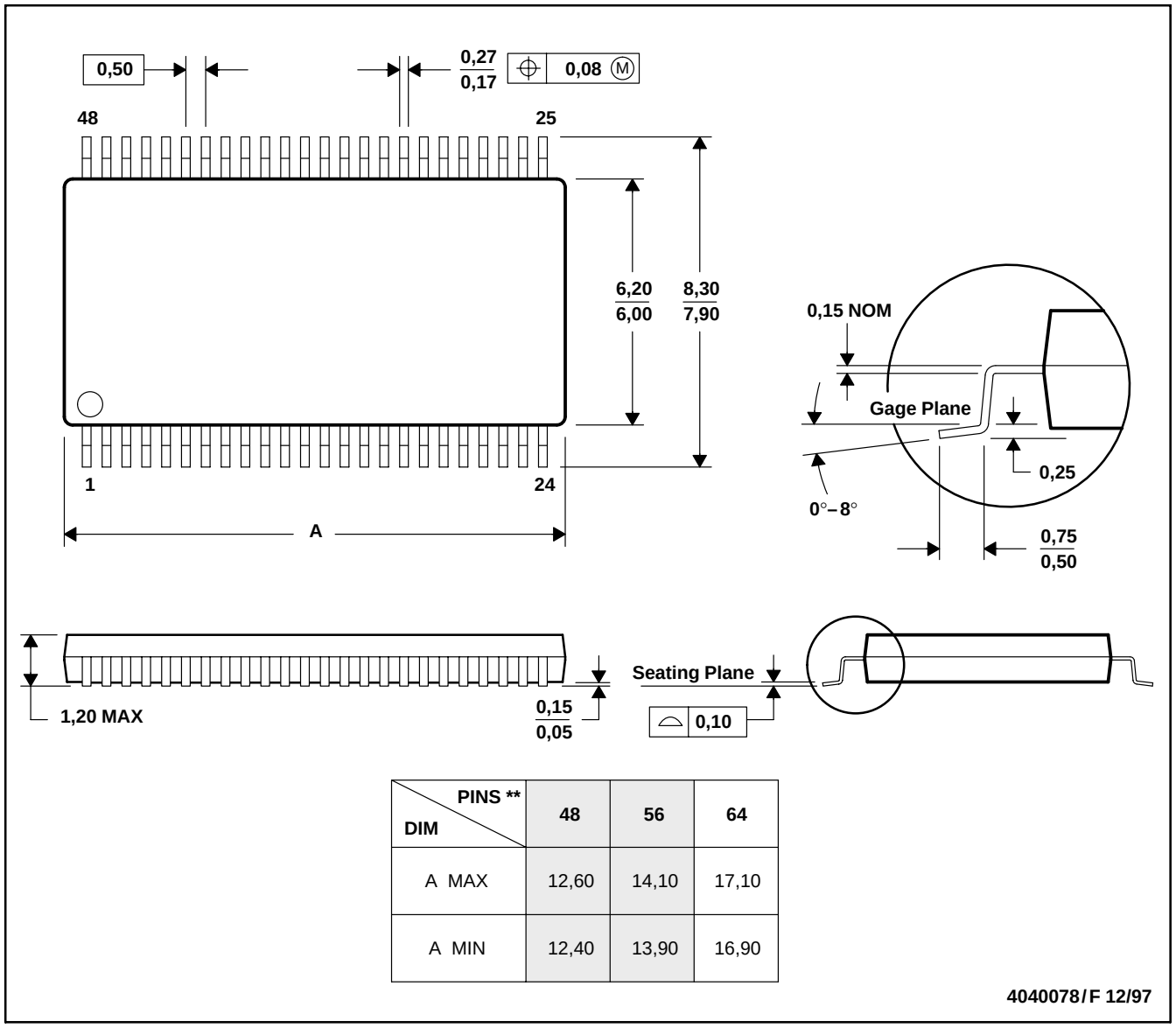


Figure 47

MECHANICAL DATA

DGG (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

48 PINS SHOWN



DIM \ PINS **	48	56	64
A MAX	12,60	14,10	17,10
A MIN	12,40	13,90	16,90

4040078/F 12/97

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold protrusion not to exceed 0,15.
D. Falls within JEDEC MO-153

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
SN65LVDM320DGG	ACTIVE	TSSOP	DGG	64	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
SN65LVDM320DGGR	ACTIVE	TSSOP	DGG	64	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
SN65LVDM320DGGRG4	ACTIVE	TSSOP	DGG	64	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS) or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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