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SLLS877A–DECEMBER 2007–REVISED JANUARY 2008

70-V Fault-Protected RS-485 Transceiver

FEATURES

- **Bus-Pin Fault Protection to > ±70 V**
- **Operation With 3.3-V to 5-V Supply Range**
- **±16 kV HBM Protection on Bus Pins**
- **Reduced Unit Load for up to 320 Nodes**
- **Failsafe Receiver for Open-Circuit, Short-Circuit and Idle-Bus Conditions**
- **Low Power Consumption**
  - **Low Standby Supply Current, 1 μA Max**
  - **I_{CC} 4 mA Quiescent During Operation**
- **Designed for RS-485 and RS-422 Networks**
- **Pin-Compatible With Industry-Standard SN75176**

APPLICATIONS

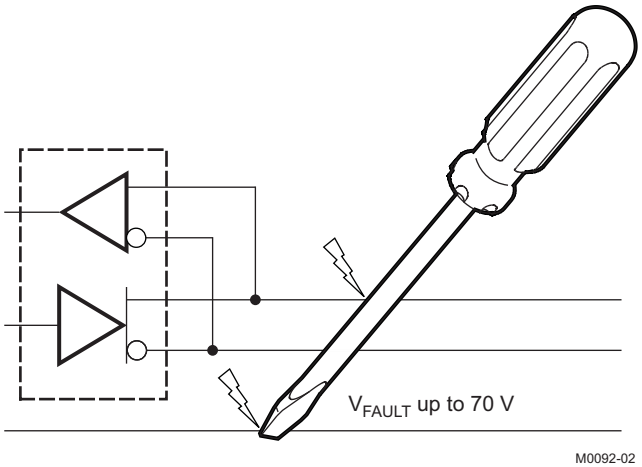
- **HVAC Networks**
- **Security Electronics**
- **Building Automation**
- **Telecomm Equipment**
- **Motion Control**
- **Industrial Networks**

DESCRIPTION

This device is designed to survive overvoltage faults such as direct shorts to power supplies, mis-wiring faults, connector failures, cable crushes, and tool mis-applications. The internal current-limit circuits allow fault survivability without causing the high bus currents that otherwise might damage external components or power supplies. It is also robust to ESD events, with high levels of protection to the JEDEC or IEC human-body-model specification.

This device combines a differential driver and a differential receiver, which operate from a single power supply. The driver differential outputs and the receiver differential inputs are connected internally to form a bus port suitable for half-duplex (two-wire bus) communication. This port features a wide common-mode voltage range, making the devices suitable for multipoint applications over long cable runs. This device is characterized from –40°C to 125°C. The SN65HVD1781 is pin-compatible with the industry-standard SN75176 transceiver, making it a drop-in upgrade for most devices.

The HVD1781 is fully compliant with ANSI TIA/EIA 485-A with a 5-V supply and can operate with a 3.3-V supply with reduced driver output voltage for low-power applications.

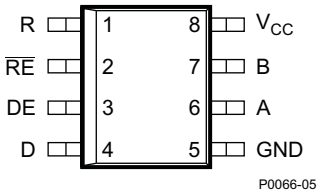


M0092-02

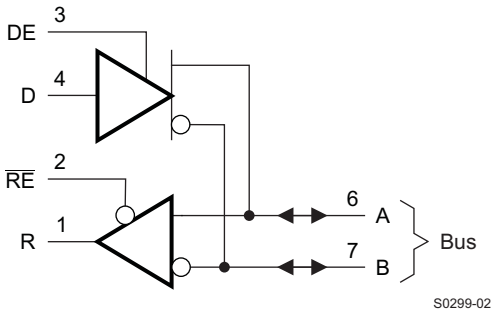
Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

SN65HVD1781
D Package
(Top View)



LOGIC DIAGRAM (POSITIVE LOGIC)



DEVICE INFORMATION

DRIVER FUNCTION TABLE

Input	Enable	Outputs		Driver State
D	**DE**	**A**	**B**	
H	H	H	L	Actively drive bus High
L	H	L	H	Actively drive bus Low
X	L	Z	Z	Driver disabled (1)
X	OPEN	Z	Z	Driver disabled by default (1)
OPEN	H	H	L	Actively drive bus High by default

(1) When both the driver and receiver are disabled, the device enters a low-power standby mode.

RECEIVER FUNCTION TABLE

Differential Input	Enable	Output	Receiver State
$V_{ID} = V_A - V_B$	**RE**	**R**	
$V_{IT+} < V_{ID}$	L	H	Receive valid bus High
$V_{IT-} < V_{ID} < V_{IT+}$	L	?	Indeterminate bus state
$V_{ID} < V_{IT-}$	L	L	Receive valid bus Low
X	H	Z	Receiver disabled (1)
X	OPEN	Z	Receiver disabled by default (1)
Open-circuit bus	L	H	Fail-safe high output
Short-circuit bus	L	H	Fail-safe high output
Idle (terminated) bus	L	H	Fail-safe high output

(1) When both the driver and receiver are disabled, the device enters a low-power standby mode.

ABSOLUTE MAXIMUM RATINGS(1)

		VALUE	UNIT
V_{CC}	Supply voltage	–0.5 to 7	V
	Voltage range at A and B inputs	–70 to 70	V
	Input voltage range at any logic pin	–0.3 to V_{CC} + 0.3	V
	Voltage input range, transient pulse, A and B, through 100 Ω	–70 to 70	V
	Receiver output current	–24 to 24	mA
T_J	Junction temperature	170	°C
	Continuous total power dissipation	See Dissipation Rating Table	
	IEC 60749-26 ESD (human-body model), bus terminals and GND	±16	kV
	JEDEC Standard 22, Test Method A114 (human-body model), bus terminals and GND	±16	kV
	JEDEC Standard 22, Test Method A114 (human-body model), all pins	±4	kV
	JEDEC Standard 22, Test Method C101 (charged-device model), all pins	±2	kV
	JEDEC Standard 22, Test Method A115 (machine model), all pins	±400	V

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

PACKAGE DISSIPATION RATINGS

PACKAGE(1)	JEDEC THERMAL MODEL	T_A < 25°C RATING	DERATING FACTOR ABOVE T_A = 25°C	T_A = 85°C RATING	T_A = 105°C RATING	T_A = 125°C RATING (3.3 V ONLY)
SOIC (D) 8-pin	High-K	905 mW	7.25 mW/°C	470 mW	325 mW	180 mW
	Low-K	516 mW	4.1 mW/°C	268 mW	186 mW	103 mW

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.

RECOMMENDED OPERATING CONDITIONS

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		3.15	5	5.5	V
V_I	Input voltage at any bus terminal (separately or common mode)(1)		–7		12	V
V_{IH}	High-level input voltage (driver, driver enable, and receiver enable inputs)		2		V_{CC}	V
V_{IL}	Low-level input voltage (driver, driver enable, and receiver enable inputs)		0		0.8	V
V_{ID}	Differential input voltage		–12		12	V
I_O	Output current, driver		–60		60	mA
	Output current, receiver		–8		8	mA
R_L	Differential load resistance		54	60		Ω
C_L	Differential load capacitance			50		pF
$1/t_{UI}$	Signaling rate				1	Mbps
T_A	Operating free-air temperature (See application section for thermal information)	5-V supply	–40		105	°C
		3.3-V supply	–40		125	
T_J	Junction temperature		–40		150	°C

(1) By convention, the least positive (most negative) limit is designated as minimum in this data sheet.

ELECTRICAL CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$\|V_{OD}\|$	Driver differential output voltage magnitude	R_L = 60 Ω, 4.75 V ≤ V_{CC} 375 Ω on each output to –7 V to 12 V, T_A < 85°C, See Figure 1		1.5			V
		R_L = 60 Ω, 4.75 V ≤ V_{CC} 375 Ω on each output to –7 V to 12 V, T_A < 125°C, See Figure 1		1.4			
		R_L = 54 Ω, 4.75 V ≤ V_{CC} ≤ 5.25 V, T_A < 85°C		1.7	2		
		R_L = 54 Ω, 4.75 V ≤ V_{CC} ≤ 5.25 V, T_A < 125°C		1.5			
		R_L = 54 Ω, 3.15 V ≤ V_{CC} ≤ 3.45 V		0.8	1		
		R_L = 100 Ω, 4.75 V ≤ V_{CC} ≤ 5.25 V, T_A < 85°C		2.2	2.5		
		R_L = 100 Ω, 4.75 V ≤ V_{CC} ≤ 5.25 V, T_A < 125°C		2			
$\Delta\|V_{OD}\|$	Change in magnitude of driver differential output voltage	R_L = 54 Ω		–50	0	50	mV
$V_{OC(SS)}$	Steady-state common-mode output voltage			1	V_{CC}/2	3	V
ΔV_{OC}	Change in differential driver output common-mode voltage			–50	0	50	mV
$V_{OC(PP)}$	Peak-to-peak driver common-mode output voltage	Center of two 27-Ω load resistors, See Figure 2			500		mV
C_{OD}	Differential output capacitance				23		pF
V_{IT+}	Positive-going receiver differential input voltage threshold				–100	–35	mV
$V_{IT–}$	Negative-going receiver differential input voltage threshold			–180	–150		
V_{HYS}	Receiver differential input voltage threshold hysteresis (V_{IT+} – $V_{IT–}$)			30	50		
V_{OH}	Receiver high-level output voltage	I_{OH} = –8 mA		2.4	V_{CC} – 0.3		V
V_{OL}	Receiver low-level output voltage	I_{OL} = 8 mA, T_A < 85°C			0.2	0.4	V
		I_{OL} = 8 mA, T_A < 125°C				0.5	
$I_{I(LOGIC)}$	Driver input, driver enable, and receiver enable input current			–50		50	µA
I_{OZ}	Receiver output high-impedance current	V_O = 0 V or V_{CC}, $\overline{RE}$ at V_{CC}		–1		1	µA
I_{OS}	Driver short-circuit output current			–150		150	mA
$I_{I(BUS)}$	Bus input current (disabled driver)	V_{CC} = 3.15 to 5.5 V or V_{CC} = 0 V, DE at 0 V	V_I = 12 V		75	100	µA
			V_I = –7 V	–60	–40		

ELECTRICAL CHARACTERISTICS (continued)

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
I_{CC}	Supply current (quiescent)	Driver and receiver enabled	DE = V_{CC}, RE = GND, no load		4	6	mA
		Driver enabled, receiver disabled	DE = V_{CC}, RE = V_{CC}, no load		3	5	
		Driver disabled, receiver enabled	DE = GND, RE = GND, no load		2	4	
		Driver and receiver disabled, standby mode	DE = GND, D = open RE = V_{CC}, no load, T_A < 85°C		0.15	1	µA
			DE = GND, D = open RE = V_{CC}, no load, T_A < 125°C			12	
Supply current (dynamic)		See *Typical Characteristics* section					

SWITCHING CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
DRIVER							
t_r, t_f	Driver differential output rise/fall time	R_L = 54 Ω, C_L = 50 pF, See Figure 3		70		300	ns
t_{PHL}, t_{PLH}	Driver propagation delay					170	ns
$t_{SK(P)}$	Driver differential output pulse skew, $\|t_{PHL} - t_{PLH}\|$					20	ns
t_{PHZ}, t_{PLZ}	Driver disable time		See Figure 4 and Figure 5			0.1	µs
t_{PZH}, t_{PZL}	Driver enable time	Receiver enabled				260	ns
		Receiver disabled				5	µs
RECEIVER							
t_r, t_f	Receiver output rise/fall time	C_L = 15 pF, See Figure 6			4	10	ns
t_{PHL}, t_{PLH}	Receiver propagation delay time				100	150	ns
$t_{SK(P)}$	Receiver output pulse skew, $\|t_{PHL} - t_{PLH}\|$				6	10	ns
t_{PLZ}, t_{PHZ}	Receiver disable time	Driver enabled, See Figure 7			15	50	ns
$t_{PZL(1)}$, $t_{PZH(1)}$ $t_{PZL(2)}$, $t_{PZH(2)}$	Receiver enable time	Driver enabled, See Figure 7			80	200	ns
		Driver disabled, See Figure 8			3	5	µs

THERMAL INFORMATION

PARAMETER		TEST CONDITIONS	VALUE	UNIT
$R_{\theta JA}$ Junction-to-ambient thermal resistance (no airflow)	SOIC-8	JEDEC high-K model	138	°C/W
		JEDIC low-K model	242	
	DIP-8	JEDEC high-K model	59	
		JEDIC low-K model	128	
	SOIC-14	JEDEC high-K model	95	
		JEDIC low-K model	168	
$R_{\theta JB}$ Junction-to-board thermal resistance	SOIC-8		62	°C/W
	DIP-8		39	
	SOIC-14		40	
$R_{\theta JC}$ Junction-to-case thermal resistamce	SOIC-8		61	°C/W
	DIP-8		61	
	SOIC-14		44	
P_D Power dissipation		V_{CC} = 3.6V, T_J = 150°C, R_L = 300 Ω, C_L = 50 pF (driver), C_L = 15 pF (receiver) 3.3-V supply, unterminated(1)	75	mW
		V_{CC} = 3.6V, T_J = 150°C, R_L = 100 Ω, C_L = 50 pF (driver), C_L = 15 pF (receiver) 3.3-V supply, RS-422 load(1)	95	
		V_{CC} = 3.6V, T_J = 150°C, R_L = 54 Ω, C_L = 50 pF (driver), C_L = 15 pF (receiver) 3.3-V supply, RS-485 load(1)	115	
		V_{CC} = 5.5V, T_J = 150°C, R_L = 300 Ω, C_L = 50 pF (driver), C_L = 15 pF (receiver) 5-V supply, unterminated(1)	290	
		V_{CC} = 5.5V, T_J = 150°C, R_L = 100 Ω, C_L = 50 pF (driver), C_L = 15 pF (receiver) 5-V supply, RS-422 load(1)	320	
		V_{CC} = 5.5V, T_J = 150°C, R_L = 54 Ω, C_L = 50 pF (driver), C_L = 15 pF (receiver) 5-V supply, RS-485 load(1)	400	
T_{SD} Thermal-shutdown junction temperature			170	°C

(1) Driver and receiver enabled, 50% duty cycle square-wave signal at signaling rate: 1 Mbps.

PARAMETER MEASUREMENT INFORMATION

Input generator rate is 100 kbps, 50% duty cycle, rise and fall times less than 6 nsec, output impedance 50 Ω.

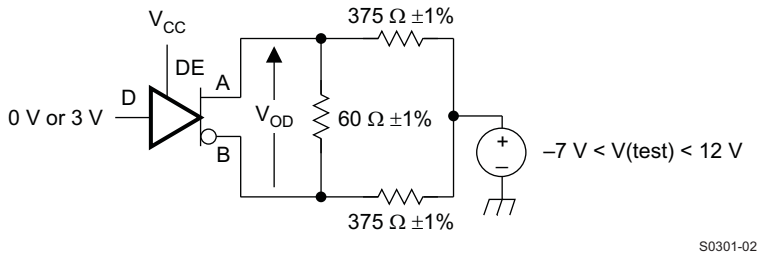


Figure 1. Measurement of Driver Differential Output Voltage With Common-Mode Load

PARAMETER MEASUREMENT INFORMATION (continued)

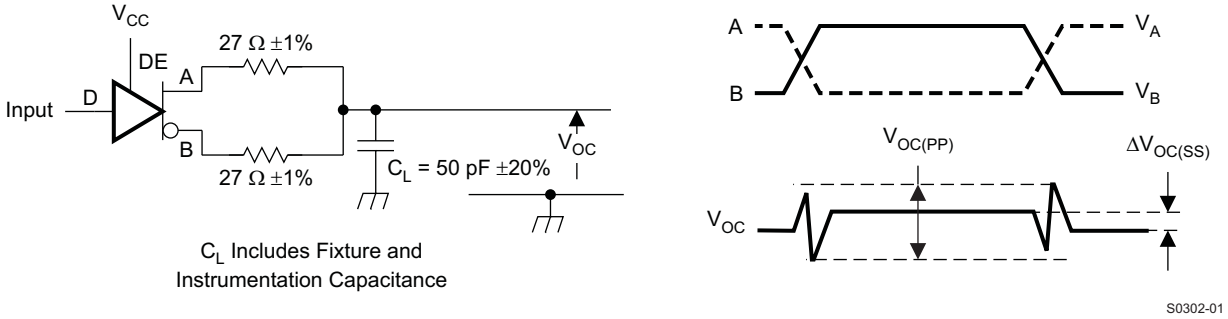


Figure 2. Measurement of Driver Differential and Common-Mode Output With RS-485 Load

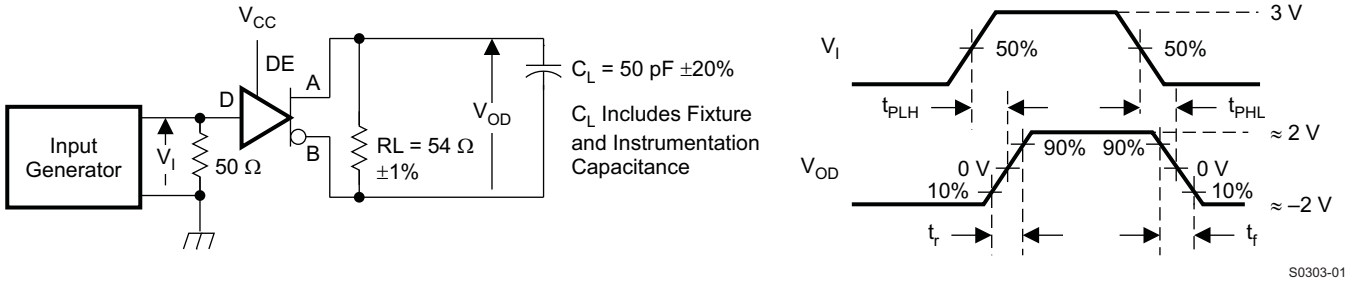
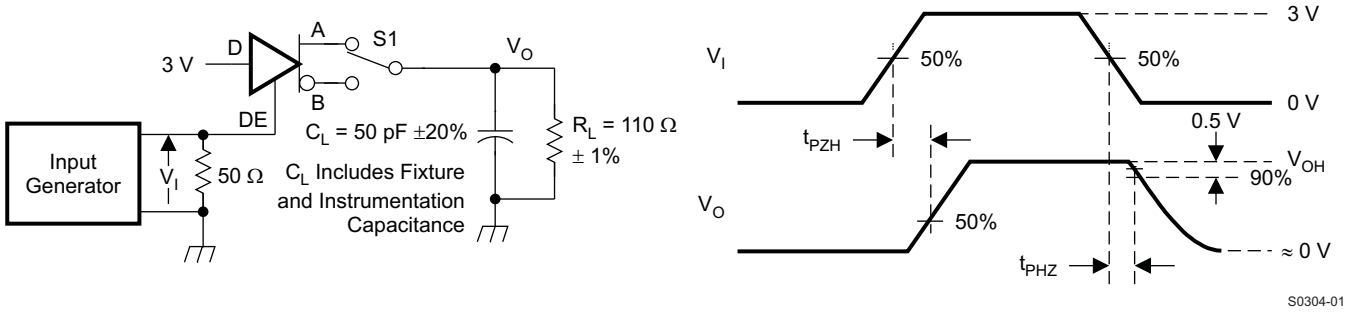
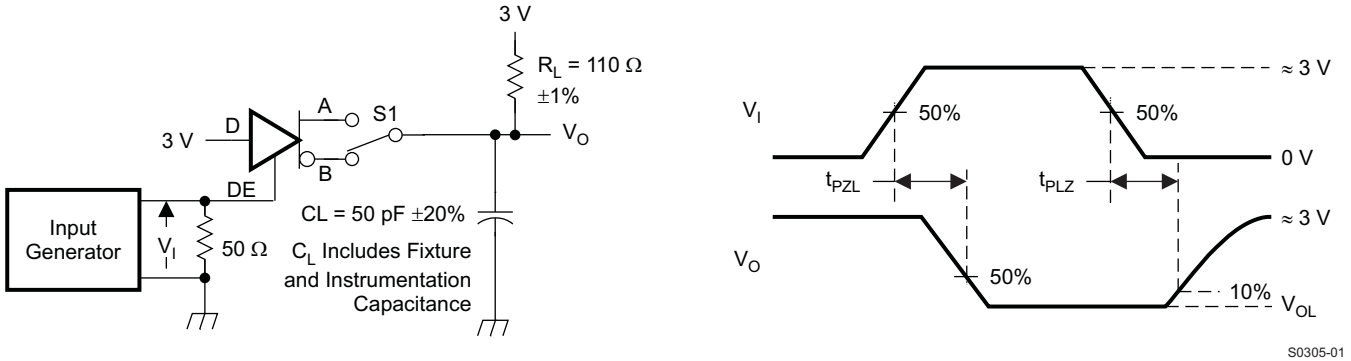


Figure 3. Measurement of Driver Differential Output Rise and Fall Times and Propagation Delays



NOTE: D at 3 V to test non-inverting output, D at 0 V to test inverting output.

Figure 4. Measurement of Driver Enable and Disable Times With Active High Output and Pulldown Load



NOTE: D at 0 V to test non-inverting output, D at 3 V to test inverting output.

Figure 5. Measurement of Driver Enable and Disable Times With Active-Low Output and Pullup Load

PARAMETER MEASUREMENT INFORMATION (continued)

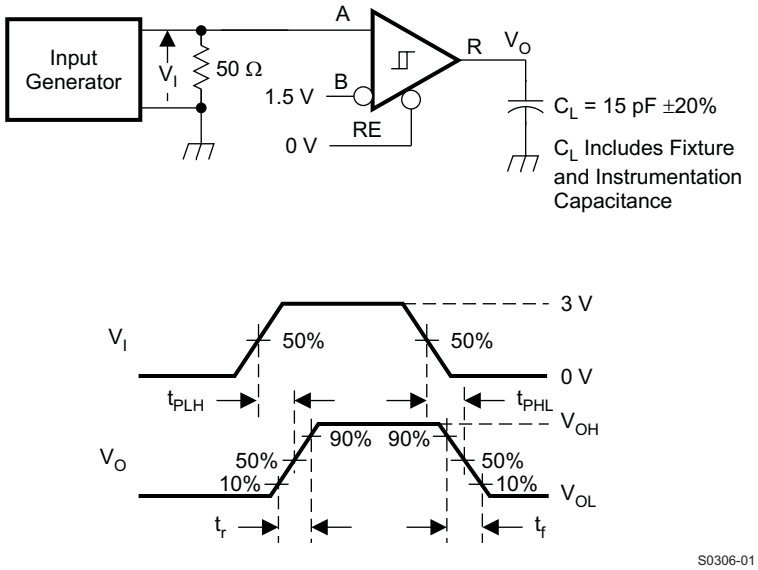


Figure 6. Measurement of Receiver Output Rise and Fall Times and Propagation Delays

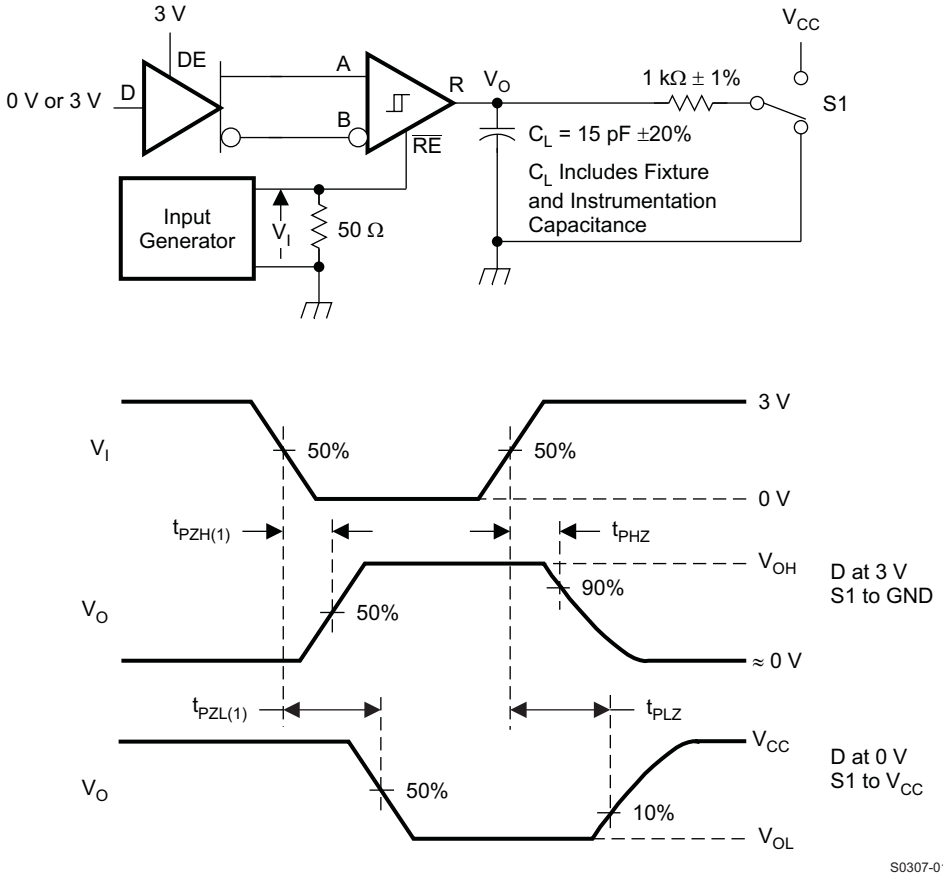


Figure 7. Measurement of Receiver Enable/Disable Times With Driver Enabled

PARAMETER MEASUREMENT INFORMATION (continued)

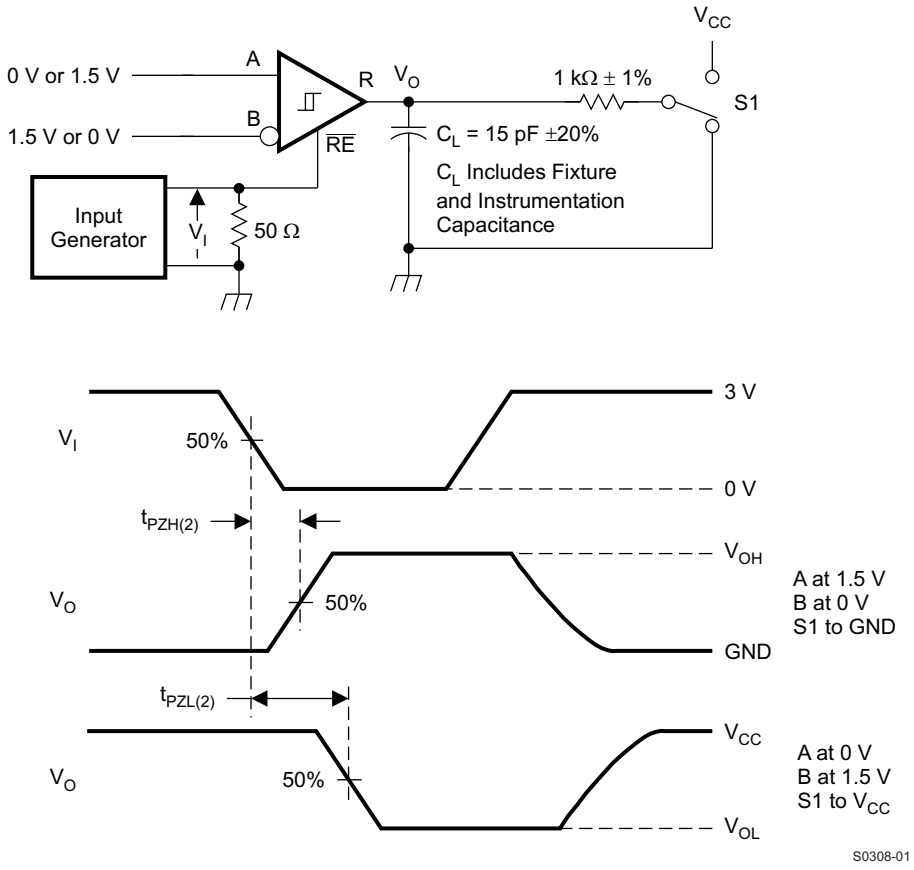


Figure 8. Measurement of Receiver Enable Times With Driver Disabled

TYPICAL CHARACTERISTICS

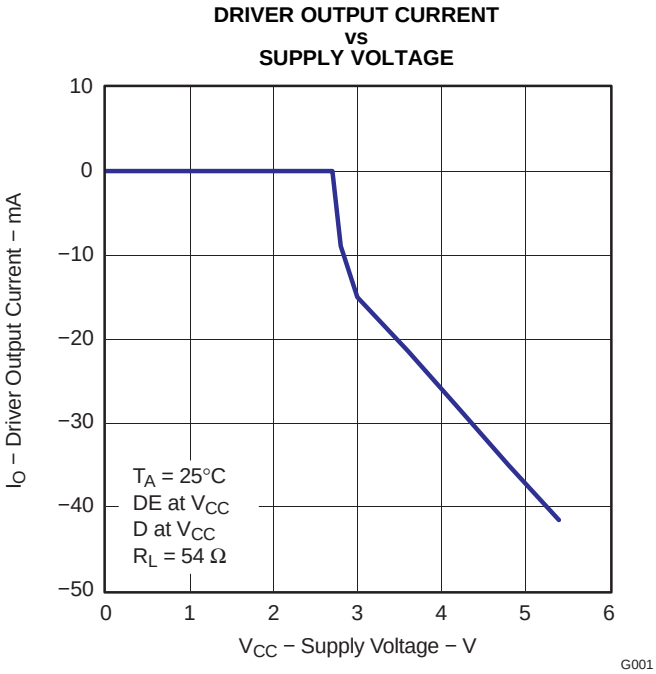


Figure 9.

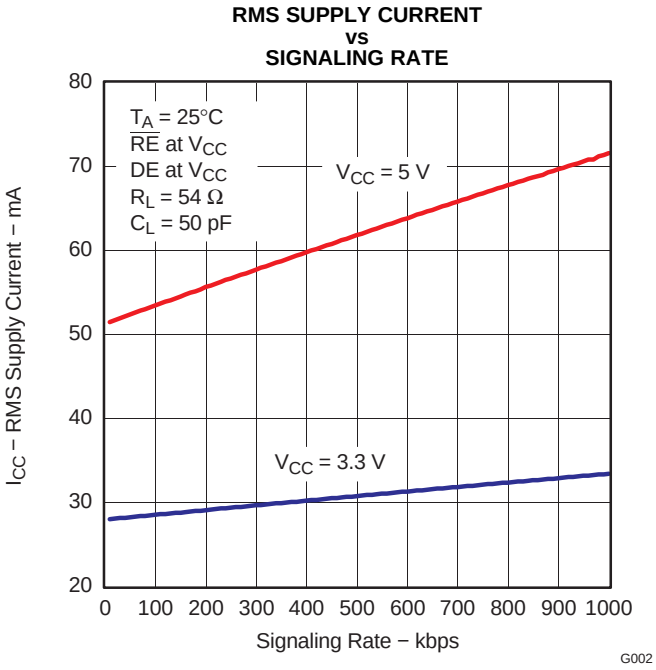


Figure 10.

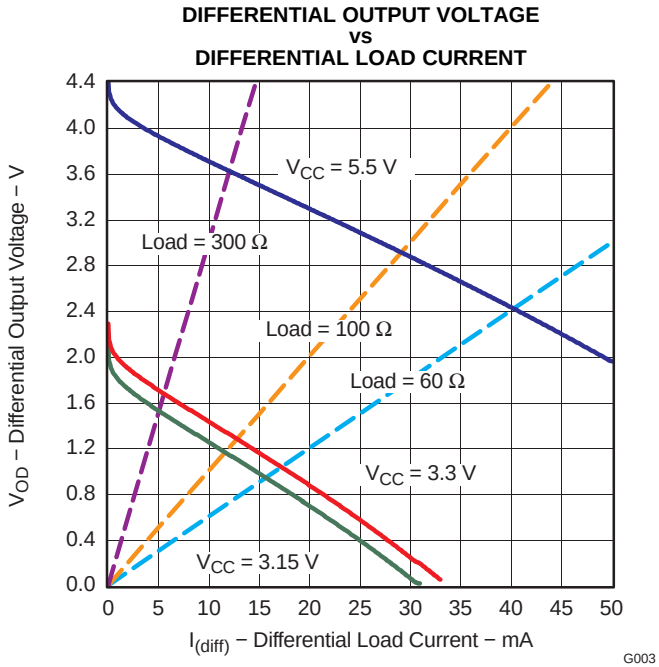


Figure 11.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
SN65HVD1781D	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN65HVD1781DG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN65HVD1781DR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN65HVD1781DRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

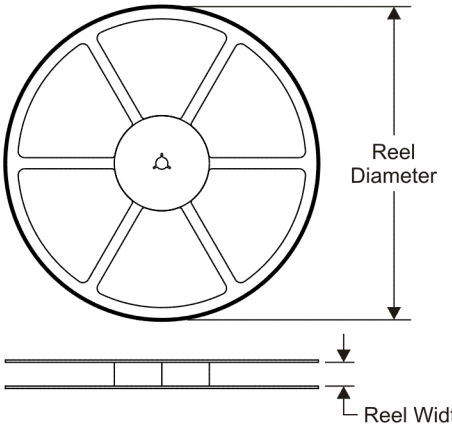
(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

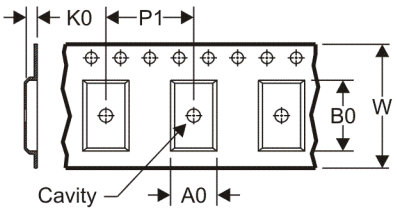
(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

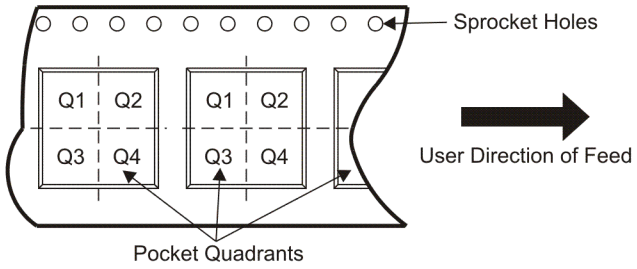


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

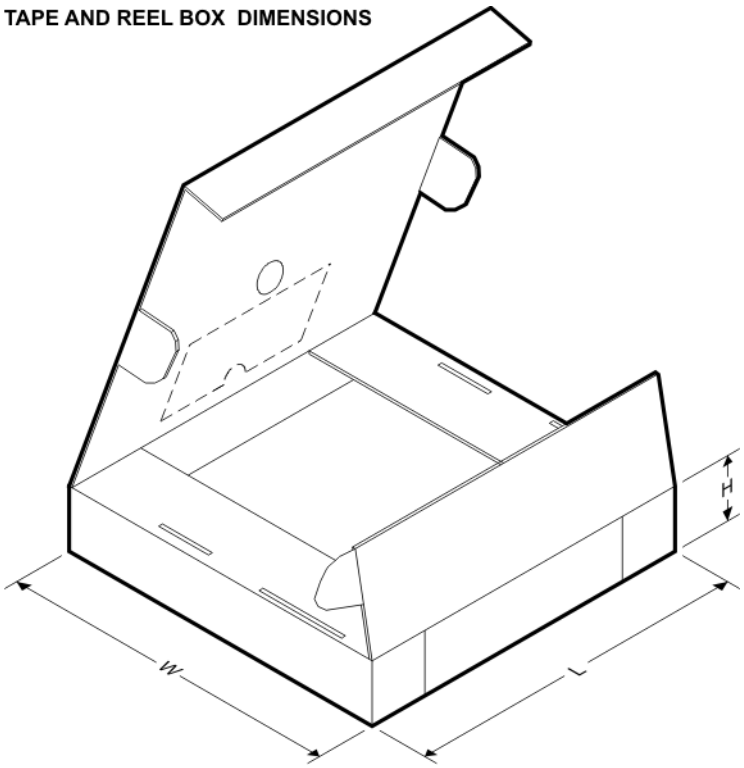
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN65HVD1781DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

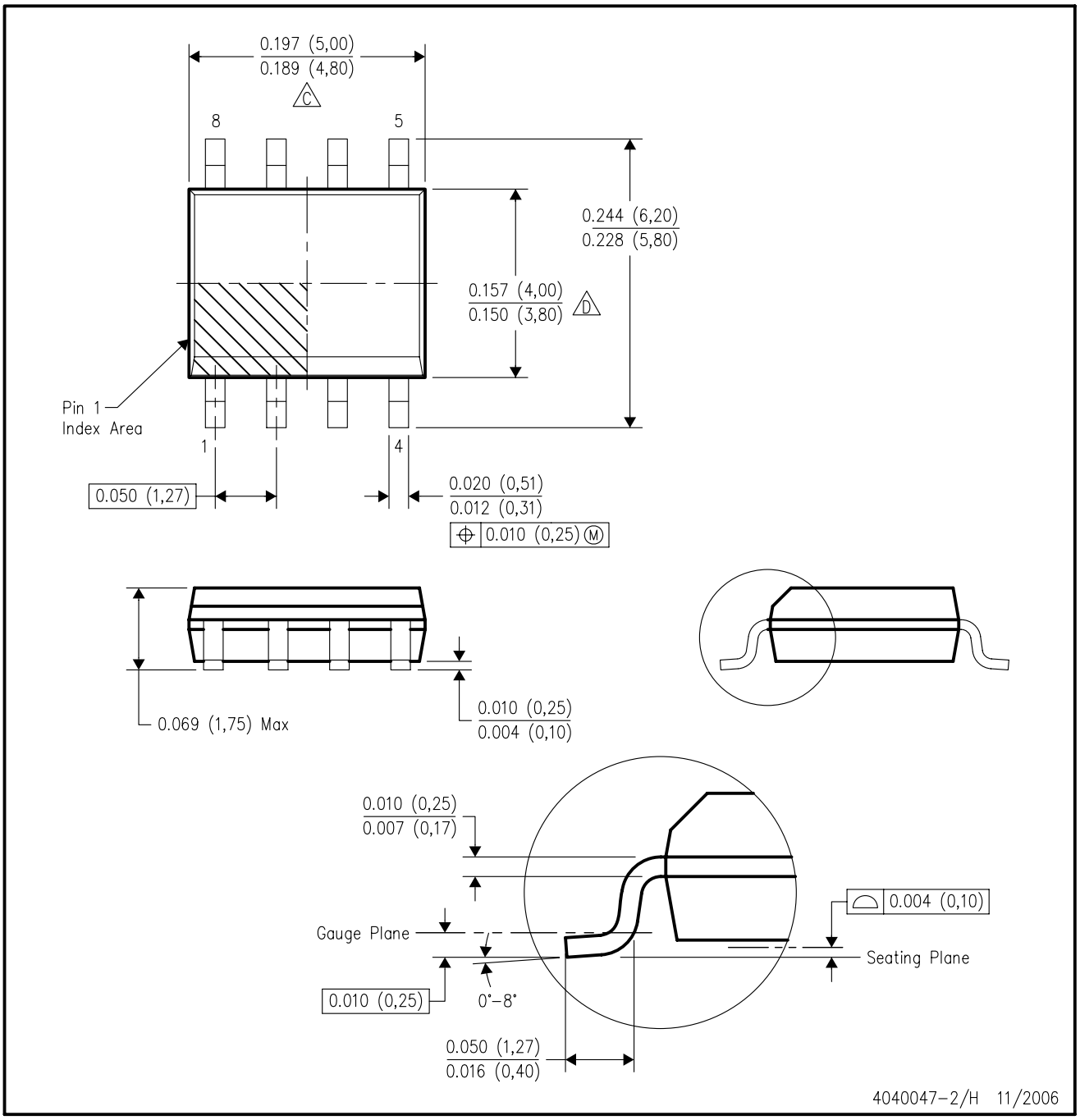
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN65HVD1781DR	SOIC	D	8	2500	346.0	346.0	29.0

D (R–PDSO–G8) PLASTIC SMALL–OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 (0,15) per end.
D. Body width does not include interlead flash. Interlead flash shall not exceed .017 (0,43) per side.
E. Reference JEDEC MS–012 variation AA.

IMPORTANT NOTICE

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