70-V Fault-Protected RS-485 Transceivers

FEATURES

- **Bus-Pin Fault Protection to > ±70 V**
- **Common-Mode Voltage Range (–20 V to 25 V) More Than Doubles TIA/EIA 485 Requirement**
- **Bus I/O Protection**
  - **±16 kV JEDEC HBM Protection**
- **Reduced Unit Load for Up to 256 Nodes**
- **Failsafe Receiver for Open-Circuit, Short-Circuit and Idle-Bus Conditions**
- **Low Power Consumption**
  - **Low Standby Supply Current, 1 μA Typ**
  - **I_{CC} 5 mA Quiescent During Operation**

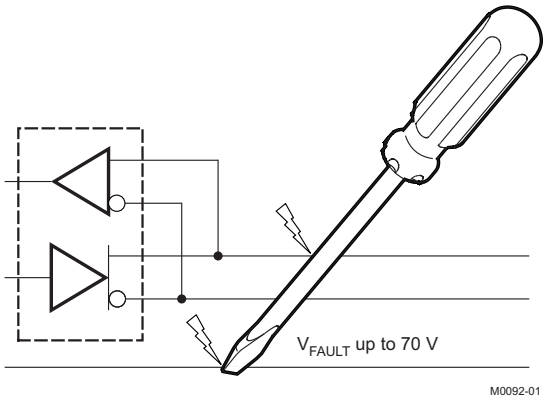
APPLICATIONS

- **Designed for RS-485 and RS-422 Networks**

DESCRIPTION

These devices are designed to survive overvoltage faults such as direct shorts to power supplies, mis-wiring faults, connector failures, cable crushes, and tool mis-applications. They are also robust to ESD events, with high levels of protection to human-body model specifications.

These devices combine a differential driver and a differential receiver, which operate from a single power supply. In the 'HVD1785, 'HVD1786, and 'HVD1787, the driver differential outputs and the receiver differential inputs are connected internally to form a bus port suitable for half-duplex (two-wire bus) communication. In the 'HVD1791, the driver differential outputs and the receiver differential inputs are separate pins, to form a bus port suitable for full-duplex (four-wire bus) communication. These ports feature a wide common-mode voltage range, making the devices suitable for multipoint applications over long cable runs. These devices are characterized from –40°C to 105°C.



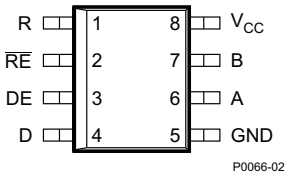
PRODUCT SELECTION GUIDE

PART NUMBER	DUPLEX	SIGNALING RATE	NODES	CABLE LENGTH
SN65HVD1785	Half	115 kbps	Up to 256	1500 m
SN65HVD1786	Half	1 Mbps	Up to 256	150 m
SN65HVD1787	Half	10 Mbps	Up to 64	50 m
SN65HVD1791	Full	115 kbps	Up to 256	1500 m
SN65HVD1792 (Preview)	Full	1 Mbps	Up to 256	150 m
SN65HVD1793 (Preview)	Full	10 Mbps	Up to 64	50 m

For similar features with 3.3 V supply operation, see the SN65HVD1781 (SLLS877).

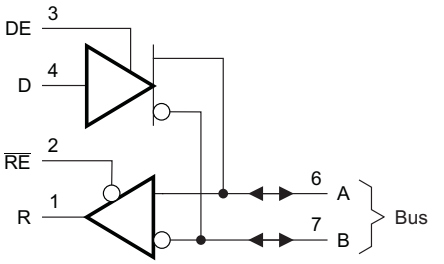
These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

SN65HVD1785, 1786, 1787
D or P Package
(Top View)



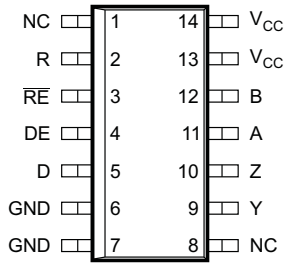
P0066-02

Logic Diagram (Positive Logic)



S0299-01

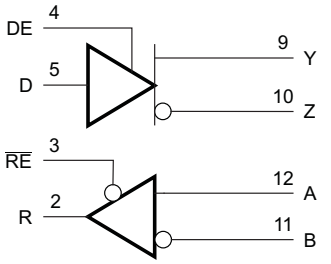
SN65HVD1791, 1792, 1793
D Package
(Top View)



NC - No internal connection

P0005-02

Logic Diagram (Positive Logic)



S0300-01

DEVICE INFORMATION

DRIVER FUNCTION TABLE

Input	Enable	Outputs		
D	**DE**	**A**	**B**	
H	H	H	L	Actively drive bus High
L	H	L	H	Actively drive bus Low
X	L	Z	Z	Driver disabled
X	OPEN	Z	Z	Driver disabled by default
OPEN	H	H	L	Actively drive bus High by default

RECEIVER FUNCTION TABLE

Differential Input	Enable	Output	
$V_{ID} = V_A - V_B$	**RE**	**R**	
$V_{IT+} < V_{ID}$	L	H	Receive valid bus High
$V_{IT-} < V_{ID} < V_{IT+}$	L	?	Indeterminate bus state
$V_{ID} < V_{IT-}$	L	L	Receive valid bus Low
X	H	Z	Receiver disabled
X	X	OPEN	Receiver disabled by default
Open-circuit bus	L	H	Fail-safe high output
Short-circuit bus	L	H	Fail-safe high output
Idle (terminated) bus	L	H	Fail-safe high output

ABSOLUTE MAXIMUM RATINGS(1)

		VALUE	UNIT
V_{CC}	Supply voltage	–0.5 to 7	V
	Voltage range at A and B inputs	–70 to 70	V
	Input voltage range at any logic pin	–0.3 to V_{CC} + 0.3	V
	Voltage input range, transient pulse, A and B, through 100 Ω	–100 to 100	V
	Receiver output current	–24 to 24	mA
T_J	Junction temperature	170	°C
	Continuous total power dissipation	See Dissipation Rating Table	
	IEC 60749-26 ESD (human-body model), bus terminals and GND	±16	kV
	JEDEC Standard 22, Test Method A114 (human-body model), bus terminals and GND	±16	kV
	JEDEC Standard 22, Test Method A114 (human-body model), all pins	±4	kV
	JEDEC Standard 22, Test Method C101 (charged-device model), all pins	±2	kV
	JEDEC Standard 22, Test Method A115 (machine model), all pins	±400	V

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

PACKAGE DISSIPATION RATINGS

PACKAGE	JEDEC THERMAL MODEL	T_A < 25°C RATING	DERATING FACTOR ABOVE T_A = 25°C	T_A = 85°C RATING	T_A = 105°C RATING
SOIC (D) 8-pin	High-K	905 mW	7.25 mW/°C	470 mW	325 mW
	Low-K	516 mW	4.1 mW/°C	268 mW	186 mW
SOIC (D) 14-pin	High-K	1315 mW	10.5 mW/°C	684 mW	474 mW
	Low-K	744 mW	6 mW/°C	387 mW	268 mW
PDIP (P) 8-pin	High-K	2119 mW	16.9 mW/°C	1100 mW	763 mW
	Low-K	976 mW	7.8 mW/°C	508 mW	352 mW

RECOMMENDED OPERATING CONDITIONS

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		4.5	5	5.5	V
V_I	Input voltage at any bus terminal (separately or common mode)(1)		–20		25	V
V_{IH}	High-level input voltage (driver, driver enable, and receiver enable inputs)		2		V_{CC}	V
V_{IL}	Low-level input voltage (driver, driver enable, and receiver enable inputs)		0		0.8	V
V_{ID}	Differential input voltage		–25		25	V
I_O	Output current, driver		–60		60	mA
	Output current, receiver		–8		8	mA
R_L	Differential load resistance		54	60		Ω
C_L	Differential load capacitance			50		pF
$1/t_{UI}$	Signaling rate	HVD1785, HVD1791			115	kbps
		HVD1786, HVD1792			1	Mbps
		HVD1787, HVD1793			10	
T_A	Operating free-air temperature (See application section for thermal information)		–40		105	°C
T_J	Junction temperature		–40		150	°C

(1) By convention, the least positive (most negative) limit is designated as minimum in this data sheet.

ELECTRICAL CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
$\|V_{OD}\|$	Driver differential output voltage magnitude	RS-485 with common-mode load, V_{CC} > 4.75 V, see Figure 1	$T_A \le 85°C$		1.5			V
			$T_A \le 105°C$		1.4			
		R_L = 54 Ω, 4.75 V ≤ V_{CC} ≤ 5.25 V			1.5	2		
		R_L = 100 Ω, 4.75 V ≤ V_{CC} ≤ 5.25 V			2	2.5		
$\Delta\|V_{OD}\|$	Change in magnitude of driver differential output voltage	R_L = 54 Ω			–0.2	0	0.2	V
$V_{OC(SS)}$	Steady-state common-mode output voltage				1	V_{CC}/2	3	V
ΔV_{OC}	Change in differential driver output common-mode voltage				–100	0	100	mV
$V_{OC(PP)}$	Peak-to-peak driver common-mode output voltage	Center of two 27-Ω load resistors, See Figure 2				500		mV
C_{OD}	Differential output capacitance					23		pF
V_{IT+}	Positive-going receiver differential input voltage threshold	V_{CM} = –20 V to 25 V				–100	–10	mV
V_{IT-}	Negative-going receiver differential input voltage threshold				–200	–150		mV
V_{HYS}	Receiver differential input voltage threshold hysteresis ($V_{IT+} - V_{IT-}$)				30	50		mV
V_{OH}	Receiver high-level output voltage	I_{OH} = –8 mA			2.4	V_{CC} – 0.3		V
V_{OL}	Receiver low-level output voltage	I_{OL} = 8 mA	$T_A \le 85°C$			0.2	0.4	V
			$T_A \le 105°C$			0.2	0.5	
I_I	Driver input, driver enable, and receiver enable input current				–100		100	µA
I_{OZ}	Receiver output high-impedance current	V_O = 0 V or V_{CC}, $\overline{RE}$ at V_{CC}			–1		1	µA
I_{OS}	Driver short-circuit output current				–250		250	mA
I_I	Bus input current (disabled driver)	V_{CC} = 4.5 to 5.5 V or V_{CC} = 0 V, DE at 0 V	85, 86, 91, 92	V_I = 12 V		75	125	µA
				V_I = –7 V	–100	–40		
			87, 93	V_I = 12 V			500	
				V_I = –7 V	–400			
I_{CC}	Supply current (quiescent)	Driver and receiver enabled	DE = V_{CC}, RE = GND, no load			4	6	mA
		Driver enabled, receiver disabled	DE = V_{CC}, RE = V_{CC}, no load			3	5	
		Driver disabled, receiver enabled	DE = GND, RE = GND, no load			2	4	
		Driver and receiver disabled	DE = GND, D = open RE = V_{CC}, no load			0.5	5	µA
	Supply current (dynamic)	See TYPICAL CHARACTERISTICS section						

SWITCHING CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
DRIVER (HVD1785 AND HVD1791)							
t_r, t_f	Driver differential output rise/fall time	R_L = 54 Ω, C_L = 50 pF, See Figure 3		0.4	1.7	2.6	µs
t_{PHL}, t_{PLH}	Driver propagation delay				0.8	2	µs
$t_{SK(P)}$	Driver differential output pulse skew, $\|t_{PHL} - t_{PLH}\|$				20	250	ns
t_{PHZ}, t_{PLZ}	Driver disable time		See Figure 4 and Figure 5		0.1	5	µs
t_{PZH}, t_{PZL}	Driver enable time	Receiver enabled			0.2	3	µs
		Receiver disabled			3	12	
DRIVER (HVD1786 AND HVD1792)							
t_r, t_f	Driver differential output rise/fall time	R_L = 54 Ω, C_L = 50 pF, See Figure 3		50		300	ns
t_{PHL}, t_{PLH}	Driver propagation delay					200	ns
$t_{SK(P)}$	Driver differential output pulse skew, $\|t_{PHL} - t_{PLH}\|$					25	ns
t_{PHZ}, t_{PLZ}	Driver disable time		See Figure 4 and Figure 5			3	µs
t_{PZH}, t_{PZL}	Driver enable time	Receiver enabled				300	ns
		Receiver disabled				10	µs
DRIVER (HVD1787 AND HVD1793)							
t_r, t_f	Driver differential output rise/fall time	R_L = 54 Ω, C_L = 50 pF, See Figure 3		3		30	ns
t_{PHL}, t_{PLH}	Driver propagation delay					50	ns
$t_{SK(P)}$	Driver differential output pulse skew, $\|t_{PHL} - t_{PLH}\|$					10	ns
t_{PHZ}, t_{PLZ}	Driver disable time		See Figure 4 and Figure 5			3	µs
t_{PZH}, t_{PZL}	Driver enable time	Receiver enabled				300	ns
		Receiver disabled				9	µs
RECEIVER (ALL DEVICES UNLESS OTHERWISE NOTED)							
t_r, t_f	Receiver output rise/fall time	C_L = 15 pF, See Figure 6			4	15	ns
t_{PHL}, t_{PLH}	Receiver propagation delay time		85, 86, 91, 92		100	200	ns
			87, 93			70	
$t_{SK(P)}$	Receiver output pulse skew, $\|t_{PHL} - t_{PLH}\|$		85, 86, 91, 92		6	20	ns
			87, 93			5	
t_{PLZ}, t_{PHZ}	Receiver disable time	Driver enabled, See Figure 7			15	100	ns
$t_{PZL(1)}$, $t_{PZH(1)}$ $t_{PZL(2)}$), $t_{PZH(2)}$	Receiver enable time	Driver enabled, See Figure 7			80	300	ns
		Driver disabled, See Figure 8			3	9	µs

THERMAL INFORMATION

PARAMETER			TEST CONDITIONS	VALUE	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance (no airflow)	SOIC-8	JEDEC high-K model	138	°C/W
			JEDIC low-K model	242	
		DIP-8	JEDEC high-K model	59	
			JEDIC low-K model	128	
		SOIC-14	JEDEC high-K model	95	
			JEDIC low-K model	168	
$R_{\theta JB}$	Junction-to-board thermal resistance	SOIC-8		62	°C/W
		DIP-8		39	
		SOIC-14		40	
$R_{\theta JC}$	Junction-to-case thermal resistamce	SOIC-8		61	°C/W
		DIP-8		61	
		SOIC-14		44	
P_D	Power dissipation	85, 91	V_{CC} = 5.5 V, T_J = 150°C, R_L = 300 Ω, C_L = 50 pF (driver), C_L = 15 pF (receiver) 5-V supply, unterminated(1)	290	mW
		85, 91	V_{CC} = 5.5 V, T_J = 150°C, R_L = 100 Ω, C_L = 50 pF (driver), C_L = 15 pF (receiver) 5-V supply, RS-422 load(1)		
		86		320	
		87			
		85, 91	V_{CC} = 5.5 V, T_J = 150°C, R_L = 54 Ω, C_L = 50 pF (driver), C_L = 15 pF (receiver) 5-V supply, RS-485 load(1)	400	
		86			
		87			
T_{SD}	Thermal-shutdown junction temperature			170	°C

(1) Driver and receiver enabled, 50% duty cycle square-wave signal at signaling rate: HVD1785, 1791 at 115 kbps, HVD1786 at 1 Mbps, HVD1787 at 10 Mbps)

PARAMETER MEASUREMENT INFORMATION

Input generator rate is 100 kbps, 50% duty cycle, rise and fall times less than 6 nsec, output impedance 50 Ω.

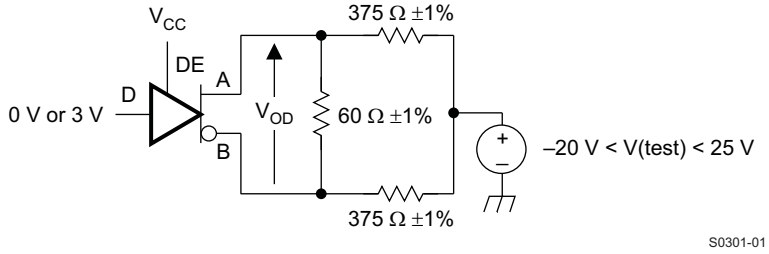


Figure 1. Measurement of Driver Differential Output Voltage With Common-Mode Load

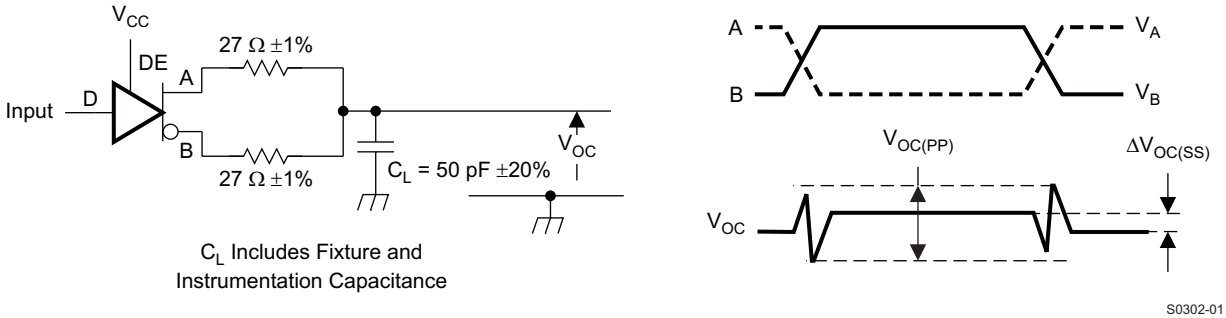


Figure 2. Measurement of Driver Differential and Common-Mode Output With RS-485 Load

PARAMETER MEASUREMENT INFORMATION (continued)

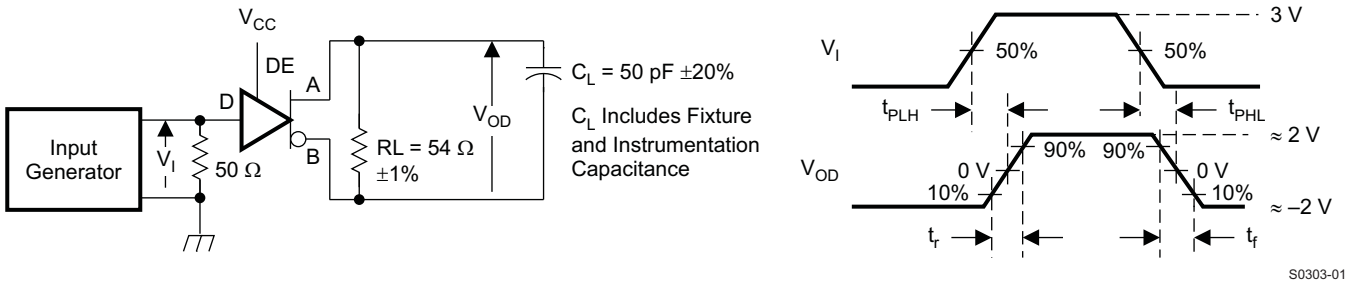
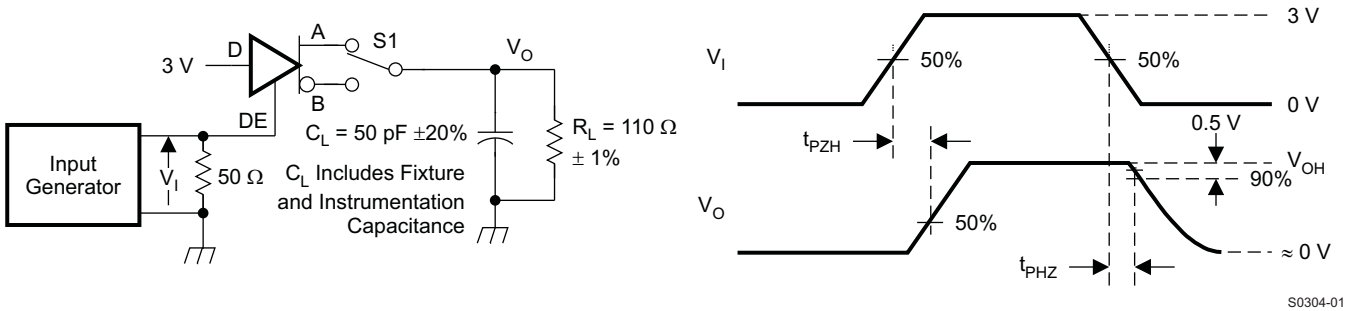
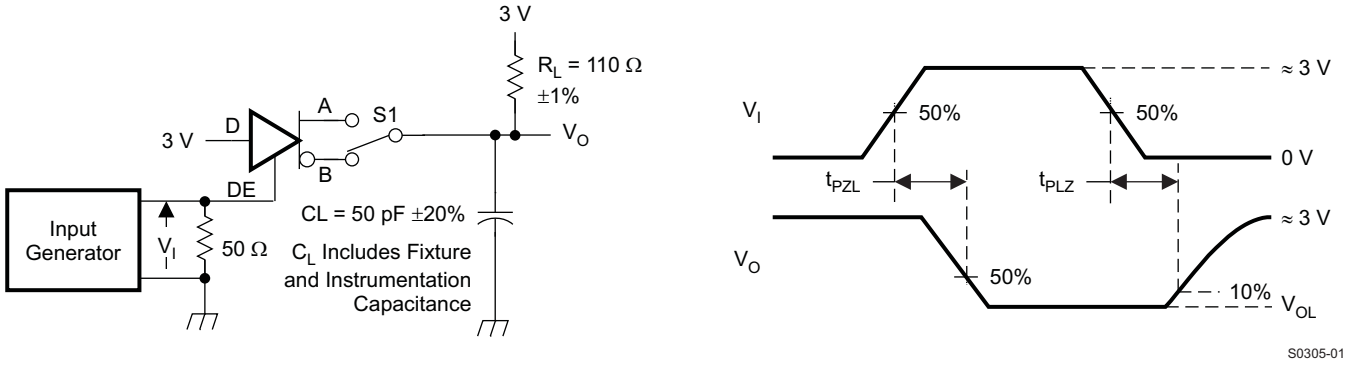


Figure 3. Measurement of Driver Differential Output Rise and Fall Times and Propagation Delays



NOTE: D at 3 V to test non-inverting output, D at 0 V to test inverting output.

Figure 4. Measurement of Driver Enable and Disable Times With Active High Output and Pulldown Load



NOTE: D at 0 V to test non-inverting output, D at 3 V to test inverting output.

Figure 5. Measurement of Driver Enable and Disable Times With Active-Low Output and Pullup Load

PARAMETER MEASUREMENT INFORMATION (continued)

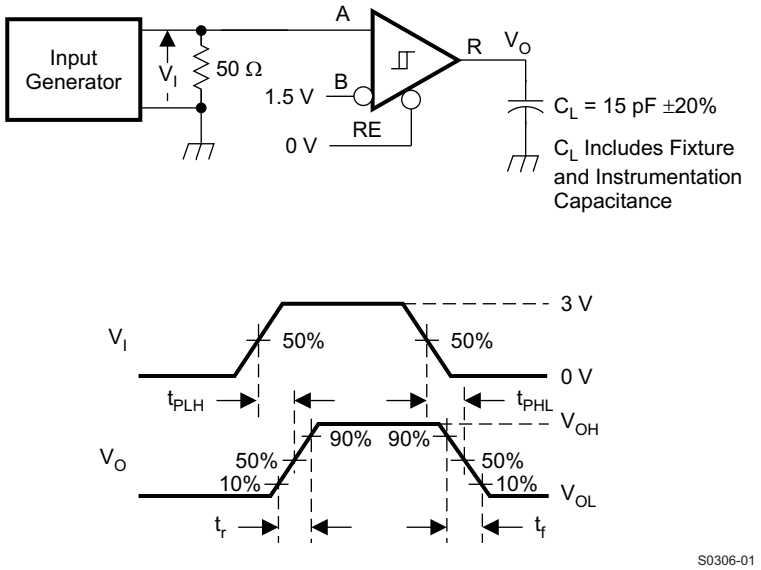


Figure 6. Measurement of Receiver Output Rise and Fall Times and Propagation Delays

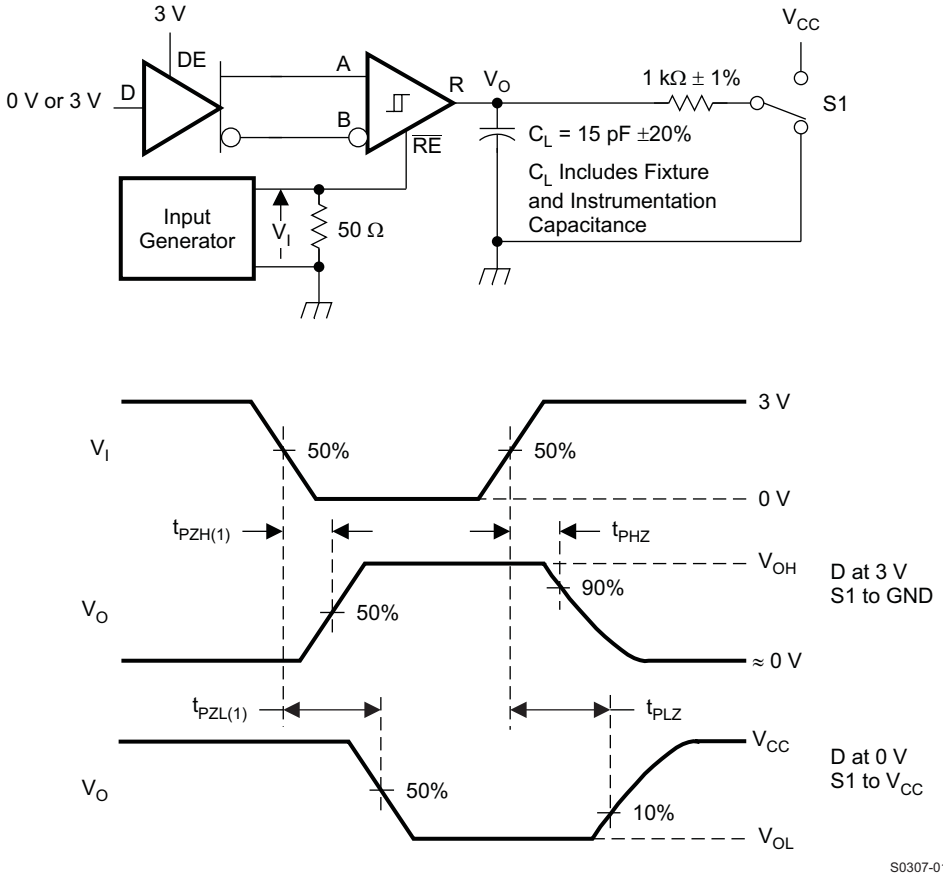


Figure 7. Measurement of Receiver Enable/Disable Times With Driver Enabled

PARAMETER MEASUREMENT INFORMATION (continued)

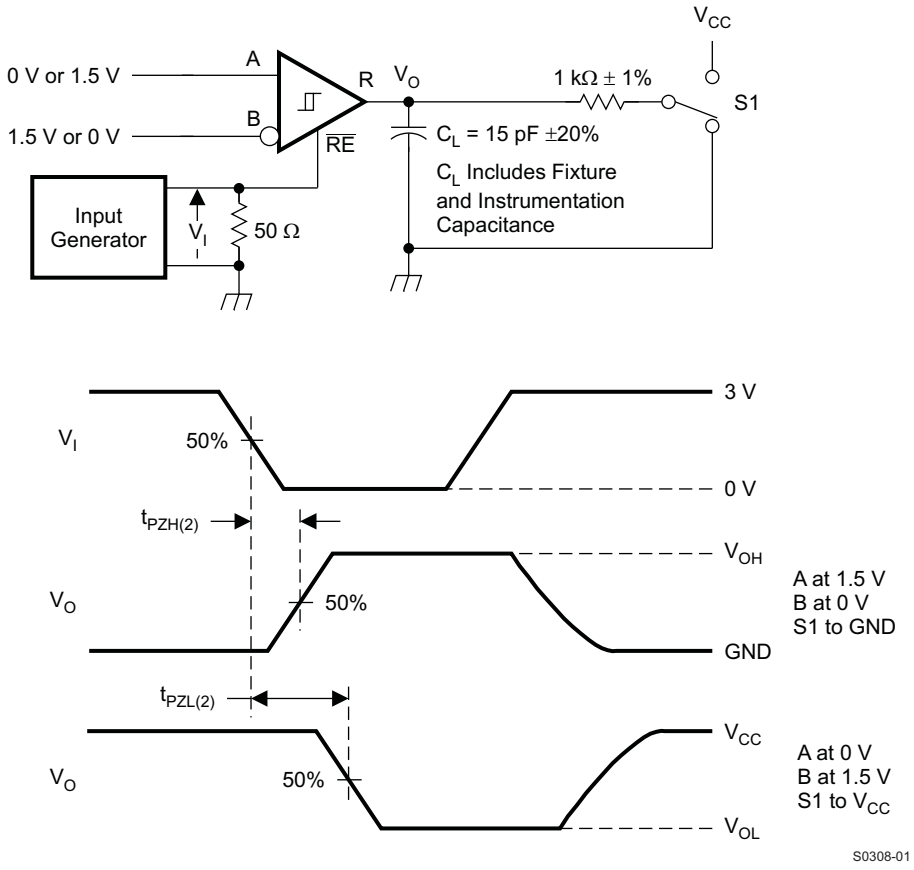


Figure 8. Measurement of Receiver Enable Times With Driver Disabled

TYPICAL CHARACTERISTICS

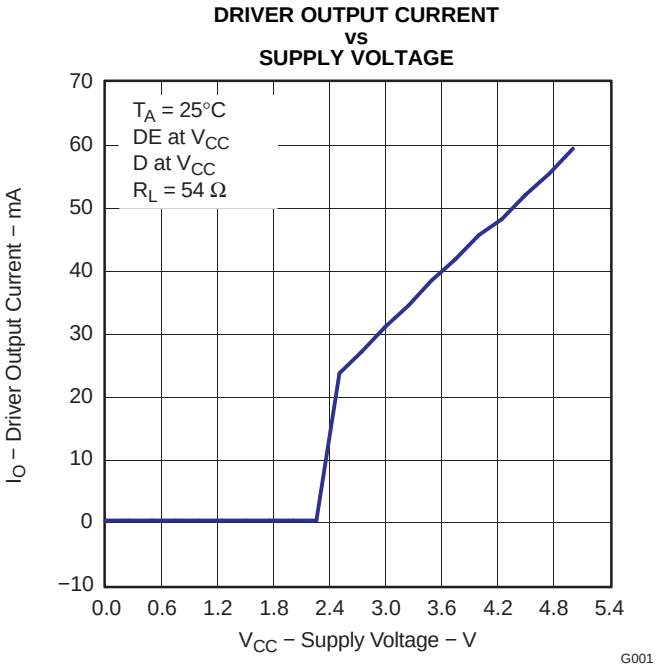


Figure 9.

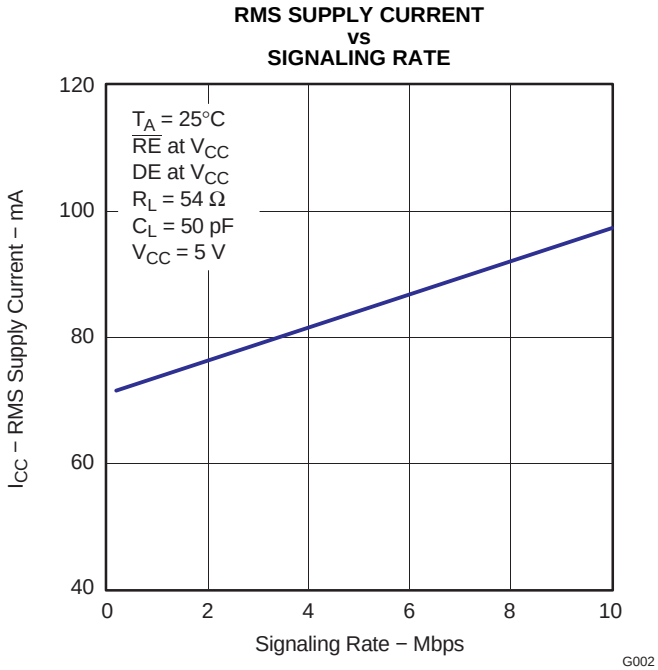


Figure 10.

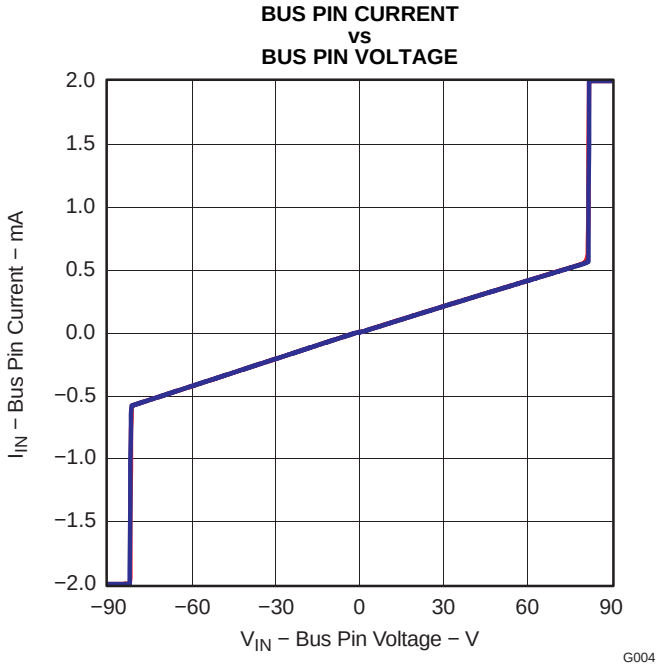


Figure 11.

ADDITIONAL OPTIONS

The SN65HVD17xx family also has options for J1708 applications, for always-enabled full-duplex versions (industry-standard SN65LBC179 footprint) and for inverting-polarity versions, which allow users to correct a reversal of the bus wires without re-wiring. Contact your local Texas Instruments representative for information on these options.

PART NUMBER	SN65HVD17xx		
FOOTPRINT/FUNCTION	SLOW	MEDIUM	FAST
Half-duplex (176 pinout)	85	86	87
Full-duplex no enables (179 pinout)	88	89	90
Full-duplex with enables (180 pinout)	91	92	93
Half-duplex with cable invert	94	95	96
Full-duplex with cable invert and enables	97	98	99
J1708	08	09	10

Figure 12. SN65HVD1708E Transceiver for J1708 Applications

Figure 13. SN65HVD17xx Always-Enabled Driver Receiver

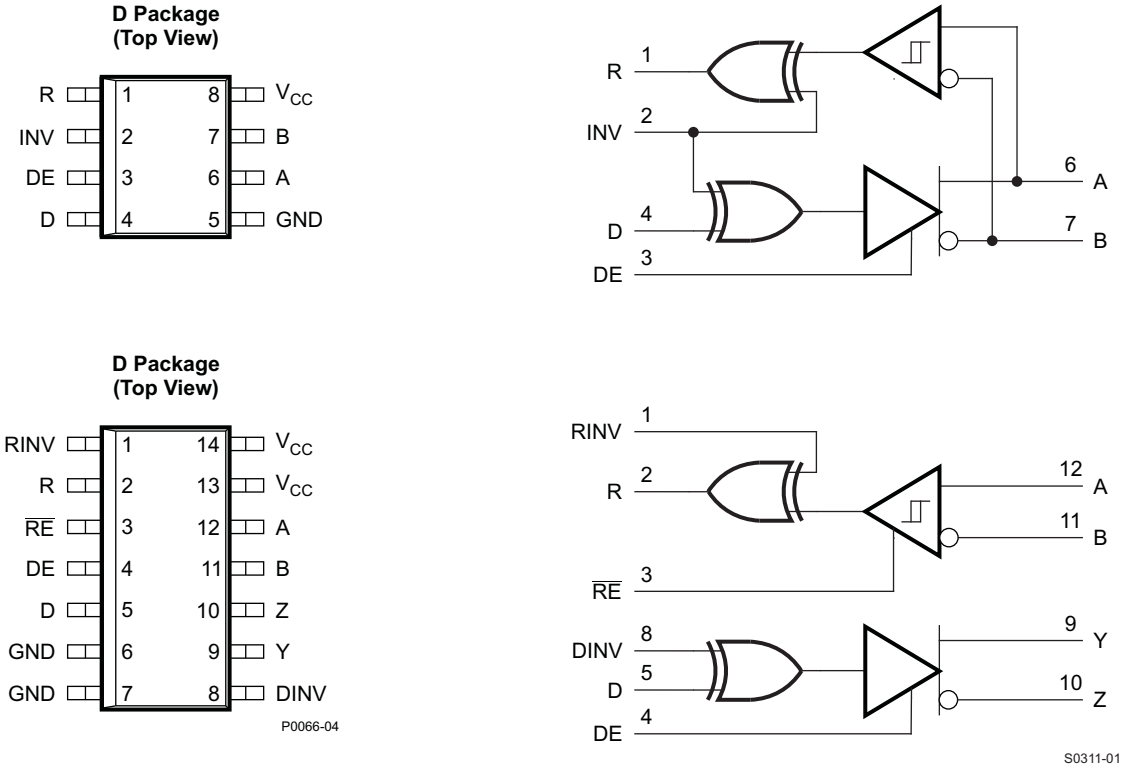


Figure 14. SN65HVD17xx Options With Inverting Feature to Correct for Miswired Cables

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
SN65HVD1785D	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN65HVD1785DR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN65HVD1785P	PREVIEW	PDIP	P	8	50	TBD	Call TI	Call TI
SN65HVD1786D	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN65HVD1786DR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN65HVD1786P	PREVIEW	PDIP	P	8		TBD	Call TI	Call TI
SN65HVD1787D	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN65HVD1787DR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN65HVD1787P	PREVIEW	PDIP	P	8		TBD	Call TI	Call TI
SN65HVD1791D	PREVIEW	SOIC	D	14	50	TBD	Call TI	Call TI
SN65HVD1791DR	PREVIEW	SOIC	D	14	2500	TBD	Call TI	Call TI

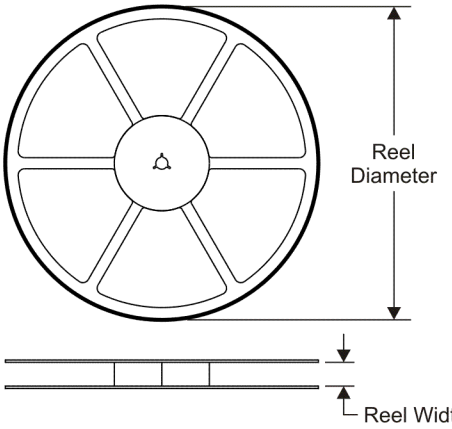
(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

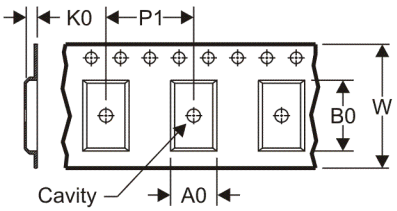
(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

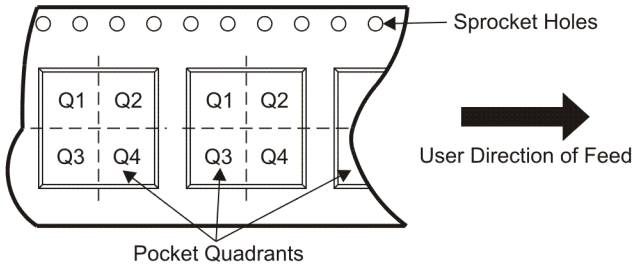


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

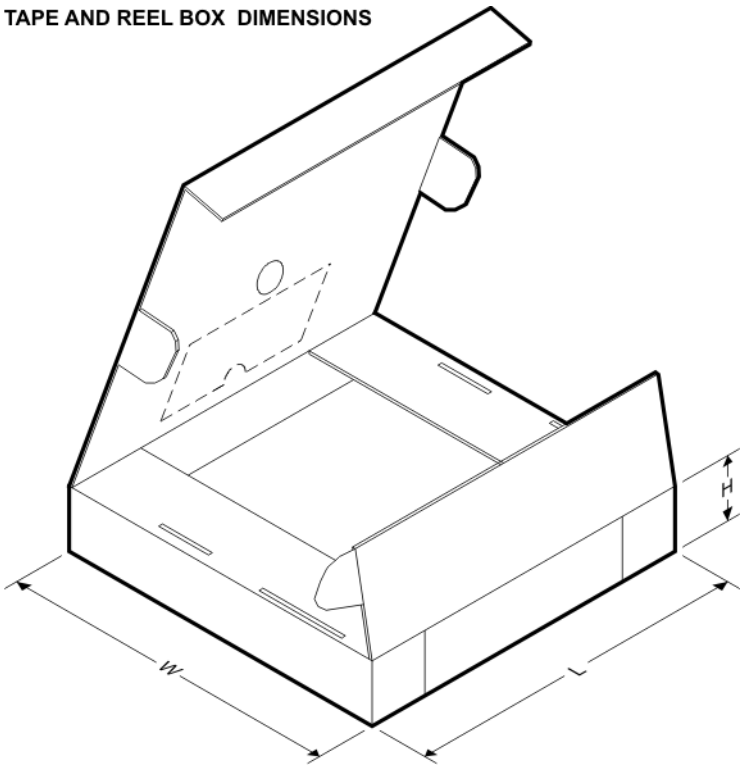
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN65HVD1785DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
SN65HVD1786DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
SN65HVD1787DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

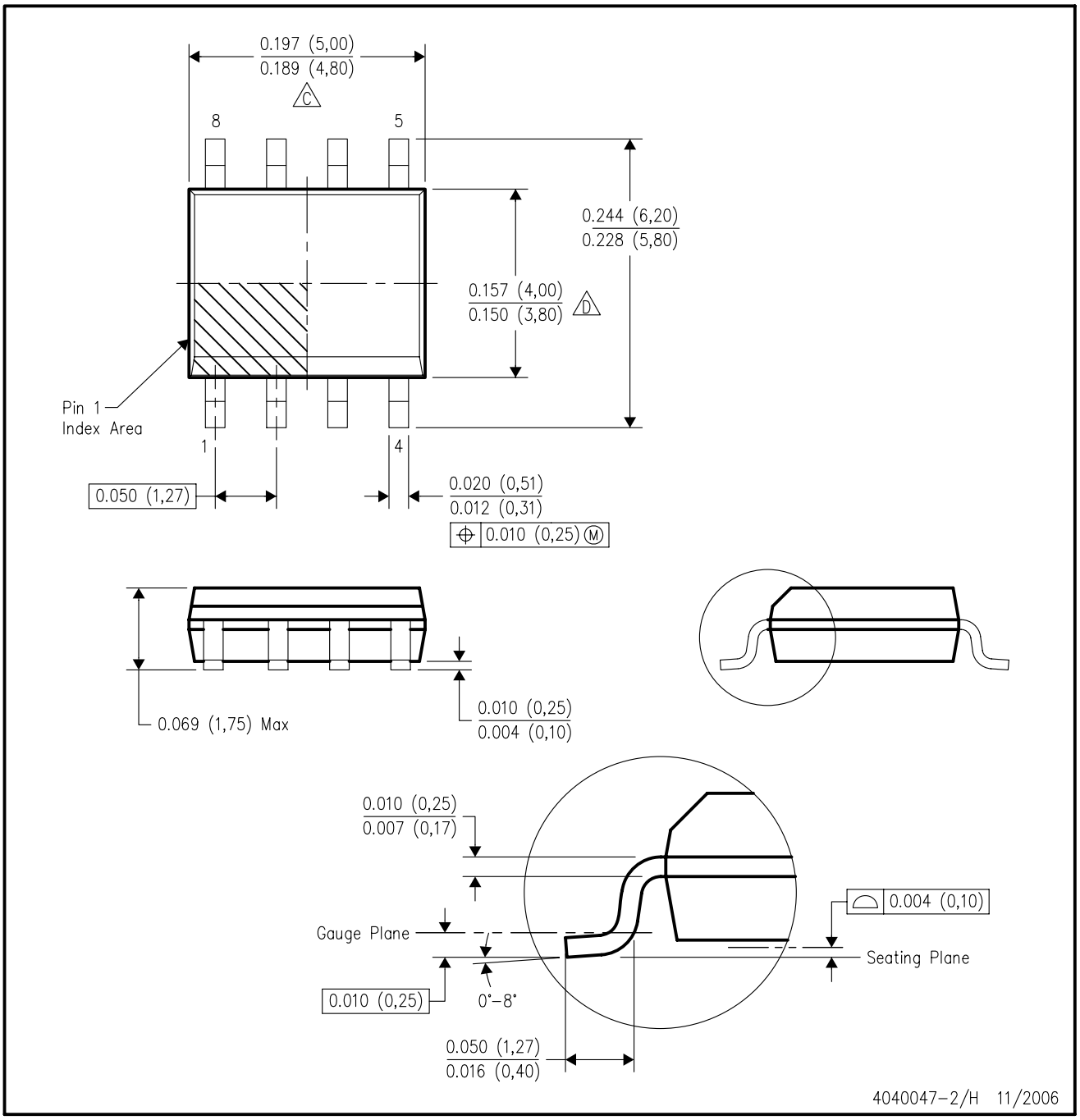
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

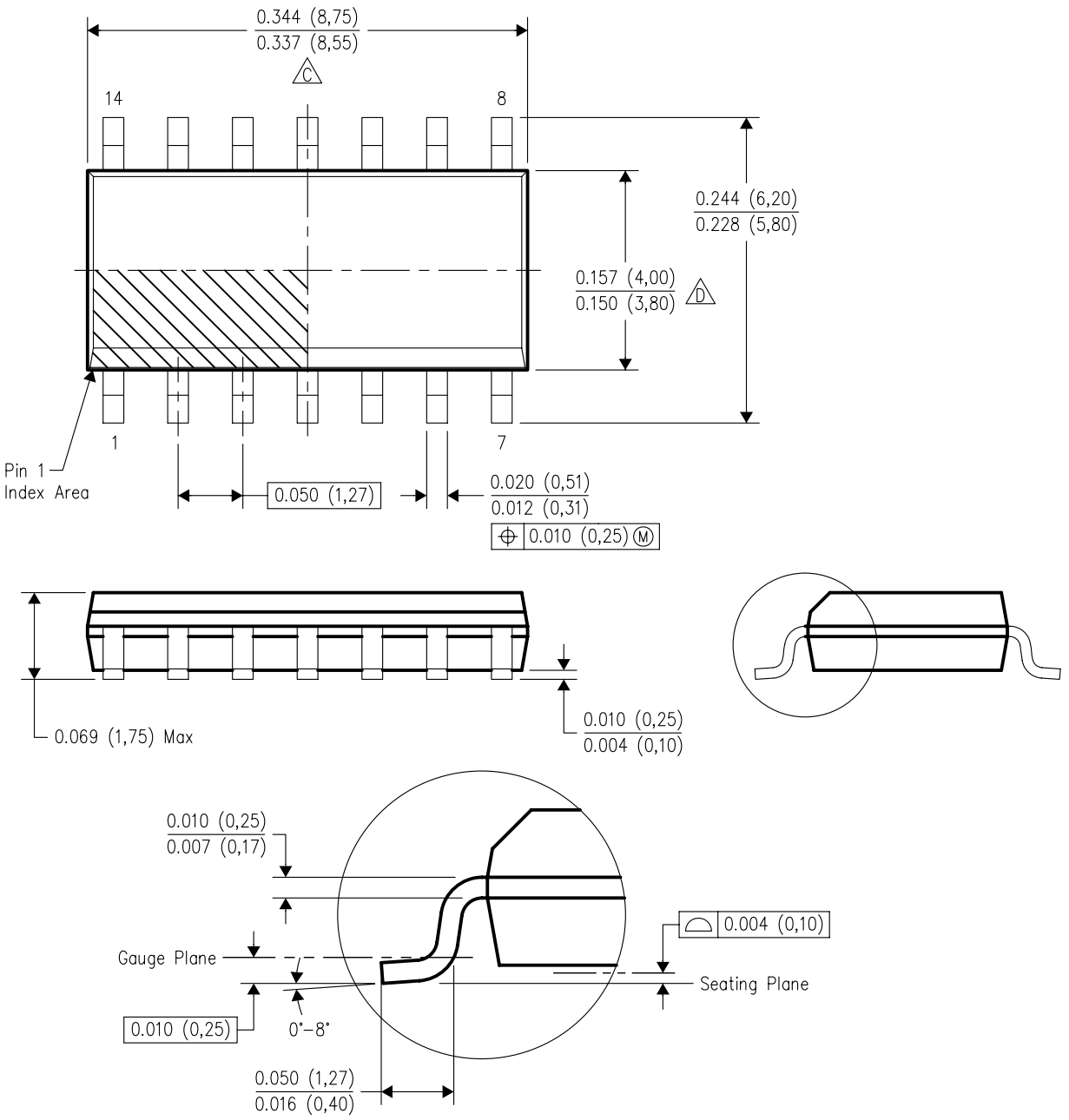
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN65HVD1785DR	SOIC	D	8	2500	346.0	346.0	29.0
SN65HVD1786DR	SOIC	D	8	2500	346.0	346.0	29.0
SN65HVD1787DR	SOIC	D	8	2500	346.0	346.0	29.0

D (R–PDSO–G8) PLASTIC SMALL–OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 (0,15) per end.
D. Body width does not include interlead flash. Interlead flash shall not exceed .017 (0,43) per side.
E. Reference JEDEC MS–012 variation AA.

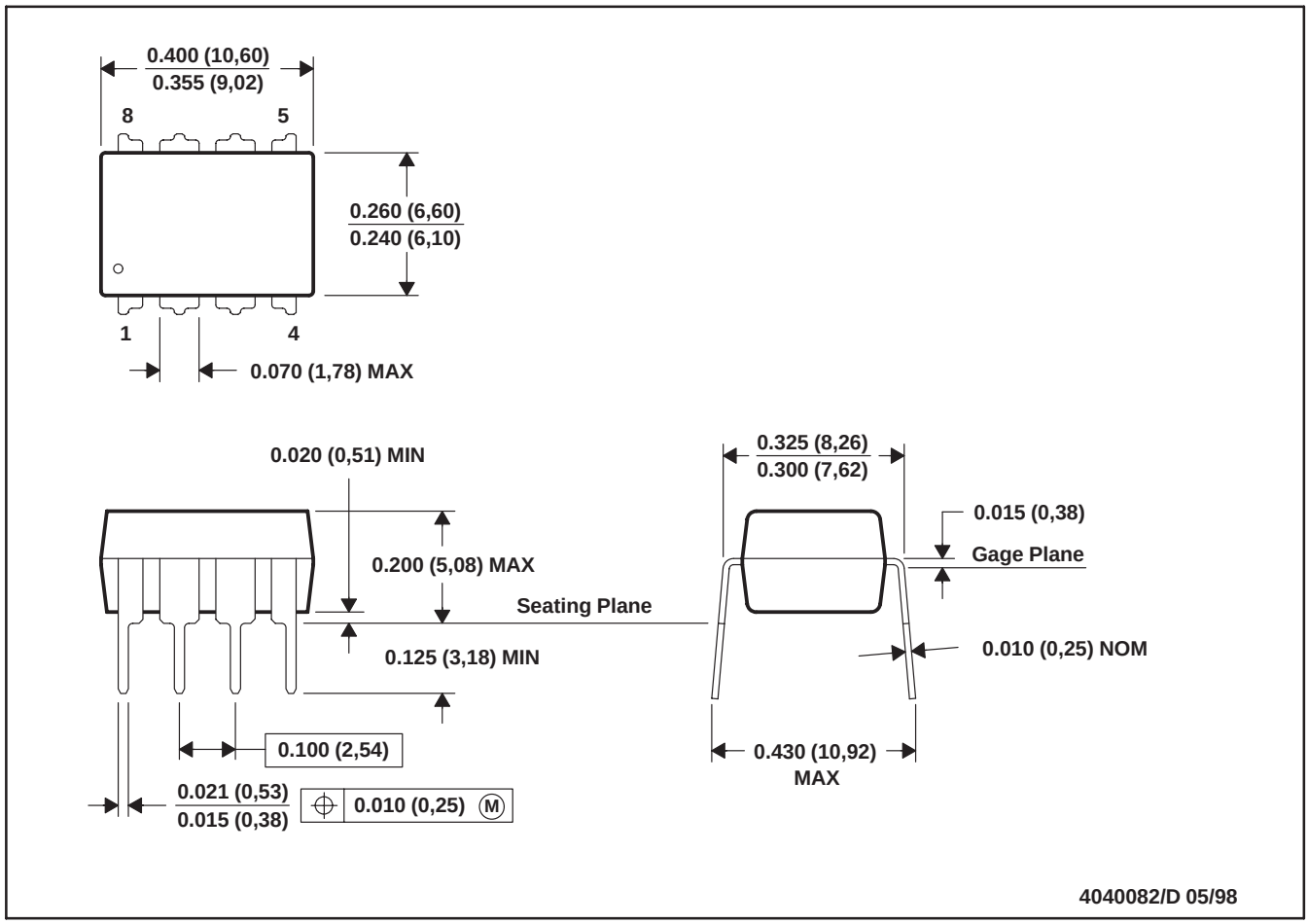
D (R–PDSO–G14) PLASTIC SMALL–OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 (0,15) per end.
D. Body width does not include interlead flash. Interlead flash shall not exceed .017 (0,43) per side.
E. Reference JEDEC MS–012 variation AB.

MPDI001A – JANUARY 1995 – REVISED JUNE 1999

P (R-PDIP-T8) **PLASTIC DUAL-IN-LINE**



NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-001

For the latest package information, go to http://www.ti.com/sc/docs/package/pkg_info.htm

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third-party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

TI products are not authorized for use in safety-critical applications (such as life support) where a failure of the TI product would reasonably be expected to cause severe personal injury or death, unless officers of the parties have executed an agreement specifically governing such use. Buyers represent that they have all necessary expertise in the safety and regulatory ramifications of their applications, and acknowledge and agree that they are solely responsible for all legal, regulatory and safety-related requirements concerning their products and any use of TI products in such safety-critical applications, notwithstanding any applications-related information or support that may be provided by TI. Further, Buyers must fully indemnify TI and its representatives against any damages arising out of the use of TI products in such safety-critical applications.

TI products are neither designed nor intended for use in military/aerospace applications or environments unless the TI products are specifically designated by TI as military-grade or "enhanced plastic." Only products designated by TI as military-grade meet military specifications. Buyers acknowledge and agree that any such use of TI products which TI has not designated as military-grade is solely at the Buyer's risk, and that they are solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI products are neither designed nor intended for use in automotive applications or environments unless the specific TI products are designated by TI as compliant with ISO/TS 16949 requirements. Buyers acknowledge and agree that, if they use any non-designated products in automotive applications, TI will not be responsible for any failure to meet such requirements.

Following are URLs where you can obtain information on other Texas Instruments products and application solutions:

Products		**Applications**	
Amplifiers	amplifier.ti.com	Audio	www.ti.com/audio
Data Converters	dataconverter.ti.com	Automotive	www.ti.com/automotive
DSP	dsp.ti.com	Broadband	www.ti.com/broadband
Clocks and Timers	www.ti.com/clocks	Digital Control	www.ti.com/digitalcontrol
Interface	interface.ti.com	Medical	www.ti.com/medical
Logic	logic.ti.com	Military	www.ti.com/military
Power Mgmt	power.ti.com	Optical Networking	www.ti.com/opticalnetwork
Microcontrollers	microcontroller.ti.com	Security	www.ti.com/security
RFID	www.ti-rfid.com	Telephony	www.ti.com/telephony
RF/IF and ZigBee® Solutions	www.ti.com/lprf	Video & Imaging	www.ti.com/video
		Wireless	www.ti.com/wireless

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265