



SCCS032 - September 1994 - Revised March 2000

**CY74FCT652T**

## 8-Bit Registered Transceiver

### Features

- Function, pinout, and drive compatible with FCT and F logic
- FCT-C speed at 5.4 ns max. (Com'l)  
FCT-A speed at 6.3 ns max. (Com'l)
- Reduced  $V_{OH}$  (typically = 3.3V) versions of equivalent FCT functions
- Edge-rate control circuitry for significantly improved noise characteristics
- Power-off disable feature
- Matched rise and fall times
- Fully compatible with TTL input and output logic levels
- Sink Current 64 mA  
Source Current 32 mA
- Independent register for A and B buses
- Multiplexed real-time and stored data transfer
- Extended commercial range of  $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$

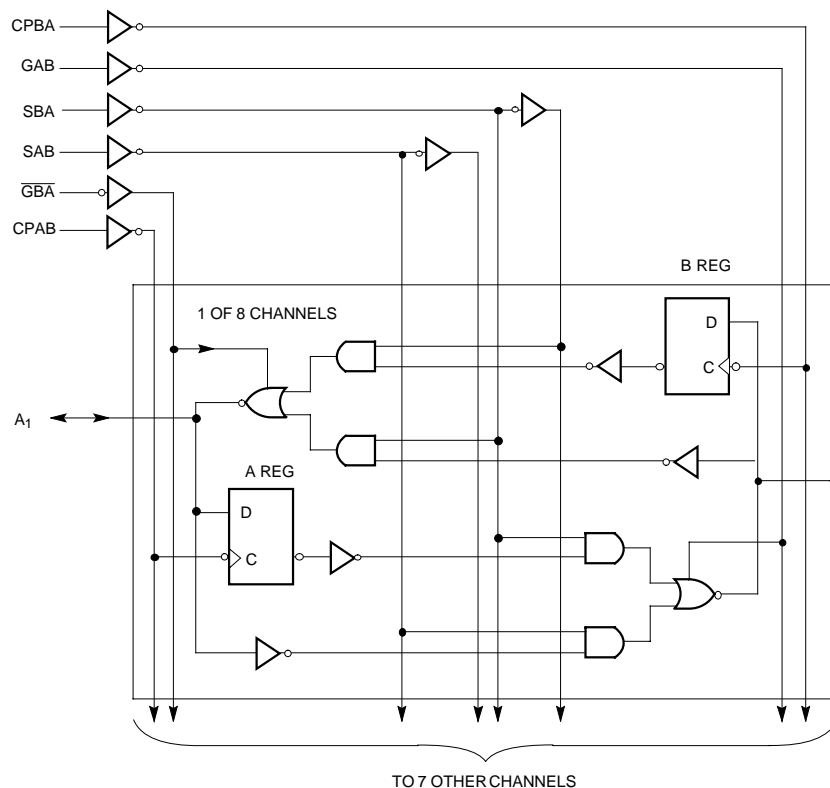
### Functional Description

The FCT652T consists of bus transceiver circuits, D-type flip-flops, and control circuitry arranged for multiplexed transmission of data directly from the input bus or from the internal storage registers. GAB and GBA control pins are provided to control the transceiver functions. SAB and SBA control pins are provided to select either real-time or stored data transfer. The circuitry used for select control will eliminate the typical decoding glitch that occurs in a multiplexer during the transition between stored and real-time data. A LOW input level selects real-time data and a HIGH selects stored data.

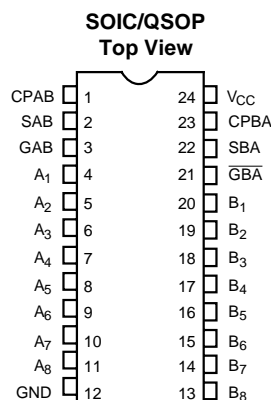
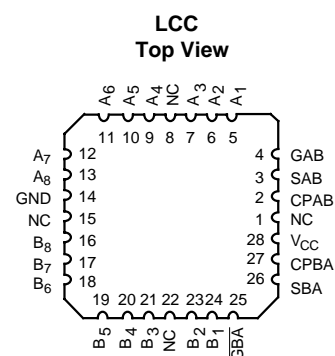
Data on the A or B data bus, or both, can be stored in the internal D flip-flops by LOW-to-HIGH transitions at the appropriate clock pins (CPAB or CPBA), regardless of the select or enable control pins. When SAB and SBA are in the real-time transfer mode, it is also possible to store data without using the internal D-type flip-flops by simultaneously enabling GAB and GBA. In this configuration, each output reinforces its input. Thus, when all other data sources to the two sets of bus lines are at high impedance, each set of bus lines will remain at its last state.

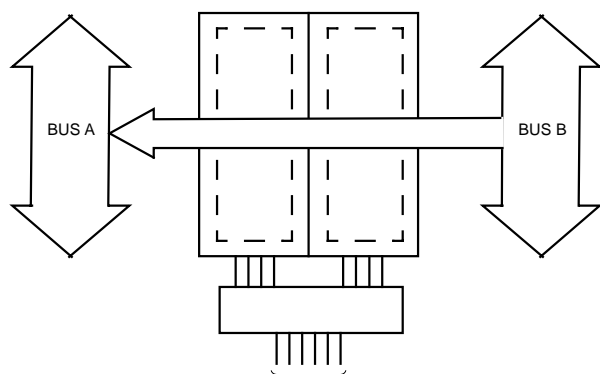
The outputs are designed with a power-off disable feature to allow for live insertion of boards.

### Logic Block Diagram



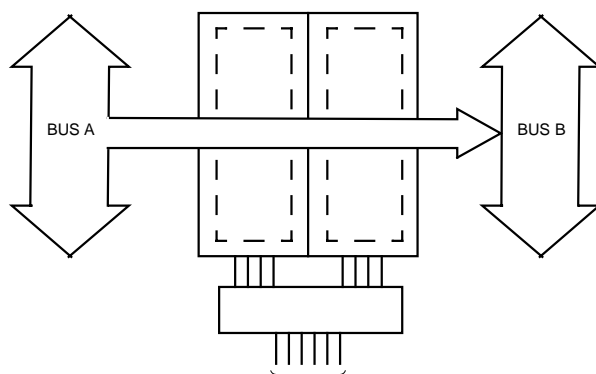
### Pin Configurations





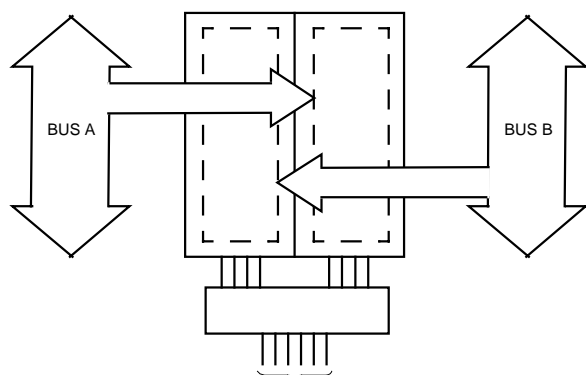
GAB L     $\overline{\text{GBA}}$  L    CPAB X    CPBA X    SAB X    SBA L

**Real-Time Transfer  
Bus B to Bus A**



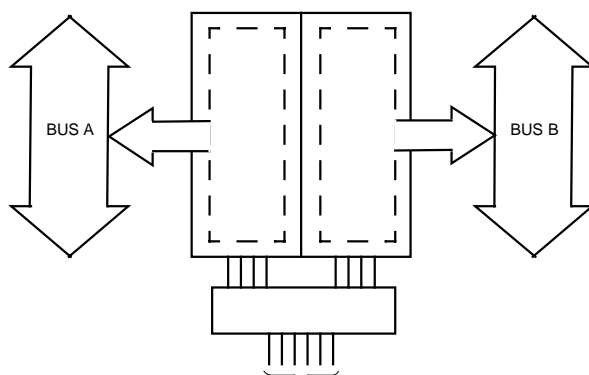
GAB H     $\overline{\text{GBA}}$  H    CPAB X    CPBA X    SAB L    SBA X

**Real-Time Transfer  
Bus A to Bus B**



GAB X L L     $\overline{\text{GBA}}$  H X H    CPAB  $\downarrow$  X  $\downarrow$     CPBA X  $\downarrow$   $\downarrow$     SAB X X X    SBA X X X

**Store Data from A and/or B**



GAB H     $\overline{\text{GBA}}$  L    CPAB H or L    CPBA H or L    SAB H    SBA H

**Transferred Stored Data  
to A and/or B**

### Function Table<sup>[1]</sup>

Inputs						Data I/O		Operation or Function
GAB	$\overline{\text{GBA}}$	CPAB	CPBA	SAB	SBA	A <sub>1</sub> thru A <sub>8</sub>	B <sub>1</sub> thru B <sub>8</sub>	
L	H	H or L	H or L	X	X	Input	Input	Isolation
L	H	$\downarrow$	$\downarrow$	X	X			Store A and B Data
X	H	$\downarrow$	H or L	X	X	Input	Unspecified <sup>[2]</sup>	Store A, Hold B
H	H	$\downarrow$	$\downarrow$	X <sup>[1]</sup>	X	Input	Output	Store A in both registers
L	X	H or L	$\downarrow$	X	X	Unspecified <sup>[2]</sup>	Input	Hold A, Store B
L	L	$\downarrow$	$\downarrow$	X	X <sup>[1]</sup>	Output	Input	Store B in both registers
L	L	X	X	X	L	Output	Input	Real-Time B Data to A Bus
L	L	X	H or L	X	H			Stored B Data to A Bus
H	H	X	X	L	X	Input	Output	Real-Time A Data to B Bus
H	H	H or L	X	H	X			Stored A Data to B Bus
H	L	H or L	H or L	H	H	Output	Output	Stored A Data to B Bus and Stored B Data to A Bus

#### Notes:

- Select control=L: clocks can occur simultaneously. Select control=H: clocks must be staggered in order to load both registers. H = HIGH Voltage Level. L = LOW Voltage Level. X = Don't Care.  $\downarrow$  = LOW-to-HIGH Transition.
- The data output functions may be enabled or disabled by various signals at the GAB or GBA inputs. Data input functions are always enabled, i.e., data at the bus pins will be stored on every LOW-to-HIGH transition on the clock inputs.

**Maximum Ratings**<sup>[3, 4]</sup>

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... –65°C to +150°C

Ambient Temperature with  
Power Applied ..... –65°C to +135°C

Supply Voltage to Ground Potential ..... –0.5V to +7.0V

DC Input Voltage ..... –0.5V to +7.0V

DC Output Voltage ..... –0.5V to +7.0V

DC Output Current (Maximum Sink Current/Pin) ..... 120 mA

Power Dissipation ..... 0.5W

Static Discharge Voltage ..... >2001V  
(per MIL-STD-883, Method 3015)

**Operating Range**

Range	Range	Ambient Temperature	V <sub>CC</sub>
Commercial	T, AT, CT	–40°C to +85°C	5V ± 5%

**Electrical Characteristics** Over the Operating Range

Parameter	Description	Test Conditions	Min.	Typ. <sup>[5]</sup>	Max.	Unit
V <sub>OH</sub>	Output HIGH Voltage	V <sub>CC</sub> =Min., I <sub>OH</sub> =–32 mA	2.0			V
		V <sub>CC</sub> =Min., I <sub>OH</sub> =–15 mA	2.4	3.3		V
V <sub>OL</sub>	Output LOW Voltage	V <sub>CC</sub> =Min., I <sub>OL</sub> =64 mA		0.3	0.55	V
V <sub>IH</sub>	Input HIGH Voltage		2.0			V
V <sub>IL</sub>	Input LOW Voltage				0.8	V
V <sub>H</sub>	Hysteresis <sup>[6]</sup>	All inputs		0.2		V
V <sub>IK</sub>	Input Clamp Diode Voltage	V <sub>CC</sub> =Min., I <sub>IN</sub> =–18 mA		–0.7	–1.2	V
I <sub>I</sub>	Input HIGH Current	V <sub>CC</sub> =Max., V <sub>IN</sub> =V <sub>CC</sub>			5	μA
I <sub>IH</sub>	Input HIGH Current <sup>[6]</sup>	V <sub>CC</sub> =Max., V <sub>IN</sub> =2.7V			±1	μA
I <sub>IL</sub>	Input LOW Current <sup>[6]</sup>	V <sub>CC</sub> =Max., V <sub>IN</sub> =0.5V			±1	μA
I <sub>OZH</sub>	Off State HIGH-Level Output Current	V <sub>CC</sub> =Max., V <sub>OUT</sub> =2.7V			10	μA
I <sub>OZL</sub>	Off State LOW-Level Output Current	V <sub>CC</sub> =Max., V <sub>OUT</sub> =0.5V			–10	μA
I <sub>OS</sub>	Output Short Circuit Current <sup>[7]</sup>	V <sub>CC</sub> =Max., V <sub>OUT</sub> =0.0V	–60	–120	–225	mA
I <sub>OFF</sub>	Power-Off Disable	V <sub>CC</sub> =0V, V <sub>OUT</sub> =4.5V			±1	μA

**Capacitance**<sup>[6]</sup>

Parameter	Description	Typ. <sup>[5]</sup>	Max.	Unit
C <sub>IN</sub>	Input Capacitance	5	10	pF
C <sub>OUT</sub>	Output Capacitance	9	12	pF

**Notes:**

- Unless otherwise noted, these limits are over the operating free-air temperature range.
- Unused inputs must always be connected to an appropriate logic voltage level, preferably either V<sub>CC</sub> or ground.
- Typical values are at V<sub>CC</sub>=5.0V, T<sub>A</sub>=+25°C ambient.
- This parameter is specified but not tested.
- Not more than one output should be shorted at a time. Duration of short should not exceed one second. The use of high-speed test apparatus and/or sample and hold techniques are preferable in order to minimize internal chip heating and more accurately reflect operational values. Otherwise prolonged shorting of a high output may raise the chip temperature well above normal and thereby cause invalid readings in other parametric tests. In any sequence of parameter tests, I<sub>OS</sub> tests should be performed last.

**Power Supply Characteristics**

Parameter	Description	Test Conditions	Typ. <sup>[5]</sup>	Max.	Unit
$I_{CC}$	Quiescent Power Supply Current	$V_{CC}=\text{Max.}$ , $V_{IN}\leq 0.2V$ , $V_{IN}\geq V_{CC}-0.2V$	0.1	0.2	mA
$\Delta I_{CC}$	Quiescent Power Supply Current (TTL inputs HIGH)	$V_{CC}=\text{Max.}$ , $V_{IN}=3.4V$ , $f_1=0$ , Outputs Open <sup>[8]</sup>	0.5	2.0	mA
$I_{CCD}$	Dynamic Power Supply Current <sup>[9]</sup>	$V_{CC}=\text{Max.}$ , One Input Toggling, 50% Duty Cycle, Outputs Open, $GAB=\overline{GND}$ , $\overline{GBA}=\overline{GND}$ , $V_{IN}\leq 0.2V$ or $V_{IN}\geq V_{CC}-0.2V$	0.06	0.12	mA/MHz
$I_C$	Total Power Supply Current <sup>[10]</sup>	$V_{CC}=\text{Max.}$ , $f_0=10\text{ MHz}$ , 50% Duty Cycle, Outputs Open, One Bit Toggling at $f_1=5\text{ MHz}$ , $GAB=\overline{GND}$ , $\overline{GBA}=\overline{GND}$ , $SAB=CPAB=\overline{GND}$ , $SBA=V_{CC}$ , $V_{IN}\leq 0.2V$ or $V_{IN}\geq V_{CC}-0.2V$	0.7	1.4	mA
		$V_{CC}=\text{Max.}$ , $f_0=10\text{ MHz}$ , 50% Duty Cycle, Outputs Open, One Bit Toggling at $f_1=5\text{ MHz}$ , $GAB=\overline{GND}$ , $\overline{GBA}=\overline{GND}$ , $SAB=CPAB=\overline{GND}$ , $SBA=V_{CC}$ , $V_{IN}=3.4V$ or $V_{IN}=\overline{GND}$	1.2	3.4	mA
		$V_{CC}=\text{Max.}$ , $f_0=10\text{ MHz}$ , 50% Duty Cycle, Outputs Open, Eight Bits Toggling at $f_1=5\text{ MHz}$ , $GAB=\overline{GBA}=\overline{GND}$ , $SAB=CPAB=\overline{GND}$ , $SBA=V_{CC}$ , $V_{IN}\leq 0.2V$ or $V_{IN}\geq V_{CC}-0.2V$	2.8	5.6 <sup>[11]</sup>	mA
		$V_{CC}=\text{Max.}$ , $f_0=10\text{ MHz}$ , 50% Duty Cycle, Outputs Open, Eight Bits Toggling at $f_1=5\text{ MHz}$ , $GAB=\overline{GBA}=\overline{GND}$ , $SAB=CPAB=\overline{GND}$ , $SBA=V_{CC}$ , $V_{IN}=3.4V$ or $V_{IN}=\overline{GND}$	5.1	14.6 <sup>[11]</sup>	mA

**Notes:**

8. Per TTL driven input ( $V_{IN}=3.4V$ ); all other inputs at  $V_{CC}$  or  $\overline{GND}$ .
9. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
10.  $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$   
 $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD}(f_0/2 + f_1 N_1)$   
 $I_{CC}$  = Quiescent Current with CMOS input levels  
 $\Delta I_{CC}$  = Power Supply Current for a TTL HIGH input ( $V_{IN}=3.4V$ )  
 $D_H$  = Duty Cycle for TTL inputs HIGH  
 $N_T$  = Number of TTL inputs at  $D_H$   
 $I_{CCD}$  = Dynamic Current caused by an input transition pair (HLH or LHL)  
 $f_0$  = Clock frequency for registered devices, otherwise zero  
 $f_1$  = Input signal frequency  
 $N_1$  = Number of inputs changing at  $f_1$   
All currents are in milliamps and all frequencies are in megahertz.
11. Values for these conditions are examples of the  $I_{CC}$  formula. These limits are specified but not tested.

**Switching Characteristics** Over the Operating Range<sup>[12]</sup>

Parameter	Description	FCT652T		FCT652AT		FCT652CT		Unit	Fig. No. <sup>[13]</sup>
		Commercial		Commercial		Commercial			
		Min.	Max.	Min.	Max.	Min.	Max.		
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay Bus to Bus	1.5	9.0	1.5	6.3	1.5	5.4	ns	1, 3
t <sub>PZH</sub> t <sub>PZL</sub>	Output Enable Time Enable to Bus	1.5	14.0	1.5	9.8	1.5	7.8	ns	1, 7, 8
t <sub>PHZ</sub> t <sub>PLZ</sub>	Output Disable Time Enable to Bus	1.5	9.0	1.5	6.3	1.5	6.3	ns	1, 7, 8
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay Clock to Bus	1.5	9.0	1.5	6.3	1.5	5.7	ns	1, 5
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay SBA or SAB to A or B	1.5	11.0	1.5	7.7	1.5	6.2	ns	1, 5
t <sub>S</sub>	Set-Up Time HIGH or LOW Bus to Clock	4.0		2.0		2.0		ns	4
t <sub>H</sub>	Hold Time HIGH or LOW Bus to Clock	2.0		1.5		1.5		ns	4
t <sub>W</sub>	Clock Pulse Width, <sup>[14]</sup> HIGH or LOW	6.0		5.0		5.0		ns	5

**Ordering Information**

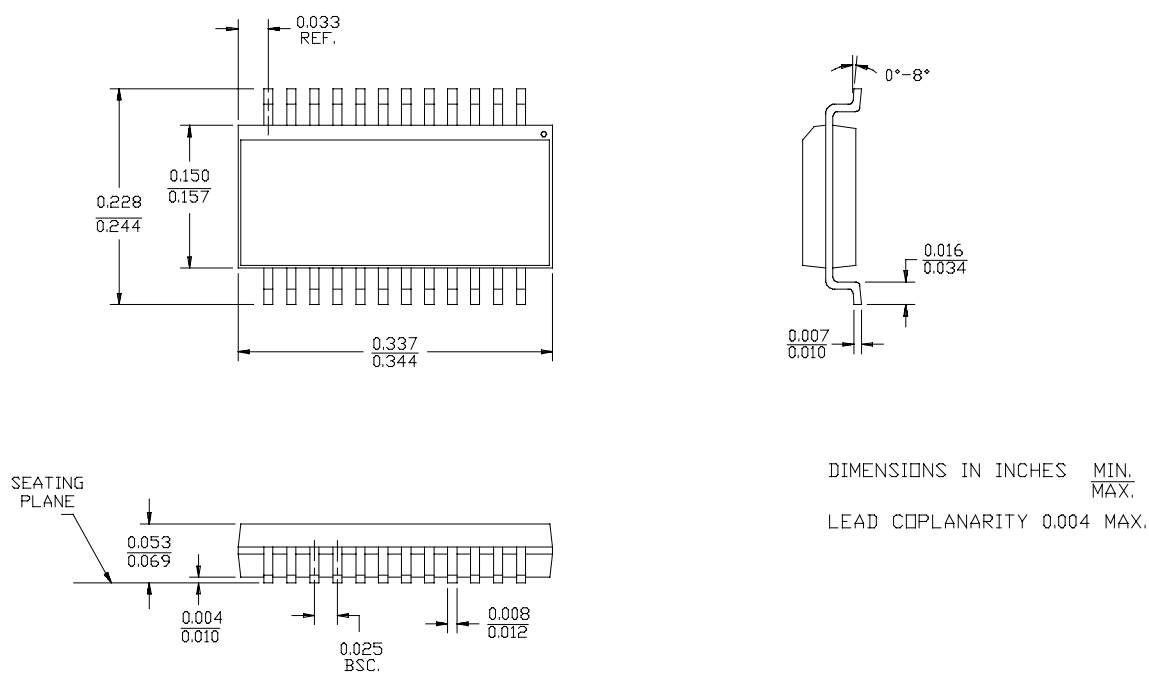
Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
5.4	CY74FCT652CTQCT	Q13	24-Lead (150-Mil) QSOP	Commercial
	CY74FCT652CTSOC/SOCT	S13	24-Lead (300-Mil) Molded SOIC	
6.3	CY74FCT652ATQCT	Q13	24-Lead (150-Mil) QSOP	Commercial
	CY74FCT652ATSOC/SOCT	S13	24-Lead (300-Mil) Molded SOIC	
9.0	CY74FCT652TQCT	Q13	24-Lead (150-Mil) QSOP	Commercial

**Notes:**

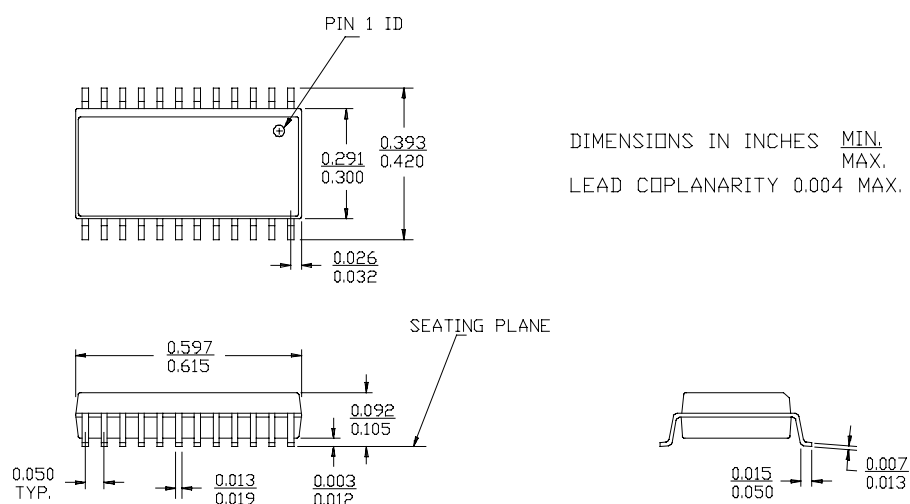
12. Minimum limits are specified but not tested on Propagation Delays.  
13. See "Parameter Measurement Information" in the General Information section.  
14. With one data channel toggling, t<sub>W(L)</sub>=t<sub>W(H)</sub>=4.0 ns and t<sub>r</sub>=t<sub>f</sub>=1.0 ns.

**Package Diagrams**

**24-Lead Quarter Size Outline Q13**



**24-Lead (300-Mil) Molded SOIC S13**



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