

512K (32K x 16) Static RAM

Features

- Pin-and function-compatible with CY7C1020CV33
- High speed
 - $t_{AA} = 10 \text{ ns}$
- Low active power
 - $I_{CC} = 60 \text{ mA @ } 10 \text{ ns}$
- Low CMOS standby power
 - $I_{SB2} = 3 \text{ mA}$
- 2.0V Data retention
- Automatic power-down when deselected
- CMOS for optimum speed/power
- Independent control of upper and lower bits
- Available in Pb-free 44-pin 400-Mil wide Molded SOJ and 44-pin TSOP II packages

Functional Description^[1]

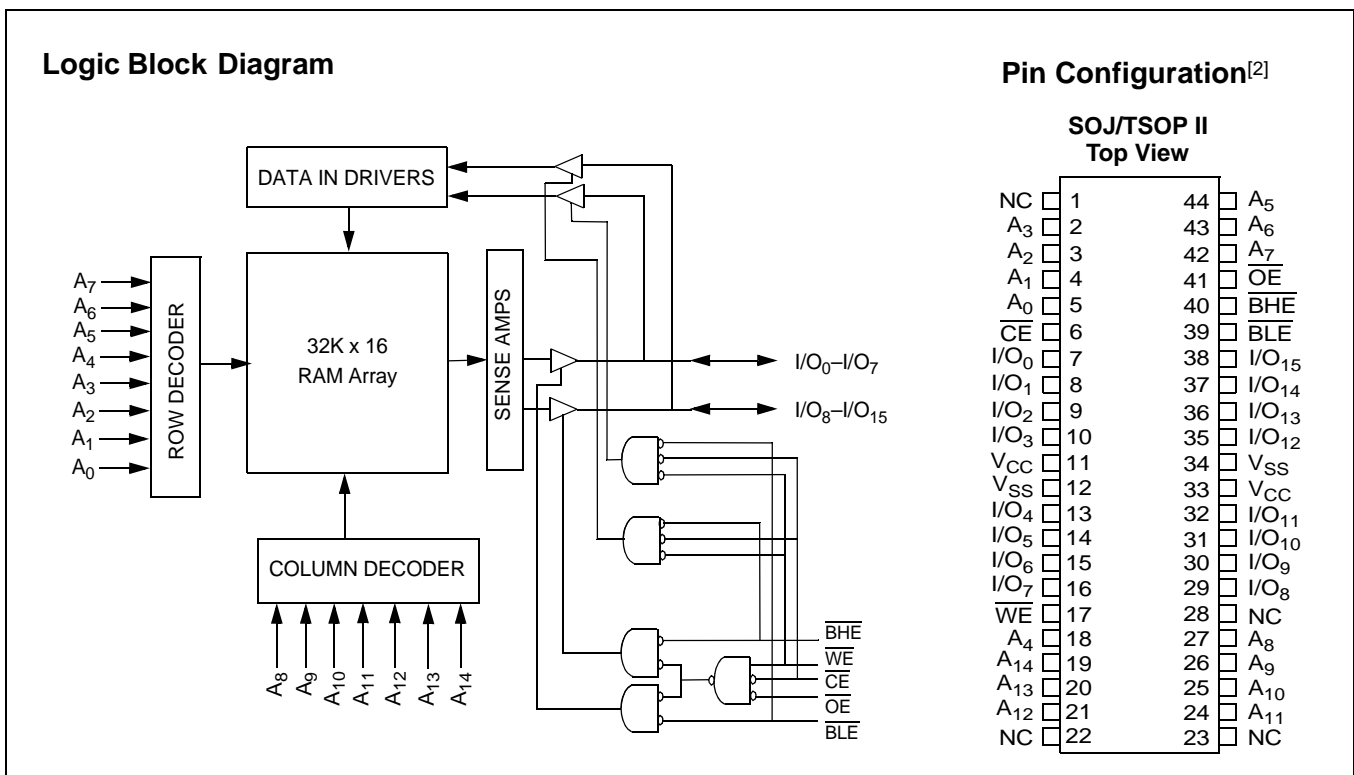
The CY7C1020DV33 is a high-performance CMOS static RAM organized as 32,768 words by 16 bits. This device has an automatic power-down feature that significantly reduces power consumption when deselected.

Writing to the device is accomplished by taking Chip Enable (\overline{CE}) and Write Enable (\overline{WE}) inputs LOW. If Byte Low Enable (\overline{BLE}) is LOW, then data from I/O pins (I/O_0 through I/O_7), is written into the location specified on the address pins (A_0 through A_{14}). If Byte High Enable (\overline{BHE}) is LOW, then data from I/O pins (I/O_8 through I/O_{15}) is written into the location specified on the address pins (A_0 through A_{14}).

Reading from the device is accomplished by taking Chip Enable (\overline{CE}) and Output Enable (\overline{OE}) LOW while forcing the Write Enable (\overline{WE}) HIGH. If Byte Low Enable (\overline{BLE}) is LOW, then data from the memory location specified by the address pins will appear on I/O_0 to I/O_7 . If Byte High Enable (\overline{BHE}) is LOW, then data from memory will appear on I/O_8 to I/O_{15} . See the truth table at the back of this data sheet for a complete description of read and write modes.

The input/output pins (I/O_0 through I/O_{15}) are placed in a high-impedance state when the device is deselected (\overline{CE} HIGH), the outputs are disabled (\overline{OE} HIGH), the \overline{BHE} and \overline{BLE} are disabled (\overline{BHE} , \overline{BLE} HIGH), or during a write operation (\overline{CE} LOW, and \overline{WE} LOW).

The CY7C1020DV33 is available in Pb-free 44-pin 400-Mil wide Molded SOJ and 44-pin TSOP II packages.



Notes

- For guidelines on SRAM system design, please refer to the 'System Design Guidelines' Cypress application note, available on the internet at www.cypress.com
- NC pins are not connected on the die.

Selection Guide

	–10 (Industrial)	–12 (Automotive)^[3]	Unit
Maximum Access Time	10	12	ns
Maximum Operating Current	60	100	mA
Maximum CMOS Standby Current	3	15	mA

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature –65°C to +150°C

Ambient Temperature with Power Applied –55°C to +125°C

Supply Voltage on V_{CC} to Relative GND^[4] –0.5V to +4.6V

DC Voltage Applied to Outputs in High-Z State^[4] –0.5V to $V_{CC} + 0.5V$

DC Input Voltage^[4] –0.5V to $V_{CC} + 0.5V$

Current into Outputs (LOW) 20 mA

Static Discharge Voltage > 2001V (per MIL-STD-883, Method 3015)

Latch-up Current > 200 mA

Operating Range

Range	Ambient Temperature	V_{CC}	Speed
Industrial	–40°C to +85°C	3.3V ± 0.3V	10 ns
Automotive	–40°C to +125°C		12 ns

Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions	–10 (Industrial)		–12 (Automotive)		Unit
			Min.	Max.	Min.	Max.	
V_{OH}	Output HIGH Voltage	$V_{CC} = \text{Min.}, I_{OH} = -4.0 \text{ mA}$	2.4		2.4		V
V_{OL}	Output LOW Voltage	$V_{CC} = \text{Min.}, I_{OL} = 8.0 \text{ mA}$		0.4		0.4	V
V_{IH}	Input HIGH Voltage		2.0	$V_{CC} + 0.3$	2.0	$V_{CC} + 0.3$	V
V_{IL}	Input LOW Voltage ^[4]		–0.3	0.8	–0.3	0.8	V
I_{IX}	Input Load Current	$GND \leq V_I \leq V_{CC}$	–1	+1	–1	+1	μA
I_{OZ}	Output Leakage Current	$GND \leq V_I \leq V_{CC}$, Output Disabled	–1	+1	–1	+1	μA
I_{CC}	V_{CC} Operating Supply Current	$V_{CC} = \text{Max.}, I_{OUT} = 0 \text{ mA}, f = f_{MAX} = 1/t_{RC}$	100 MHz	60		–	mA
			83 MHz	55		100	mA
			66 MHz	45		90	mA
			40 MHz	30		60	mA
I_{SB1}	Automatic CE Power-down Current—TTL Inputs	Max. V_{CC} , $\overline{CE} \geq V_{IH}$, $V_{IN} \geq V_{IH}$ or $V_{IN} \leq V_{IL}$, $f = f_{MAX}$		10		50	mA
I_{SB2}	Automatic CE Power-down Current—CMOS Inputs	Max. V_{CC} , $\overline{CE} \geq V_{CC} - 0.3V$, $V_{IN} \geq V_{CC} - 0.3V$, or $V_{IN} \leq 0.3V$, $f = 0$		3		15	mA

Notes

3. Automotive Product Information is Preliminary.

4. $V_{IL}(\text{min.}) = -2.0V$ and $V_{IH}(\text{max.}) = V_{CC} + 1V$ for pulse durations of less than 5 ns.

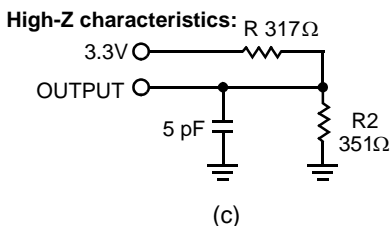
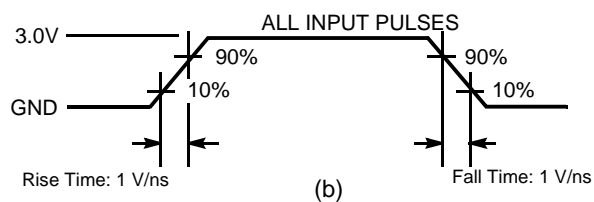
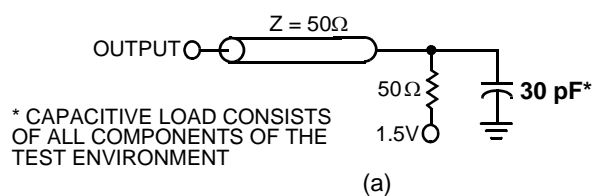
Capacitance^[5]

Parameter	Description	Test Conditions	Max.	Unit
C _{IN}	Input Capacitance	T _A = 25°C, f = 1 MHz, V _{CC} = 3.3V	8	pF
C _{OUT}	Output Capacitance		8	pF

Thermal Resistance^[5]

Parameter	Description	Test Conditions	SOJ	TSOP II	Unit
Θ _{JA}	Thermal Resistance (Junction to Ambient)	Still Air, soldered on a 3 × 4.5 inch, four-layer printed circuit board	59.52	53.91	°C/W
Θ _{JC}	Thermal Resistance (Junction to Case)		36.75	21.24	°C/W

AC Test Loads and Waveforms^[6]



Notes

5. Tested initially and after any design or process changes that may affect these parameters.
6. AC characteristics (except High-Z) are tested using the load conditions shown in Figure (a). High-Z characteristics are tested for all speeds using the test load shown in Figure (c).

Switching Characteristics Over the Operating Range ^[7]

Parameter	Description	–10 (Industrial)		–12 (Automotive)		Unit
		Min.	Max.	Min.	Max.	
Read Cycle						
t _{power} ^[8]	V _{CC} (typical) to the first access	100		100		μs
t _{RC}	Read Cycle Time	10		12		ns
t _{AA}	Address to Data Valid		10		12	ns
t _{OHA}	Data Hold from Address Change	3		3		ns
t _{ACE}	$\overline{\text{CE}}$ LOW to Data Valid		10		12	ns
t _{DOE}	$\overline{\text{OE}}$ LOW to Data Valid		5		6	ns
t _{LZOE}	$\overline{\text{OE}}$ LOW to Low-Z ^[9]	0		0		ns
t _{HZOE}	$\overline{\text{OE}}$ HIGH to High-Z ^[9, 10]		5		6	ns
t _{LZCE}	$\overline{\text{CE}}$ LOW to Low-Z ^[9]	3		3		ns
t _{HZCE}	$\overline{\text{CE}}$ HIGH to High-Z ^[9, 10]		5		6	ns
t _{PU} ^[11]	$\overline{\text{CE}}$ LOW to Power-up	0		0		ns
t _{PD} ^[11]	$\overline{\text{CE}}$ HIGH to Power-down		10		12	ns
t _{DBE}	Byte Enable to Data Valid		5		6	ns
t _{LZBE}	Byte Enable to Low-Z	0		0		ns
t _{HZBE}	Byte Disable to High-Z		5		6	ns
Write Cycle ^[12]						
t _{WC}	Write Cycle Time	10		12		ns
t _{SCE}	$\overline{\text{CE}}$ LOW to Write End	8		9		ns
t _{AW}	Address Set-up to Write End	8		9		ns
t _{HA}	Address Hold from Write End	0		0		ns
t _{SA}	Address Set-up to Write Start	0		0		ns
t _{PWE}	$\overline{\text{WE}}$ Pulse Width	7		8		ns
t _{SD}	Data Set-up to Write End	5		6		ns
t _{HD}	Data Hold from Write End	0		0		ns
t _{LZWE}	$\overline{\text{WE}}$ HIGH to Low-Z ^[9]	3		3		ns
t _{HZWE}	$\overline{\text{WE}}$ LOW to High-Z ^[9, 10]		5		6	ns
t _{BW}	Byte Enable to End of Write	7		8		ns

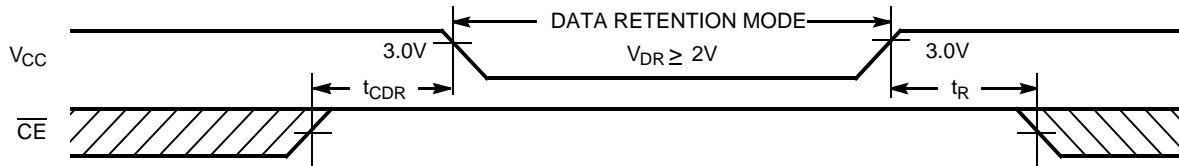
Notes

7. Test conditions assume signal transition time of 3 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V.
8. t_{POWER} gives the minimum amount of time that the power supply should be at typical V_{CC} values until the first memory access can be performed
9. t_{HZOE} , t_{HZBE} , t_{HZCE} , and t_{HZWE} are specified with a load capacitance of 5 pF as in (c) of AC Test Loads. Transition is measured when the outputs enter a high impedance state.
10. At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE} , t_{HZOE} is less than t_{LZOE} , and t_{HZWE} is less than t_{LZWE} for any given device.
11. This parameter is guaranteed by design and is not tested.
12. The internal Write time of the memory is defined by the overlap of $\overline{\text{CE}}$ LOW, $\overline{\text{WE}}$ LOW and $\overline{\text{BHE/BLE}}$ LOW. $\overline{\text{CE}}$, $\overline{\text{WE}}$ and $\overline{\text{BHE/BLE}}$ must be LOW to initiate a Write and the transition of these signals can terminate the Write. The input data set-up and hold timing should be referenced to the leading edge of the signal that terminates the Write.

Data Retention Characteristics (Over the Operating Range)

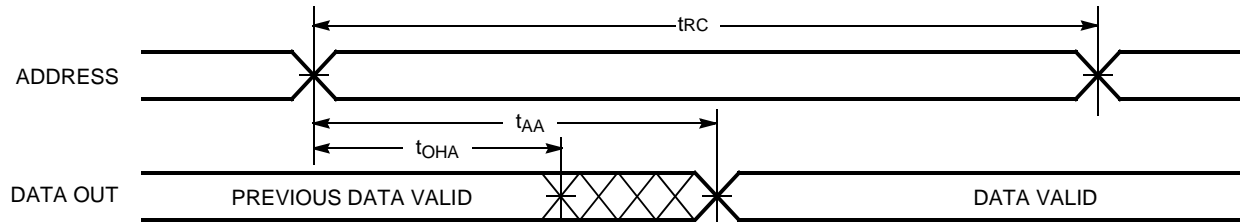
Parameter	Description	Conditions	Min.	Max.	Unit
V_{DR}	V_{CC}		2.0		V
I_{CCDR}	Data Retention Current	$V_{CC} = V_{DR} = 2.0V$, $\overline{CE} \geq V_{CC} - 0.3V$, $V_{IN} \geq V_{CC} - 0.3V$ or $V_{IN} \leq 0.3V$			
		Industrial		3	mA
		Automotive		15	mA
$t_{CDR}^{[5]}$	Chip Deselect to Data Retention Time		0		ns
$t_R^{[13]}$	Operation Recovery Time		t_{RC}		ns

Data Retention Waveform

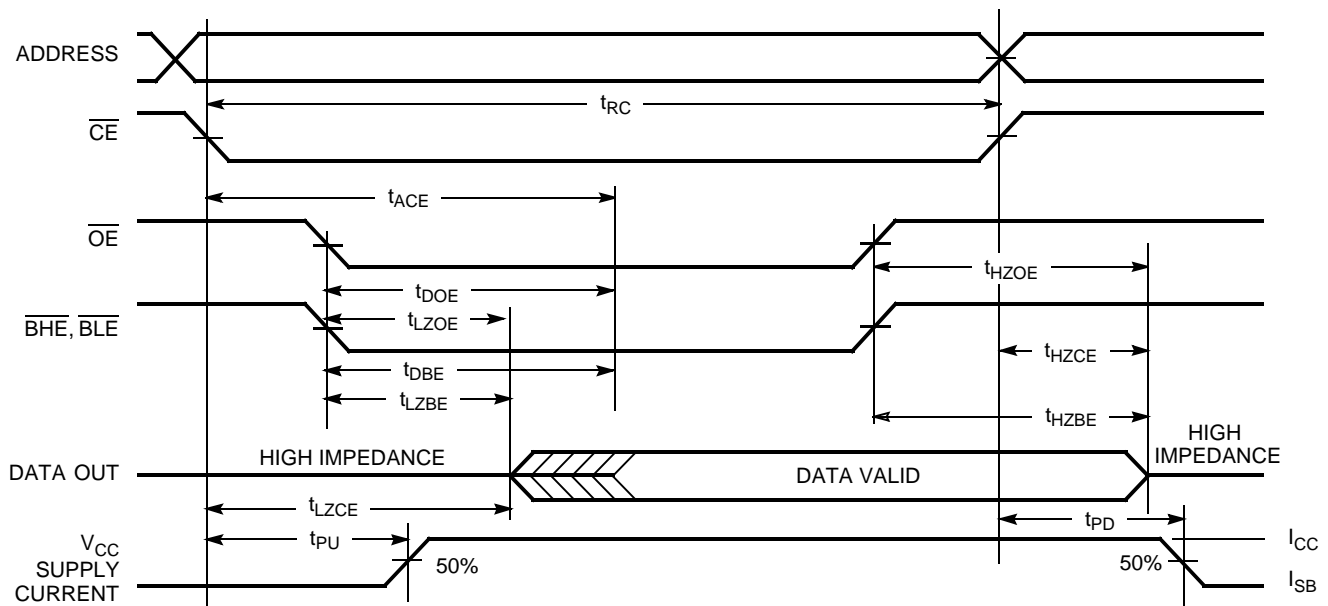


Switching Waveforms

Read Cycle No. 1 (Address Transition Controlled)^[14, 15]



Read Cycle No. 2 (\overline{OE} Controlled)^[15, 16]

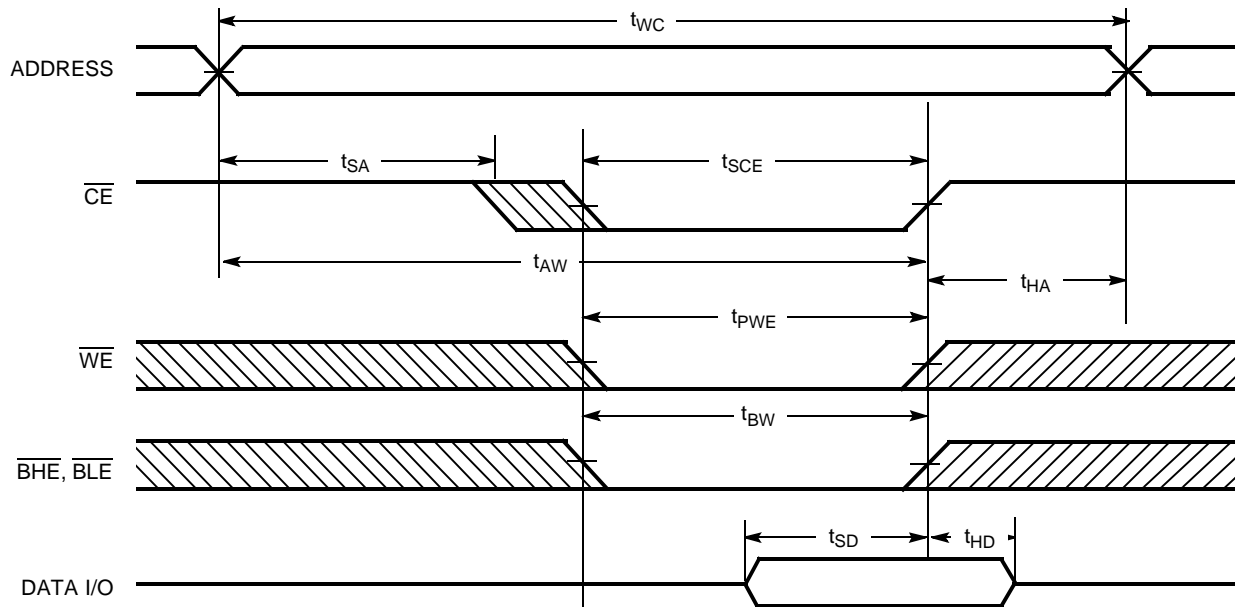


Notes:

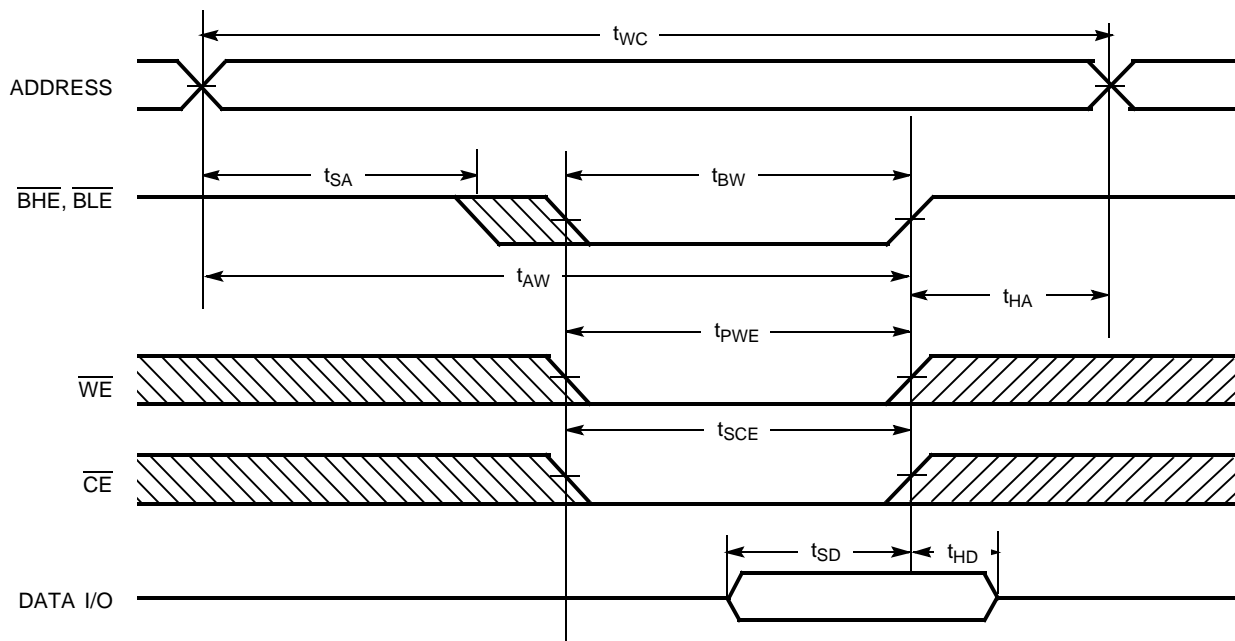
13. Full device operation requires linear V_{CC} ramp from V_{DR} to $V_{CC(min.)} \geq 50 \mu s$ or stable at $V_{CC(min.)} \geq 50 \mu s$.
14. Device is continuously selected. OE, CE, BHE and/or BLE = V_{IL} .
15. WE is HIGH for Read cycle.
16. Address valid prior to or coincident with \overline{CE} transition LOW.

Switching Waveforms (continued)

Write Cycle No. 1 ($\overline{\text{CE}}$ Controlled)^[17, 18]



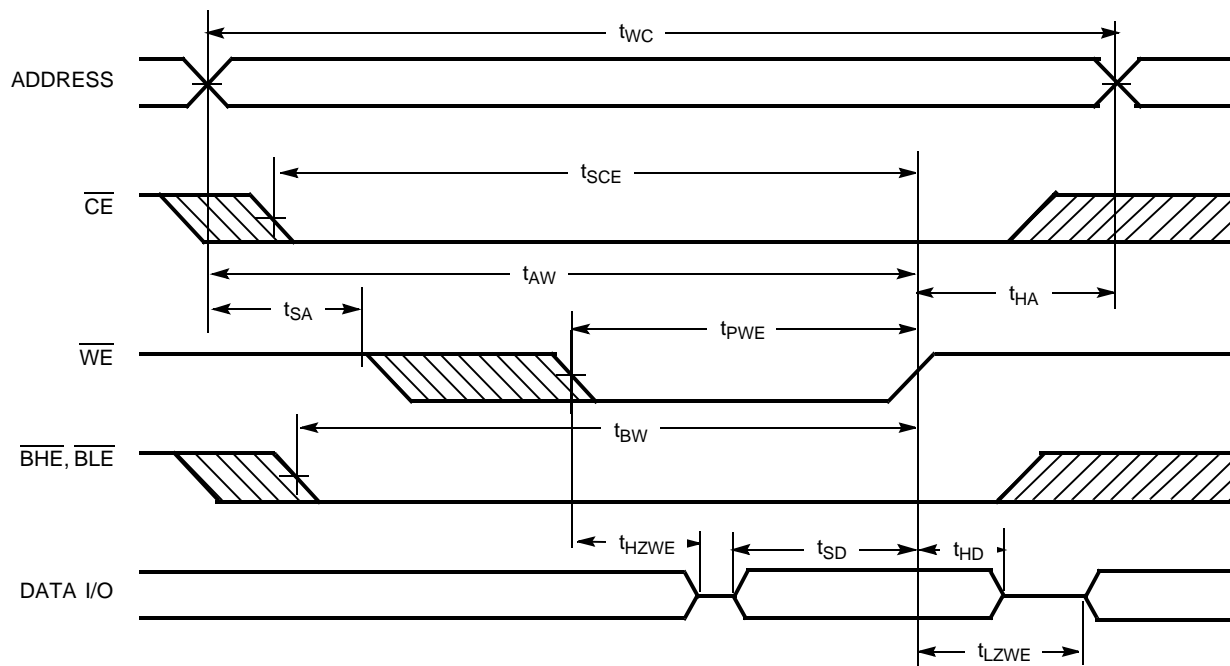
Write Cycle No. 2 ($\overline{\text{BLE}}$ or $\overline{\text{BHE}}$ Controlled)



Notes:

17. Data I/O is high impedance if $\overline{\text{OE}}$ or $\overline{\text{BHE}}$ and/or $\overline{\text{BLE}} = V_{\text{IH}}$.
18. If $\overline{\text{CE}}$ goes HIGH simultaneously with $\overline{\text{WE}}$ going HIGH, the output remains in a high-impedance state.

Switching Waveforms (continued)

Write Cycle No. 3 ($\overline{\text{WE}}$ Controlled, $\overline{\text{OE}}$ LOW)

Truth Table

$\overline{\text{CE}}$	$\overline{\text{OE}}$	$\overline{\text{WE}}$	$\overline{\text{BLE}}$	$\overline{\text{BHE}}$	I/O ₀ –I/O ₇	I/O ₈ –I/O ₁₅	Mode	Power
H	X	X	X	X	High-Z	High-Z	Power-down	Standby (I_{SB})
L	L	H	L	L	Data Out	Data Out	Read—All bits	Active (I_{CC})
			L	H	Data Out	High-Z	Read—Lower bits only	Active (I_{CC})
			H	L	High-Z	Data Out	Read—Upper bits only	Active (I_{CC})
L	X	L	L	L	Data In	Data In	Write—All bits	Active (I_{CC})
			L	H	Data In	High-Z	Write—Lower bits only	Active (I_{CC})
			H	L	High-Z	Data In	Write—Upper bits only	Active (I_{CC})
L	H	H	X	X	High-Z	High-Z	Selected, Outputs Disabled	Active (I_{CC})
L	X	X	H	H	High-Z	High-Z	Selected, Outputs Disabled	Active (I_{CC})

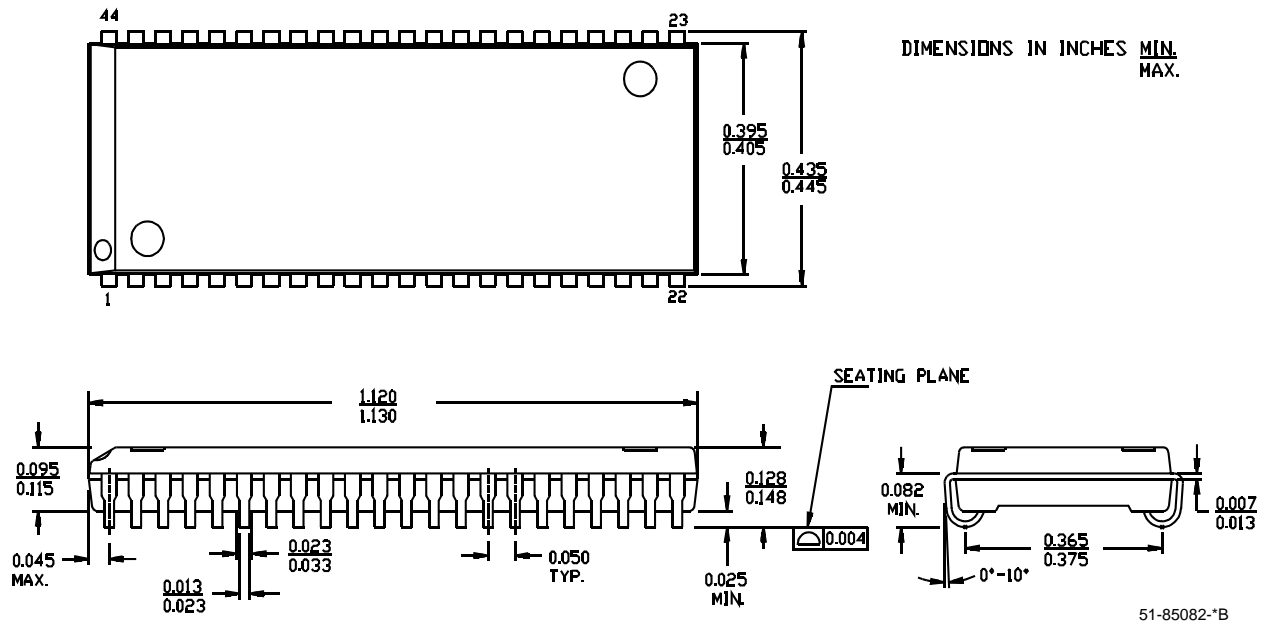
Ordering Information

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
10	CY7C1020DV33-10VXI	51-85082	44-pin (400-Mil) Molded SOJ (Pb-free)	Industrial
	CY7C1020DV33-10ZSXI	51-85087	44-pin TSOP Type II (Pb-free)	
12	CY7C1020DV33-12ZSXE	51-85087	44-pin TSOP Type II (Pb-free)	Automotive

Shaded areas contain advance information. Please contact your local Cypress sales representative for availability of these parts.

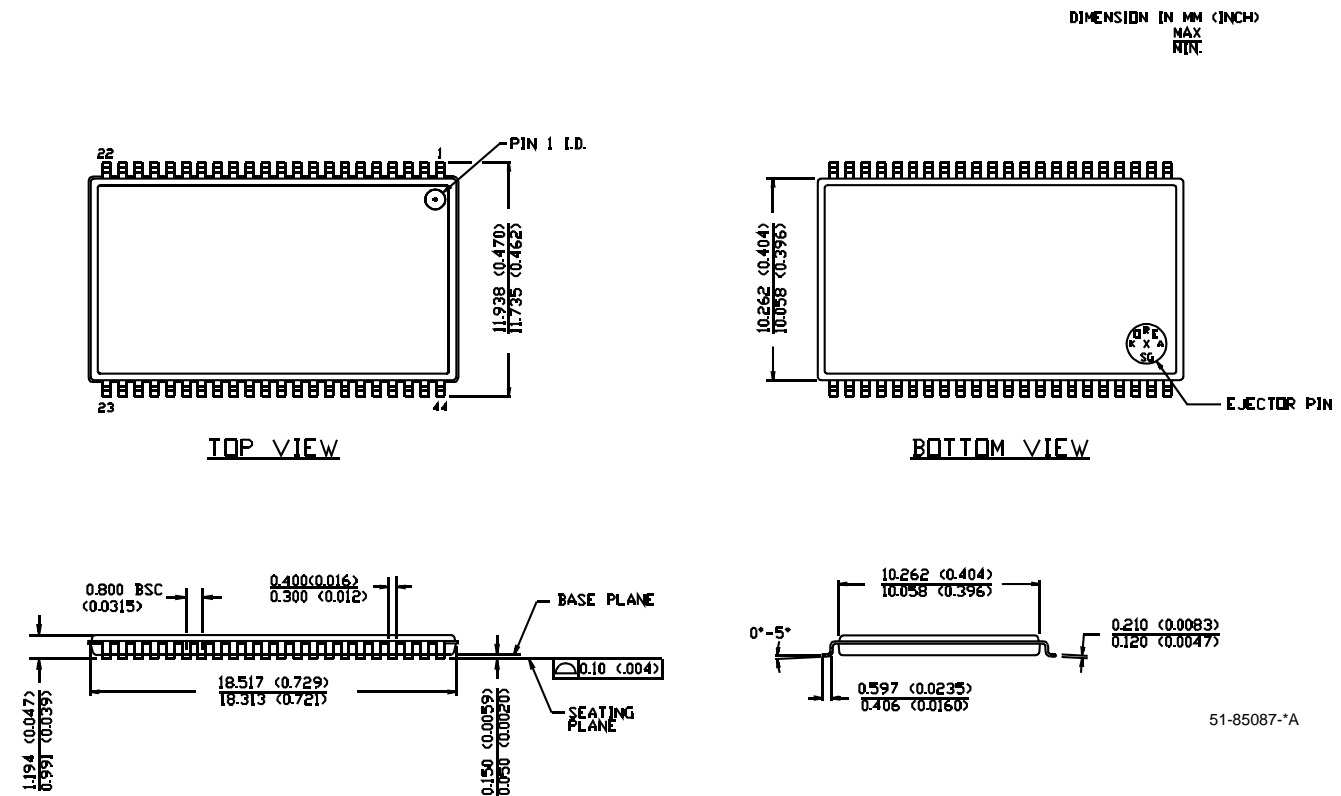
Package Diagrams

Figure 1. 44-pin (400-Mil) Molded SOJ (51-85082)



Package Diagrams (continued)

Figure 2. 44-Pin Thin Small Outline Package Type II (51-85087)



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Document History Page

Document Title: CY7C1020DV33, 512K (32K x 16) Static RAM
Document Number: 38-05461

REV.	ECN NO.	Issue Date	Orig. of Change	Description of Change
**	201560	See ECN	SWI	Advance Information data sheet for C9 IPP
*A	233695	See ECN	RKF	DC parameters modified as per EROS (Spec # 01-02165) Pb-free Offering in Ordering Information
*B	262950	See ECN	RKF	Changed I/O ₁ – I/O ₁₆ to I/O ₀ – I/O ₁₅ Added Data Retention Characteristics table Added T _{power} spec in Switching Characteristics table Added 44-SOJ package diagram Shaded Ordering Information
*C	307596	See ECN	RKF	Reduced Speed bins to –8 and –10 ns
*D	560995	See ECN	VKN	Converted from Preliminary to Final Removed Commercial operating range Removed 8 ns speed bin Added Automotive information Added I _{CC} values for the frequencies 83MHz, 66MHz and 40MHz Updated Thermal Resistance table Updated Ordering Information table Changed Overshoot spec from V _{CC} +2V to V _{CC} +1V in footnote #4