CY7C1046BN

1M x 4 Static RAM

Features

- Low active power
  — 825 mW (max)
- Low CMOS standby power
  — 44 mW (max)
- 2.0V data retention (400 μW at 2.0V retention)
- Automatic power down when deselected
- TTL-compatible inputs and outputs
- Easy memory expansion with CE and OE features
- Available in non Pb-free 400 mil wide 32-pin SOJ package

Functional Description

The CY7C1046BN is a high performance CMOS static RAM organized as 1,048,576 words by 4 bits. Easy memory expansion is provided by an active LOW Chip Enable ($\overline{CE}$), an active LOW Output Enable ($\overline{OE}$), and tri-state drivers.

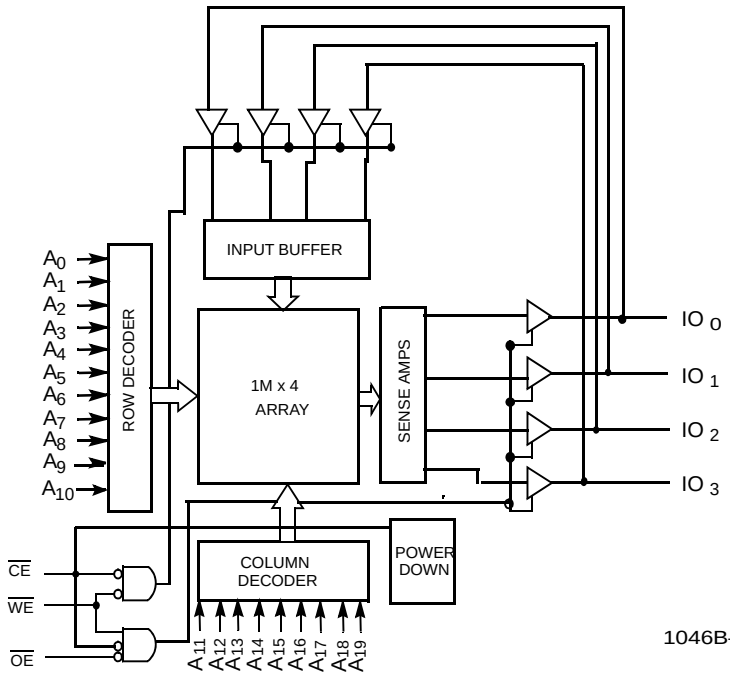
You write to the device by taking Chip Enable ($\overline{CE}$) and Write Enable ($\overline{WE}$) inputs LOW. Data on the four IO pins (IO_0 through IO_3) is then written into the location specified on the address pins (A_0 through A_{19}).

You read from the device by taking Chip Enable ($\overline{CE}$) and Output Enable ($\overline{OE}$) LOW while forcing Write Enable ($\overline{WE}$) HIGH. Under these conditions, the contents of the memory location specified by the address pins appears on the IO pins.

The four input and output pins (IO_0 through IO_3) are placed in a high impedance state when the device is deselected ($\overline{CE}$ HIGH), the outputs are disabled ($\overline{OE}$ HIGH), or when the write operation is active ($\overline{CE}$ LOW, and $\overline{WE}$ LOW).

The CY7C1046BN is available in a standard 400-mil-wide 32-pin SOJ package with center power and ground (revolutionary) pinout.

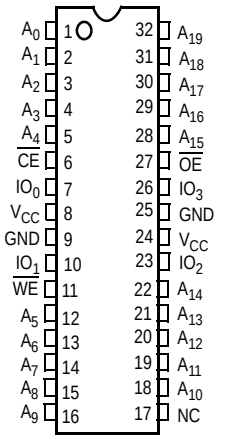
Logic Block Diagram



1046B–1

Pin Configuration

SOJ
TOP VIEW



1046B–2

Selection Guide

	7C1046BN-15
Maximum Access Time (ns)	15
Maximum Operating Current (mA)	150
Maximum CMOS Standby Current (mA)	8

Maximum Ratings

Exceeding maximum ratings may impair the useful life of the device. User guidelines are not tested.

Storage Temperature .....–65°C to +150°C

Ambient Temperature with Power Applied.....–55°C to +125°C

Supply Voltage on V_{CC} Relative to GND[1] .... –0.5V to +7.0V

DC Voltage Applied to Outputs in High-Z State[1] .....–0.5V to V_{CC} + 0.5V

DC Input Voltage[1].....–0.5V to V_{CC} + 0.5V

Current into Outputs (LOW)..... 20 mA

Static Discharge Voltage.....>2001V (in accordance with MIL-STD-883, Method 3015)

Latch-Up Current.....>200 mA

Operating Range

Range	Ambient Temperature[2]	V_{CC}
Commercial	0°C to +70°C	4.5V–5.5V

Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions	7C1046BN-15		Unit
			Min	Max	
V_{OH}	Output HIGH Voltage	V_{CC} = Min, I_{OH} = –4.0 mA	2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min, I_{OL} = 8.0 mA		0.4	V
V_{IH}	Input HIGH Voltage		2.2	V_{CC} + 0.3	V
V_{IL}	Input LOW Voltage[1]		–0.3	0.8	V
I_{IX}	Input Load Current	GND ≤ V_I ≤ V_{CC}	–1	+1	mA
I_{OZ}	Output Leakage Current	GND ≤ V_{OUT} ≤ V_{CC}, Output Disabled	–1	+1	mA
I_{CC}	V_{CC} Operating Supply Current	V_{CC} = Max, f = f_{MAX} = $1/t_{RC}$		150	mA
I_{SB1}	Automatic CE Power Down Current – TTL Inputs	Max V_{CC}, $\overline{CE}$ ≥ V_{IH}, V_{IN} ≥ V_{IH} or V_{IN} ≤ V_{IL}, f = f_{MAX}		20	mA
I_{SB2}	Automatic CE Power Down Current – CMOS Inputs	Max V_{CC}, $\overline{CE}$ ≥ V_{CC} – 0.3V, V_{IN} ≥ V_{CC} – 0.3V, or V_{IN} ≤ 0.3V, f = 0		8	mA

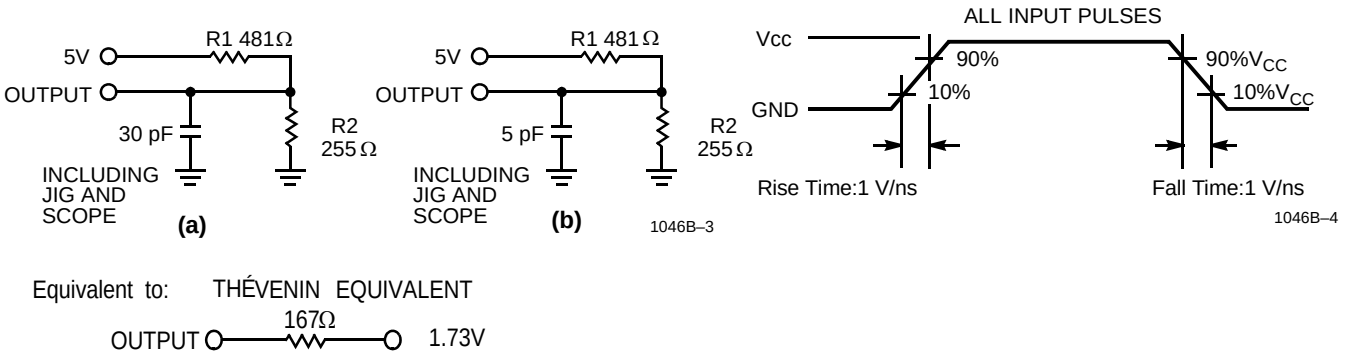
Capacitance[3]

Parameter	Description	Test Conditions	Max	Unit
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	6	pF
C_{OUT}	IO Capacitance		6	pF

Notes

1. V_{IL} (min) = –2.0V for pulse durations of less than 20 ns.
2. T_A is the "Instant On" case temperature.
3. Tested initially and after any design or process changes that may affect these parameters.

AC Test Loads and Waveforms



Equivalent to: THÉVENIN EQUIVALENT

Switching Characteristics (over the operating range)[4]

Parameter	Description	7C1046BN-15		Unit
		Min	Max	
READ CYCLE				
t_{power}	V_{CC}(typ) to the First Access[5]	1		µs
t_{RC}	Read Cycle Time	15		ns
t_{AA}	Address to Data Valid		15	ns
t_{OHA}	Data Hold from Address Change	3		ns
t_{ACE}	$\overline{CE}$ LOW to Data Valid		15	ns
t_{DOE}	$\overline{OE}$ LOW to Data Valid		7	ns
t_{LZOE}	$\overline{OE}$ LOW to Low-Z[7]	0		ns
t_{HZOE}	$\overline{OE}$ HIGH to High-Z[6, 7]		7	ns
t_{LZCE}	$\overline{CE}$ LOW to Low-Z[7]	3		ns
t_{HZCE}	$\overline{CE}$ HIGH to High-Z[6, 7]		7	ns
t_{PU}	$\overline{CE}$ LOW to Power Up	0		ns
t_{PD}	$\overline{CE}$ HIGH to Power Down		15	ns

Notes

4. Test conditions are based on signal transition times of 3 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified I_{OL}/I_{OH} and 30-pF load capacitance.
5. This part has a voltage regulator which steps down the voltage from 5V to 3.3V internally. t_{POWER} is the time that the power needs to be supplied above V_{CC}(typ) initially before a Read or Write operation can be initiated.
6. t_{HZOE}, t_{HZCE}, and t_{HZWE} are specified with a load capacitance of 5 pF as in part (b) of AC Test Loads. Transition is measured ±500 mV from steady-state voltage.
7. At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE}, t_{HZOE} is less than t_{LZOE}, and t_{HZWE} is less than t_{LZWE} for any given device.

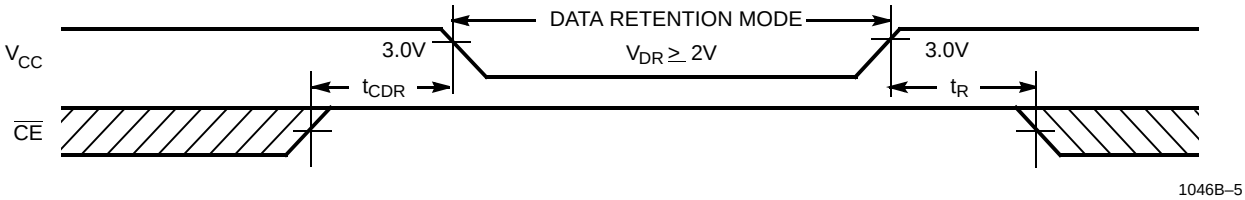
Switching Characteristics (over the operating range)[4] (continued)

Parameter	Description	7C1046BN-15		Unit
		Min	Max	
WRITE CYCLE[8, 9]				
t_{WC}	Write Cycle Time	15		ns
t_{SCE}	$\overline{CE}$ LOW to Write End	10		ns
t_{AW}	Address Setup to Write End	10		ns
t_{HA}	Address Hold from Write End	0		ns
t_{SA}	Address Setup to Write Start	0		ns
t_{PWE}	$\overline{WE}$ Pulse Width	10		ns
t_{SD}	Data Setup to Write End	8		ns
t_{HD}	Data Hold from Write End	0		ns
t_{LZWE}	$\overline{WE}$ HIGH to Low-Z[7]	3		ns
t_{HZWE}	$\overline{WE}$ LOW to High-Z[6, 7]		7	ns

Data Retention Characteristics (over the operating range)

Parameter	Description		Conditions[10]	Min	Max	Unit
V_{DR}	V_{CC} for Data Retention			2.0		V
I_{CCDR}	Data Retention Current	Com'l	$V_{CC} = V_{DR} = 2.0V$,		200	µA
t_{CDR}[3]	Chip Deselect to Data Retention Time		$\overline{CE} \geq V_{CC} - 0.3V$	0		ns
t_R	Operation Recovery Time		$V_{IN} \geq V_{CC} - 0.3V$ or $V_{IN} \leq 0.3V$	200		µs

Data Retention Waveform

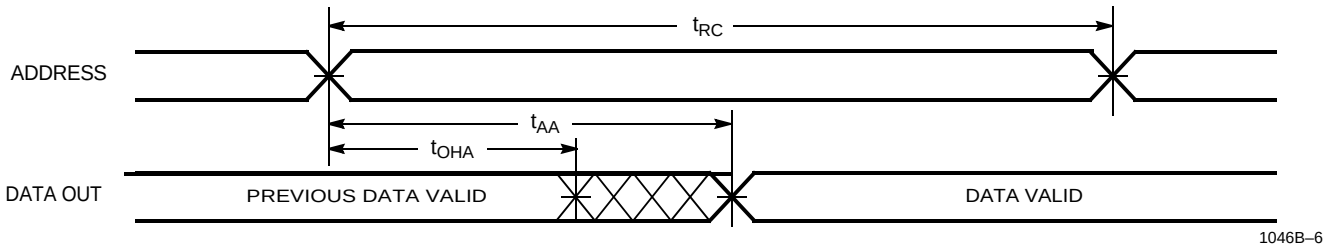


Notes

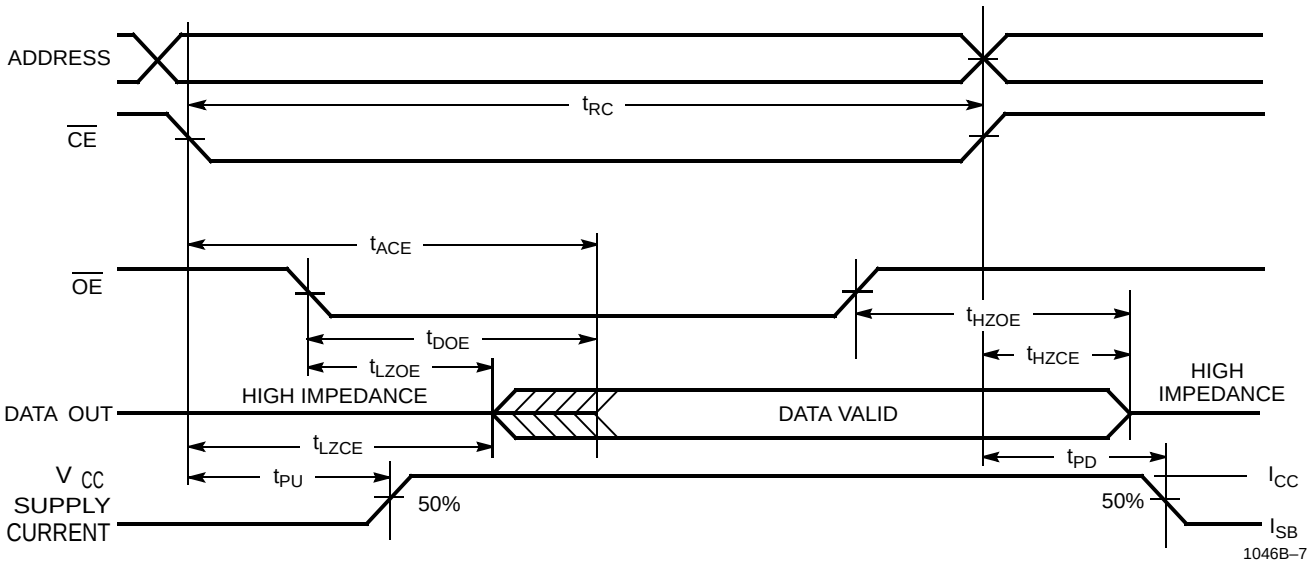
8. The internal memory write time is defined by the overlap of $\overline{CE}$ LOW, and $\overline{WE}$ LOW. $\overline{CE}$ and $\overline{WE}$ must be LOW to initiate a write, and the transition of either of these signals can terminate the write. The input data setup and hold timing must be referenced to the leading edge of the signal that terminates the write.
9. The minimum write cycle time for write cycle 3 ($\overline{WE}$ controlled, $\overline{OE}$ LOW) is the sum of t_{HZWE} and t_{SD}.
10. No input may exceed V_{CC} + 0.5V.

Switching Waveforms

Read Cycle 1[11, 12]



Read Cycle 2 ($\overline{OE}$ controlled)[12, 13]

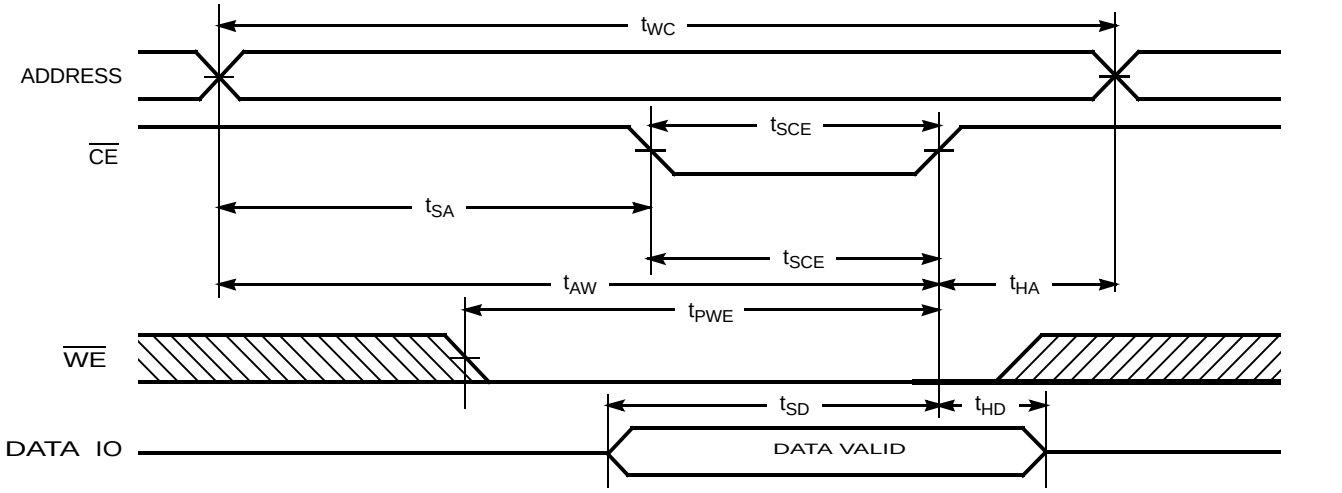


Notes

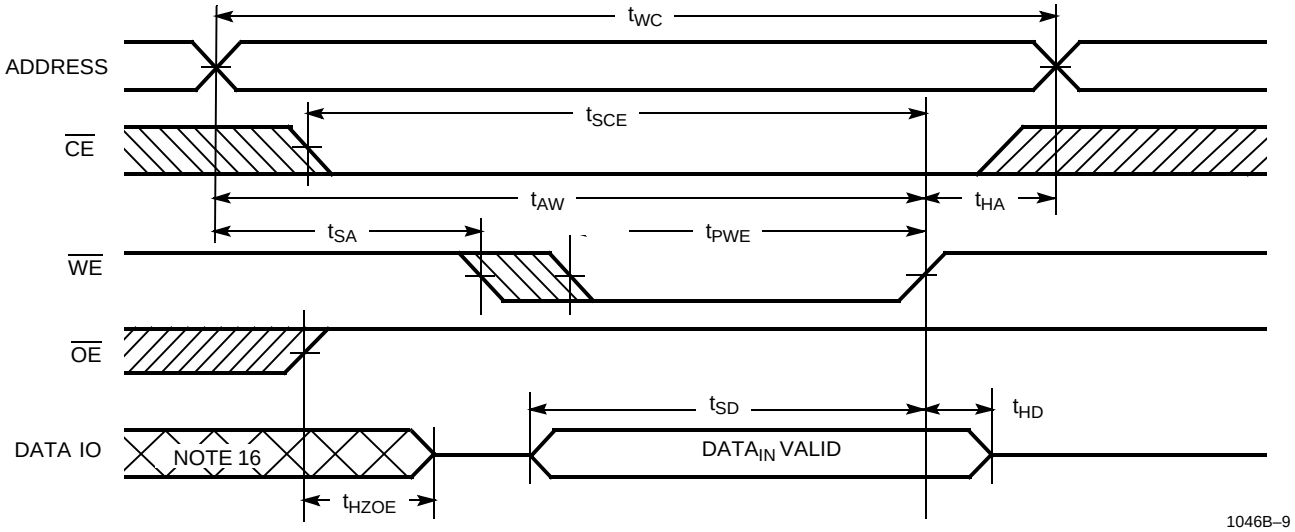
11. Device is continuously selected. $\overline{OE}$, $\overline{CE}$ = V_{IL}.
12. $\overline{WE}$ is HIGH for read cycle.
13. Address valid before or similar to $\overline{CE}$ transition LOW.

Switching Waveforms (continued)

Write Cycle 1 ($\overline{CE}$ controlled)[14, 15]



Write Cycle 2 ($\overline{WE}$ controlled, $\overline{OE}$ HIGH during write)[14, 15]

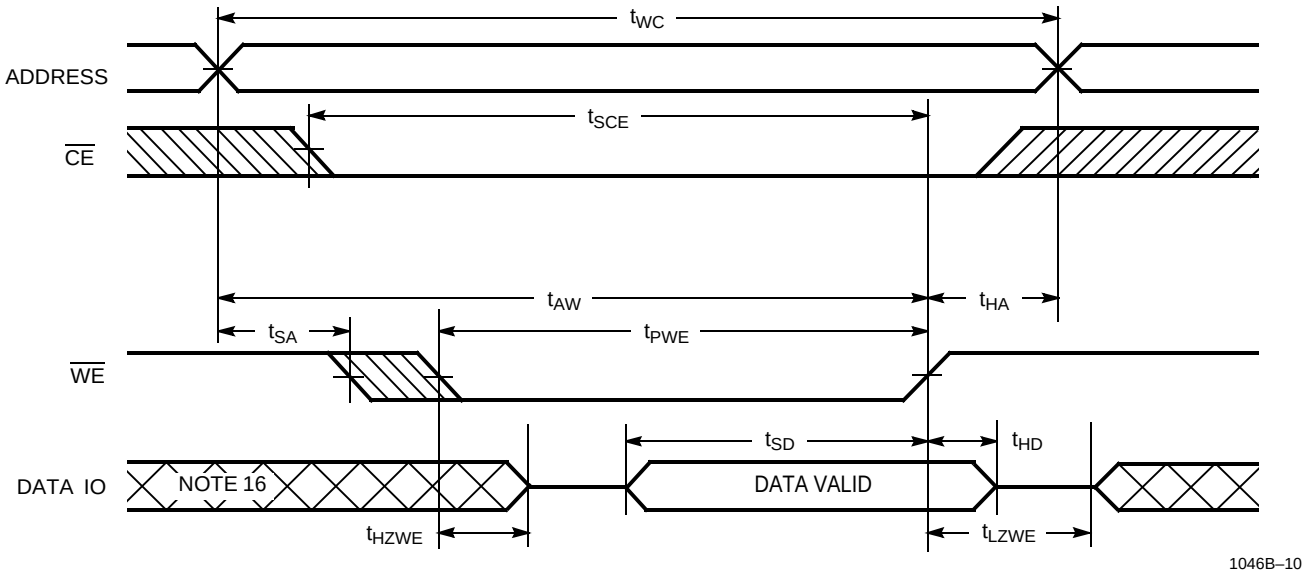


Notes

14. Data IO is high impedance if $\overline{OE} = V_{IH}$.
15. If $\overline{CE}$ goes HIGH simultaneously with $\overline{WE}$ going HIGH, the output remains in a high impedance state.
16. During this period the IOs are in the output state and input signals must not be applied.

Switching Waveforms (continued)

Write Cycle 3 ($\overline{WE}$ controlled, $\overline{OE}$ LOW)[15]

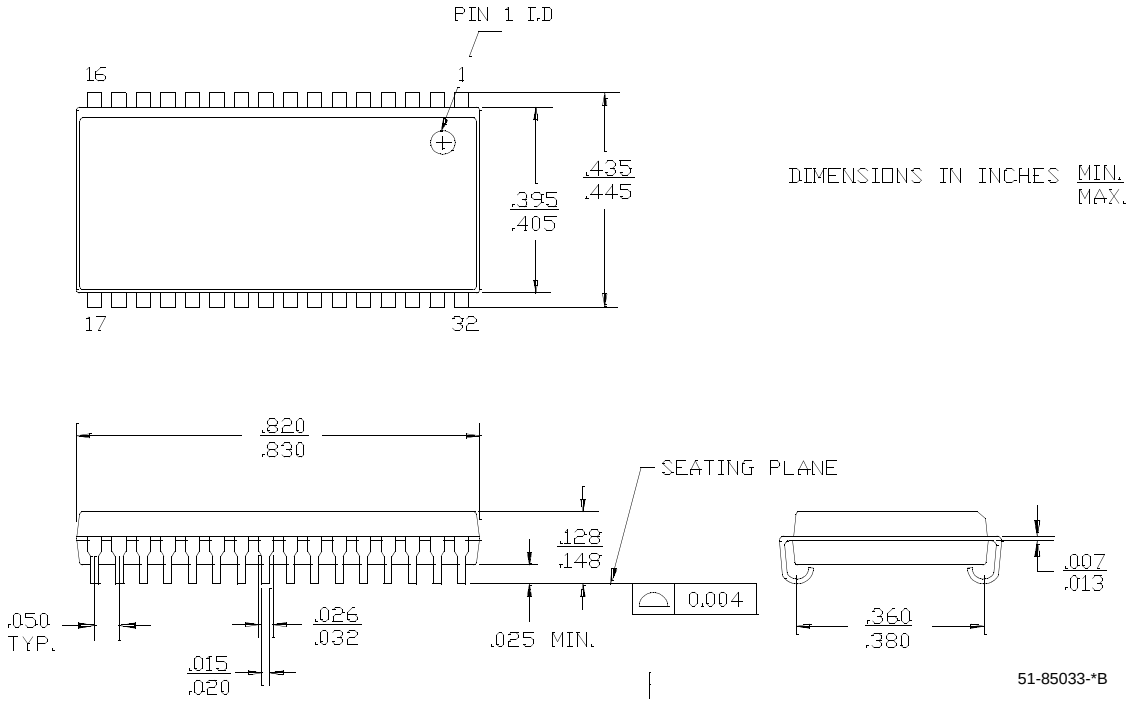


Ordering Information

Speed (ns)	Ordering Code	Package Diagram	Package Type	Operating Range
15	CY7C1046BN-15VC	51-85033	32-Pin (400-Mil) Molded SOJ	Commercial

Package Diagram

Figure 1. 32-pin (400-Mil) Molded SOJ, 51-85033



Document History Page

Document Title: CY7C1046BN 1M x 4 Static RAM Document Number: 001-11924				
REV.	**ECN NO.**	**Issue Date**	**Orig. of Change**	**Description of Change**
**	610496	See ECN	NXR	New data sheet